RCA

Solid
State

es • B-Series • B-Series • B-Series • B-Series • B-Series • B-Series • B-Series •

es • A-Series • A-Series • A-Series • A-Series • A-Series • A-Series • A-Se

eeping & Special • Timekeeping & Special • Timekeeping & Special • Timekeeping & S

rocessors • Microprocessors • Microprocessors • Microprocessors • Microproces

COS/MOS Integrated Circuits

RCA COS/MOS Integrated Circuits

This DATABOOK contains complete technical information on the full line of RCA standard commercial COS/MOS integrated circuits: standard A- and B-series types, timekeeping and special products, and microprocessor products. An Index to Devices provides a complete listing of types.

The DATABOOK is divided into nine major sections. The first section includes classification and selection charts, functional diagrams, and photographs of available package options. This section is followed by a discussion of general considerations that should be taken into account in the operation and application of COS/MOS integrated circuits.

Four separate data sections provide definitive ratings and characteristics for (1) high-voltage B-series types, (2) A-series types, (3) timekeeping and special products, and (4) CDP-1800-series microprocessor products. Data pages for individual devices are included as nearly as possible in alpha-numerical sequence of type numbers. Because some devices are grouped together to show similarity of function or data, individual type numbers may be out of sequence. If you don't find the type number you're looking for where you expect it to be, check the Index to Devices.

The data sections are followed by a Dimensional Outlines section, an Application Notes section, and a section that lists RCA Sales Offices, Manufacturers' Representatives, and Authorized Distributors.

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The device data shown for some types are indicated as preliminary or objective. **Preliminary data** are intended for guidance purposes in evaluating devices for equipment design. Such data are shown for types currently being designed for inclusion in our standard line of commercially available products. **Objective data** are intended for engineering evaluation of types in the initial stages of design. The type designations and data are subject to change, unless otherwise arranged. No obligations are assumed for notice of change or future manufacture of these devices. For current information on the status of preliminary or objective programs, please contact your local RCA sales office.

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Index to Devices

This index does not include package designation suffix letters for individual type numbers; the various packages available are shown in the data section.

Index To Application Notes

Product Selection Guides

Function Classification Charts

COS/MOS B-SERIES INTEGRATED CIRCUITS

GATES

SINGLE-LEVEL

NOR/NAND	OR/AND	BUFF./CONV., INVERTERS
CD4000B	CD4071B	CD4007UB
CD4000UB	CD4072B	CD4009UB
CD4001B	CD4073B	CD4010B
CD4001UB	CD4075B	CD4041UB
CD4002B	CD4081B	CD4049UB
CD4002UB	CD4082B	CD4050B
CD4011B	CD4068B	CD4069UB
CD4011UB	CD4078B	CD4502B
CD4012B		CD40107BE
CD4012UB		
CD4023B		LEVEL SHIFTER
CD4023UB		CD4009UB
CD4025B		CD4010B
CD4025UB		CD4049UB
CD4068B		CD4050B
CD4078B		CD40109B
CD40107B		

MULTI-LEVEL

MULTIFUNCTION/ AOI	DECODERS/ ENCODERS	SCHMITT TRIGGER
CD4019B	CD4028B	CD4093B
CD4030B	CD4514B	CD40106B
CD4048B	CD4515B	
CD4070B■	CD4532B	
CD4077B■	CD4555B*	
CD4085B	CD4556B*	
CD4086B		

■See Comparators

*See Demultiplexers

MULTIVIBRATORS

FLIP-FLOPS/ LATCHES	ASTABLE/ MONOSTABLE
CD4013B	CD4047B
CD4027B	CD4098B
CD4042B	
CD4043B	
CD4044B	
CD4076B**	
CD4095B	
CD4096B	
CD4099B**	
CD4508B	
CD40174B	

**See Storage Registers

REGISTERS

SHIFT	STORAGE	FIFO BUFFER
CD4006B	CD4076B	CD40105B
CD4014B	CD4099B	
CD4015B	CD40108B●	
CD4021B	CD40208B●	
CD4031B		
CD4034B		
CD4035B		
CD4094B		
CD40100B		
CD40104B		
CD40194B		

●See Multiport Register

COUNTERS

BINARY RIPPLE	SYNCHRONOUS
CD4020B	CD4017B
CD4024B	CD4018B
CD4040B	CD4022B
CD4060B	CD4029B
	CD4510B
CLOCK TIMER CD4045B	CD4516B
	CD4518B
	CD4520B
	CD40102B
	CD40103B
	CD40160B
	CD40161B
	CD40162B
	CD40163B
	CD40192B
	CD40193B

DISPLAY DRIVERS

WITH COUNTER	FOR LCD☆ DRIVE	FOR LED●● DRIVE
CD4026B	CD4054B	CD4511B
CD4033B	CD4055B	
CD40110B	CD4056B	

☆Liquid Crystal Display

●●Light-Emitting Diode

MULTIPLEXERS/ DEMULTIPLEXERS

ANALOG/ DIGITAL DATA SELECTORS

CD4016B▲
CD4019B
CD4051B
CD4052B
CD4053B
CD4066B▲
CD4067B
CD4097B
CD4555B⊕
CD4556B⊕
CD40257B

▲See Quad Bilateral Switch

⊕See Decoders/ Encoders

PHASE-LOCKED LOOP

CD4046B

ARITHMETIC CIRCUITS

ADDERS/ COMPARATORS

CD4008B
CD4030B
CD4032B
CD4038B
CD4063B
CD4070B♦
CD4077B♦

♦See Multifunction/ AOI

ALU/RATE MULTIPLIERS

CD4089B
CD4527B
CD40181B
CD40182B

PARITY GENERATOR/ CHECKER

CD40101B

MULTIPORT REGISTER

CD40108B
CD40208B

QUAD BILATERAL SWITCHES

CD4016B♦
CD4066B♦

♦See Multiplexers

COS/MOS A-SERIES INTEGRATED CIRCUITS

GATES						MULTIVIBRATORS	
SINGLE-LEVEL			MULTI-LEVEL				
NOR/NAND	OR/AND	BUFF./CONV., INVERTERS	MULTIFUNCTION/ AOI	DECODERS/ ENCODERS	SCHMITT TRIGGER	FLIP-FLOPS/ LATCHES	ASTABLE/ MONOSTABLE
CD4000A CD4001A CD4002A CD4011A CD4012A CD4023A CD4025A		CD4007A CD4009A CD4010A CD4041A CD4049A CD4050A	CD4019A CD4030A■ CD4037A CD4048A ■See Comparators	CD4028A		CD4013A CD4027A CD4042A CD4043A CD4044A	CD4047A

REGISTERS			COUNTERS		DISPLAY DRIVERS		
SHIFT	STORAGE	FIFO BUFFER	BINARY RIPPLE	SYNCHRONOUS	WITH COUNTER	FOR LCD☆ DRIVE	FOR LED●● DRIVE
Static CD4006A CD4014A CD4015A CD4021A CD4031A CD4034A CD4035A Dynamic CD4062A			CD4020A CD4024A CD4040A CD4045A CD4060A	CD4017A CD4018A CD4022A CD4029A CD4059A	CD4026A CD4033A		

MULTIPLEXERS/ DEMULTIPLEXERS	PHASE-LOCKED LOOP	ARITHMETIC CIRCUITS				MEMORIES RAM'S		QUAD BILATERAL SWITCHES
ANALOG/ DIGITAL DATA SELECTORS		ADDERS/ COMPARATORS	ALU/RATE MULTIPLIERS	PARITY GENERATOR/ CHECKER	MULTIPORT REGISTER	WORD-ORGANIZED	BIT-ORGANIZED	
CD4016A▲ CD4019A‡ CD4066A▲ ‡See Multifunction A01 ▲See Quad Bilateral Switch	CD4046A	CD4008A CD4032A CD4038A CD4030A♦ ♦See Multifunction/ AOI	CD4057A			CD4036A CD4039A	CD4061A	CD4016A♦ CD4066A♦ ♦See Multiplexers

☆ Liquid Crystal Display ●● Light-Emitting Diode

Function Classification Charts

COS/MOS TIMEKEEPING AND SPECIAL PRODUCTS

Watches			Clocks	Auto Clocks	Industrial Timer	Special Products	
3½ Digit	4 Digit	6 Digit				Crosspoint Switches	Decoder/ Drivers
CD22001 CD22002 CD22003 CD22009	CD22006 CD22007	CD22008	CD22011	CD22012 CD22013 CD22014 CD22015	CD220017	CD22100 CD22101 CD22102	CD22925 CD22926 CD22927 CD22928

MICROPROCESSOR PRODUCTS

CPU	ROM	RAM	I/O
CDP1802	CDP1831 CDP1832 CDP1833 CDP1834	CDP1821S CDP1822S CDP1823S CDP1824	CDP1852 CDP1853 CDP1854 CDP1856 CDP1857 CDP1858 CDP1859 Video Display Controller CDP1861

COS/MOS A- AND B-SERIES INTEGRATED CIRCUITS

Function	Type No.	No. of Pins
Gates		
NOR/NAND		
Dual 4-input NOR	**CD4002B**	14
	CD4002UB	14
	CD4002A	14
Dual 4-input NAND	**CD4012B**	14
	CD4012UB	14
	CD4012A	14
Triple 3-input NOR	**CD4025B**	14
	CD4025UB	14
	CD4025A	14
Triple 3-input NAND	**CD4023B**	14
	CD4023UB	14
	CD4023A	14
Quad 2-input NOR	**CD4001B**	14
	CD4001UB	14
	CD4001A	14
Quad 2-input NAND	**CD4011B**	14
	CD4011UB	14
	CD4011B	14
8-input NOR/OR	**CD4078B**	14
8-input NAND/AND	**CD4068B**	14
Dual 3-input NOR plus inverter	**CD4000B**	14
	CD4000UB	14
	CD4000A	14
Dual 2-input NAND buffer/driver	**CD40107B**	8
Level Shifter		
Quad low-to-high voltage	**CD40109B**	16
Hex high-to-low voltage (inverting)	**CD4009UB**	16
	CD4009A	16
	CD4049UB	16
	CD4049A	16
Hex high-to-low voltage (non-inverting)	**CD4010B**	16
	CD4010A	16
	CD4050B	16
	CD4050A	16
OR/AND		
Dual 4-input OR	**CD4072B**	14
Dual 4-input AND	**CD4082B**	14
Triple 3-input OR	**CD4075B**	14
Triple 3-input AND	**CD4073B**	14
Quad 2-input OR	**CD4071B**	14
Quad 2-input AND	**CD4081B**	14
Buffers and Inverters		
Dual complementary pair plus inverter	**CD4007UB**	14
	CD4007A	14
Hex inverter	**CD4069UB**	14
Strobed hex inverter/buffer	**CD4502B**	16

Function	Type No.	No. of Pins
Gates (cont'd)		
Buffers and Inverters (cont'd)		
Hex buffer/converter (inverting)	**CD4009UB**	16
	CD4009A	16
Hex buffer/converter (inverting)	**CD4049UB**	16
	CD4049A	16
Hex buffer/converter (non-inverting)	**CD4010B**	16
	CD4010A	16
Hex buffer/converter (non-inverting)	**CD4050B**	16
	CD4050A	16
Quad true/complement buffer	**CD4041UB**	14
	CD4041A	14
Dual 2-input NAND buffer/driver	**CD40107B**	8
Multifunction/AOI		
Triple AND-OR bi-phase pairs	**CD4037A**	14
Quad exclusive-OR	**CD4030B**	14
	CD4030A	14
Quad exclusive-OR	**CD4070B**	14
Quad exclusive-NOR	**CD4077B**	14
Quad AND/OR Select	**CD4019B**	16
	CD4019A	16
Dual 2-wide, 2-input AND/OR invert (AOI)	**CD4085B**	14
Expandable 4-wide, 2-input AND/OR invert (AOI)	**CD4086B**	14
Multifunctional expandable 8-input (3 state output)	**CD4048B**	16
	CD4048B	16
Decoders/Encoders		
BCD-to-decimal decoder	**CD4028B**	16
	CD4028A	16
8-input priority encoder	**CD4532B**	16
4-bit latch/4-to-16 line decoder (outputs high)	**CD4514B**	24
4-bit latch/4-to-16 line decoder (outputs low)	**CD4515B**	24
Dual 1-of-4 decoder/demultiplexer (outputs high)	**CD4555B**	16
Dual 1-of-4 decoder/demultiplexer (outputs low)	**CD4556B**	16
Schmitt Trigger		
Quad 2-input NAND	**CD4093B**	14
Hex	**CD40106B**	14
Multivibrators		
Monostable/astable	**CD4047B**	14
	CD4047A	14
Dual monostable	**CD4098B**	16

Function Selection Charts

COS/MOS A- AND B-SERIES INTEGRATED CIRCUITS

Function	Type No.	No. of Pins
Multivibrators (cont'd)		
Flip-Flops		
Dual "D" with set/reset capability	**CD4013B**	14
	CD4013A	14
Dual "J-K" with set/reset capability	**CD4027B**	16
	CD4027A	16
Gated "J-K" (non-inverting)	**CD4095B**	14
Gated "J-K" (inverting and non-inverting)	**CD4096B**	14
Hex "D"	**CD40174B**	16
4-bit "D" with 3-state outputs	**CD4076B**	14
Latches		
Quad clocked "D"	**CD4042B**	16
	CD4042A	16
Quad NOR R/S (3-state outputs)	**CD4043B**	16
	CD4043A	16
Quad NAND R/S (3-state outputs)	**CD4044B**	16
	CD4044A	16
Dual 4-bit	**CD4508B**	24
8-bit addressable	**CD4099B**	16
Registers		
Shift Registers-Static		
Dual 4-stage with serial input/parallel output	**CD4015B**	16
	CD4015A	16
18-stage	**CD4006B**	14
	CD4006A	14
64-stage	**CD4031B**	14
	CD4031A	14
8-stage with synchronous parallel or serial input/serial output	**CD4014B**	16
	CD4014A	16
8-stage with asynchronous parallel input or synchronous serial input/serial output	**CD4021B**	16
	CD4021A	16
4-stage parallel-in/parallel-out with J-K input and true/complement output	**CD4035B**	16
	CD4035A	16
8-stage bidirectional parallel or serial input/parallel output	**CD4034B**	24
	CD4034A	24
4-bit left/right	**CD40194B**	16
3-state 4-bit left/right	**CD40104B**	16
32-bit left/right	**CD40100B**	16
8-stage shift-and-store bus	**CD4094B**	16

Function	Type No.	No. of Pins
Registers (cont'd)		
Storage Registers		
8-bit addressable latch	**CD4099B**	16
4-bit "D"-type with 3-state outputs	**CD4076B**	16
4 X 4 Multiport	**CD40108B**	24
4 X 4 Multiport	**CD40208B**	24
FIFO Buffer Registers		
4-bit X 16 word	**CD40105B**	16
Counters		
Binary Ripple		
7-stage	**CD4024B**	14
	CD4024A	14
12-stage	**CD4040B**	16
	CD4040A	16
14-stage	**CD4020B**	16
	CD4020A	16
14-stage counter/divider and oscillator	**CD4060B**	16
	CD4060A	16
Clock Timer		
21-stage	**CD4045B**	14
	CD4045A	14
Synchronous		
Decade counter/divider plus 10 decoded decimal outputs	**CD4017B**	16
	CD4017A	16
Divide-by-8 counter/divider with 8 decimal outputs	**CD4022B**	16
	CD4022A	16
Presettable divide-by-"N" counter, fixed or programmable	**CD4018B**	16
	CD4018A	16
Programmable divide-by-"N" counter	**CD4059A**	24
Presettable up/down counter, binary or BCD-decade	**CD4029B**	16
	CD4029A	16
Presettable 4-bit BCD up/down counter	**CD4510B**	16
Presettable 4-bit binary up/down counter	**CD4516B**	16
Presettable 2-decade BCD down counter	**CD40102B**	16
Presettable 8-bit binary down counter	**CD40103B**	16
Presettable 4-bit BCD up/down counter	**CD40192B**	16

COS/MOS A- AND B-SERIES INTEGRATED CIRCUITS

Function	Type No.	No. of Pins
Registers (cont'd)		
Synchronous (cont'd)		
Presettable 4-bit binary up/down counter	**CD40193B**	16
Dual BCD up counter	**CD4518B**	16
Bual binary up counter	**CD4520B**	16
Decade counter/asynchronous clear	**CD40160B**	16
Binary counter/asynchronous clear	**CD40161B**	16
Decade counter/synchronous clear	**CD40162B**	16
Binary counter/synchronous clear	**CD40163B**	16
Display Drivers		
With Counter		
Decade counter/divider with 7-segment display outputs and display enable	**CD4026B**	16
	CD4026A	16
Decade counter/divider with 7-segment display outputs and ripple blanking	**CD4033B**	16
	CD4033A	16
Up/Down Counter-Latch-Decoder-Driver	**CD40110B**	16
For Liquid-Crystal-Display Drive		
4-line	**CD4054B**	16
BCD-to-7-segment decoder/driver with "display-frequency"output	**CD4055B**	16
BCD-to-7-segment decoder/driver with strobed-latch function	**CD4056B**	16
For Light-Emitting-Diode Drive		
BCD-to-7-segment latch decoder/driver	**CD4511B**	16
Multiplexers/Demultiplexers		
Analog/Digital		
Triple 2-channel	**CD4053B**	16
Differential 4-channel	**CD4052B**	16
Single 8-channel	**CD4051B**	16
Differential 8-channel	**CD4097B**	24
Single 16-channel	**CD4067B**	24
Quad bilateral switch	**CD4016B**	14
	CD4016A	14
Quad bilateral switch	**CD4066B**	14
	CD4066A	14
Quad AND/OR select	**CD4019B**	16
	CD4019A	16

Function	Type No.	No. of Pins
Multiplexers/Demultiplexers (cont'd)		
Analog/Digital (cont'd)		
Dual 1-of-4 decoder/demultiplexer (outputs high)	**CD4555B**	16
Dual 1-of-4 decoder/demultiplexer (outputs low)	**CD4556B**	16
Data Selector		
Quad 2-line-to-1-line	**CD40257B**	16
Phase Locked Loop		
Micropower	**CD4046B**	16
	CD4046A	16
Arithmetic Circuits		
Adders/Comparators		
4-bit full adder with parallel carry out	**CD4008B**	16
	CD4008A	16
Triple serial adder, positive logic	**CD4032B**	16
	CD4032A	16
Triple serial adder, negative logic	**CD4038B**	16
	CD4038A	16
4-bit magnitude comparator	**CD4063B**	16
Quad exclusive-OR gate	**CD4030B**	14
	CD4030A	14
Quad exclusive-OR gate	**CD4070B**	14
Quad exclusive-NOR gate	**CD4077B**	14
ALU/Rate Multipliers		
4-bit arithmetic logic unit	**CD40181B**	24
	CD4057A	28
BCD rate multiplier	**CD4527B**	16
Binary rate multiplier	**CD4089B**	16
Look-ahead-carry block	**CD40182B**	16
Parity Generator/Checker		
9-bit	**CD40101B**	14
Multiport Register		
4 X 4	**CD40108B**	24
4 X 4	**CD40208B**	24
Quad Bilateral Switches		
For transmission or multiplexing of analog or digital signals	**CD4016B**	14
	CD4016A	14
	CD4066B	14
	CD4066A	14

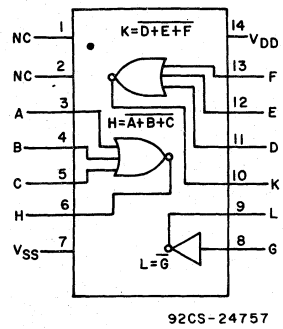
Function Selection Charts

COS/MOS TIMEKEEPING AND SPECIAL PRODUCTS

Function	Type No.	No. of Pins
Timekeeping		
Watches		
3½ Digit		
5-function LCD watch	**CD22001**	Chip
5 function LCD watch with manual reset	**CD22002**	Chip
5 function LCD watch with stopwatch	**CD22003**	Chip
2 function LCD watch	**CD22009**	Chip
2 function LCD watch (mirror image)	**CD22009R**	Chip
4 Digit		
6 function LCD watch	**CD22006**	Chip
6 function programmable LCD watch	**CD22007**	Chip
Stopwatch version	**CD22007V1**	Chip
Alarm version	**CD22007V2**	Chip
6 Digit		
6 function programmable LCD watch	**CD22008**	Chip
Stopwatch version	**CD22008V1**	Chip
Alarm version	**CD22008V2**	Chip
Clocks		
SOS stepping motor drive (2-Hz push-pull)	**CD22011**	8
Auto Clocks		
Quartz analog auto clock (0.5-Hz push-pull)	**CD22012**	14
Quartz analog auto clock (64-Hz push-pull)	**CD22013**	8
Quartz analog auto clock (60-Hz)	**CD22014**	8
Quartz analog auto clock (30-Hz push-pull)	**CD22015**	12
Industrial Timers		
Universal industrial timer	**CD22017**	16
Special Products		
Crosspoint Switches		
4 X 4 crosspoint switch with control memory	**CD22100**	16
4 X 4 X 2 crosspoint switch with control memory	**CD22101**	–
4 X 4 X 2 crosspoint switch with control memory	**CD22102**	–
Decoder/Drivers		
Counter and 7-segment decoder with multiplexer driver	**CD22925**	–
	CD22926	–
	CD22927	–
	CD22928	–

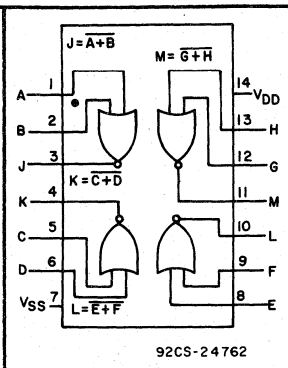
MICROPROCESSOR PRODUCTS

Function	Type No.	No. of Pins
CPU		
COSMAC 8-bit microprocessor	**CDP1802**	40
ROM		
512 X 8 mask-programmable	**CDP1831**	24
512 X 8 static mask-programmable	**CDP1832**	24
1024 X 8 mask-programmable	**CDP1833**	24
1024 X 8 static mask-programmable	**CDP1834**	24
RAM		
1024 X 1 static	**CDP1821S**	16
256 X 4 static	**CDP1822S**	22
128 X 8	**CDP1823S**	24
32 X 8 static	**CDP1824**	18
I/O		
8-bit I/O port	**CDP1852**	24
N-bit decoder	**CDP1853**	16
UART	**CDP1854**	40
4-bit memory bus buffer/separator	**CDP1856**	16
4-bit I/O bus buffer/separator	**CDP1857**	16
4-bit latch with 1 of 4 decoder	**CDP1858**	16
4-bit latch with dual 1 of 4 decoders	**CDP1859**	16
Video display controller	**CDP1861**	24



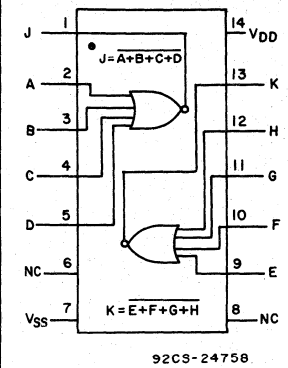
Dual 3-Input NOR Gate Plus Inverter

CD4000A	(File No. 944)
CD4000B	(File No. 985)
CD4000UB	(File No. 945)



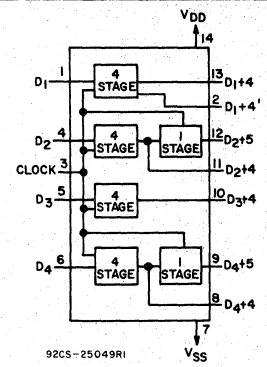
Quad 2-Input NOR Gate

CD4001A	(File No. 944)
CD4001B	(File No. 985)
CD4001UB	(File No. 945)



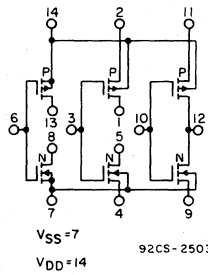
Quad 4-Input NOR Gate

CD4002A	(File No. 944)
CD4002B	(File No. 985)
CD4002UB	(File No. 945)



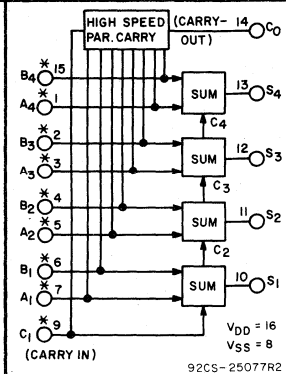
18-Stage Static Shift Register

CD4006A	(File No. 920)
CD4006B	(Prel.)



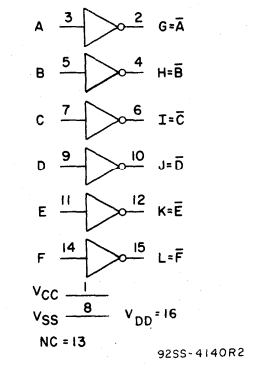
Dual Complementary Pair Plus Inverter

CD4007A	(File No. 921)
CD4007UB	(File No. 977)



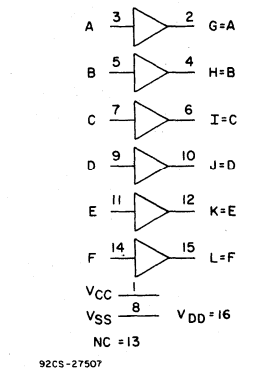
4-Bit Full Adder with Parallel Carry Out

CD4008A	(File No. 950)
CD4008B	(File No. 951)



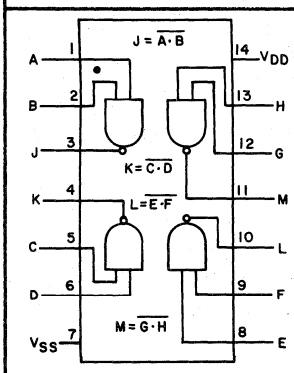
Hex Buffer/Converter Inverting Type

CD4009A	(File No. 939)
CD4009UB	(File No. 940)



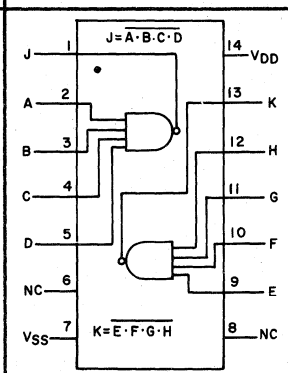
Hex Buffer/Converter Non-Inverting Type

CD4010A	(File No. 939)
CD4010B	(File No. 940)



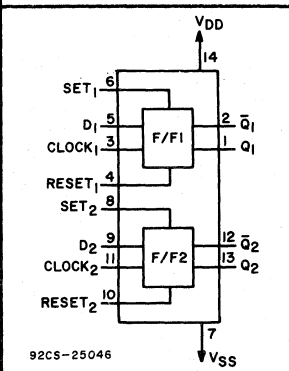
Quad 2-Input NAND Gate

CD4011A	(File No. 946)
CD4011B	(File No. 986)
CD4011UB	(File No. 947)



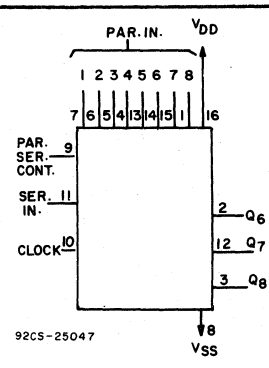
Dual 4-Input NAND Gate

CD4012A	(File No. 946)
CD4012B	(File No. 986)
CD4012UB	(File No. 947)



Dual "D" Flip-Flop with Set/Reset Capability

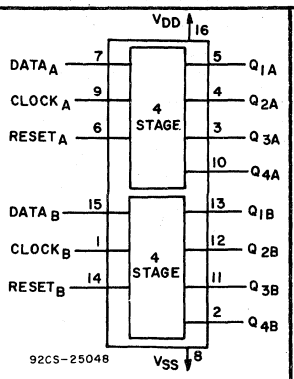
CD4013A	(File No. 935)
CD4013B	(File No. 936)



8-Stage Synchronous Shift Register with Parallel or Serial Input/Serial Output

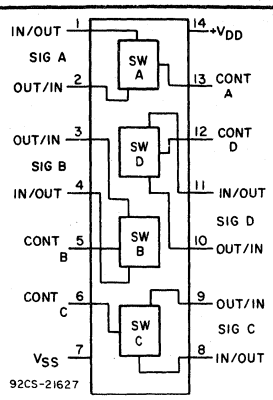
CD4014A	(File No. 922)
CD4014B	(Prel.)

Functional Diagrams



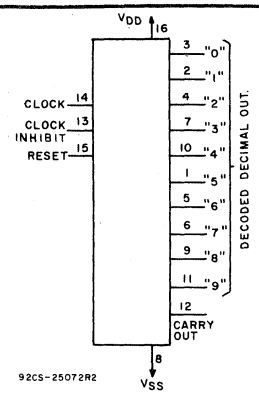
Dual 4-Stage Static Shift Register with Serial Input/ Parallel Output

CD4015A (File No. 943)
CD4015B (Prel.)



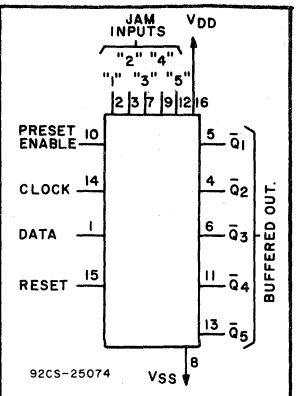
Quad Bilateral Switch

CD4016A (File No. 952)
CD4016B (File No. 953)



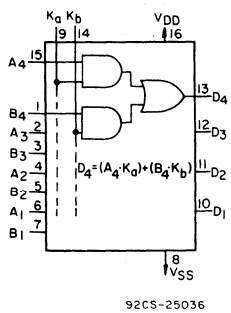
Decade Counter/Divider with 10 Decoded Decimal Outputs

CD4017A (File No. 927)
CD4017B (Prel.)



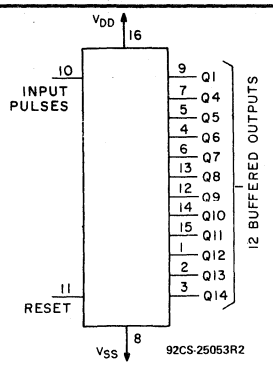
Presettable Divide-by-"N" Counter Fixed or Programmable

CD4018A (File No. 929)
CD4018B (Prel.)



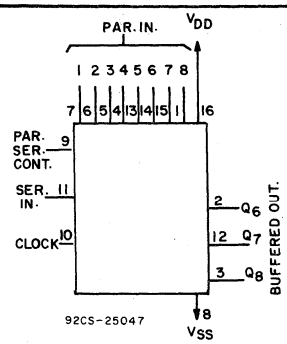
Quad AND/OR Select Gate

CD4019A (File No. 923)
CD4019B (Prel.)



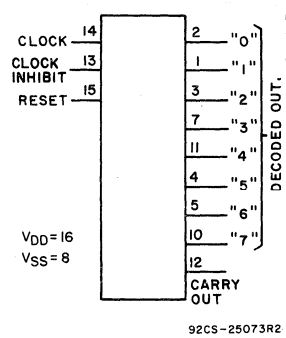
14-Stage Binary Ripple Counter

CD4020A (File No. 928)
CD4020B (Prel.)



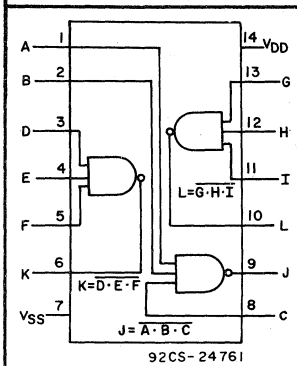
8-Stage Static Shift Register Asynchronous Parallel or Synchronous Serial Input/ Serial Output

CD4021A (File No. 933)
CD4021B (Prel.)



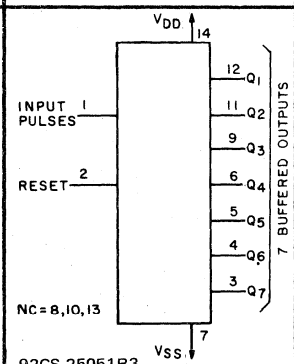
Divide-by-8 Counter/Divider with 8 Decoded Decimal Outputs

CD4022A (File No. 919)
CD4022B (Prel.)



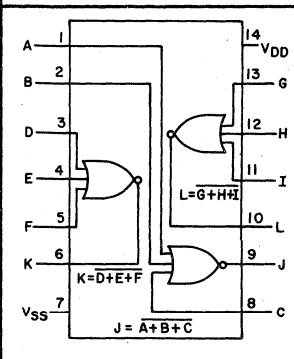
Triple 3-Input NAND Gate

CD4023A (File No. 946)
CD4023B (File No. 986)
CD4023UB (File No. 947)



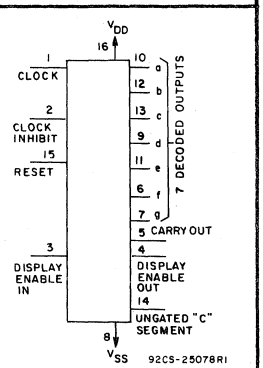
7-Stage Ripple-Carry Binary Counter/Divider

CD4024A (File No. 930)
CD4024B (Prel.)



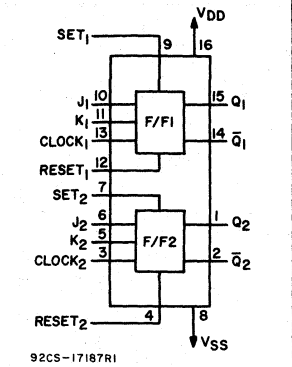
Triple 3-Input NOR Gate

CD4025A (File No. 944)
CD4025B (File No. 985)
CD4025UB (File No. 945)



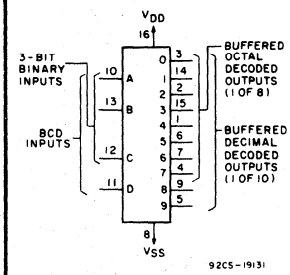
Decade Counter/Divider with 7-Segment Display Outputs and Display Enable

CD4026A (File No. 918)
CD4026B (Prel.)



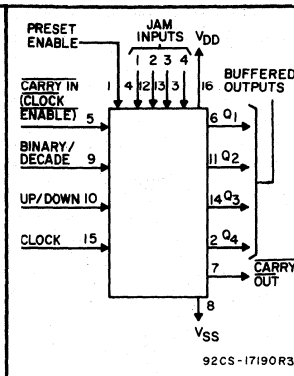
Dual J-K Master-Slave Flip-Flop with Set-Reset Capability

CD4027A (File No. 941)
CD4027B (File No. 942)



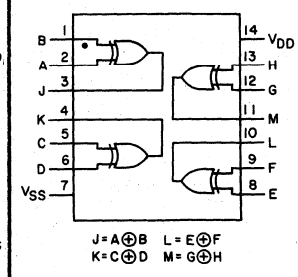
BCD-to-Decimal Decoder

CD4028A (File No. 937)
CD4028B (File No. 1016)



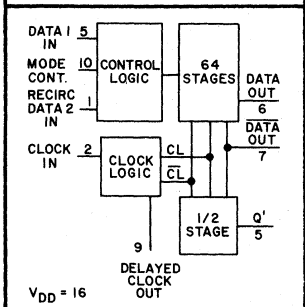
Presettable Up/Down Counter, Binary or BCD-Decade

CD4029A (File No. 931)
CD4029B (Prel.)



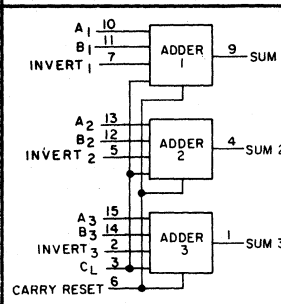
Quad Exclusive-OR Gate

CD4030A (File No. 932)
CD4030B (Prel.)



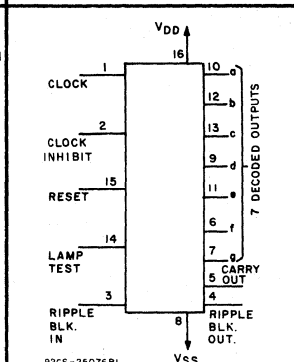
64-Stage Static Shift Register

CD4031A (File No. 569)
CD4031B (Prel.)



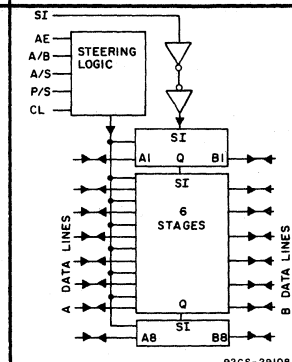
Triple Serial Adder Positive Logic

CD4032A (File No. 915)
CD4032B (Prel.)



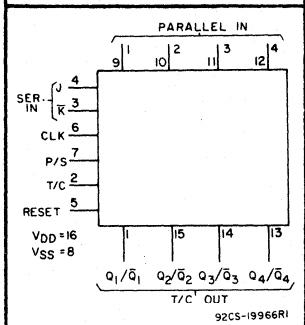
Decade Counter/Divider with 7-Segment Display Outputs and Ripple Blanking

CD4033A (File No. 918)
CD4033B (Prel.)



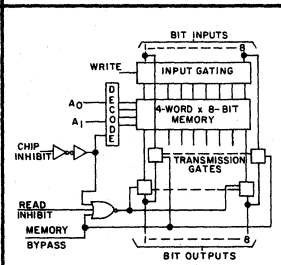
8-Stage Static Bidirectional Parallel/Serial Input/Output Bus Register

CD4034A (File No. 575)
CD4034B (Prel.)



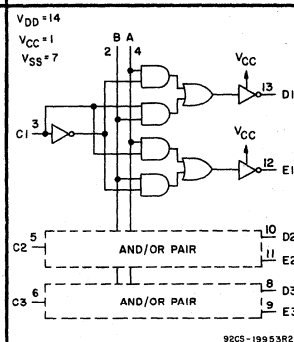
4-Stage Parallel In/Parallel Out Shift Register with J-K Serial Inputs and True/ Complement Outputs

CD4035A (File No. 568)
CD4035B (Prel.)



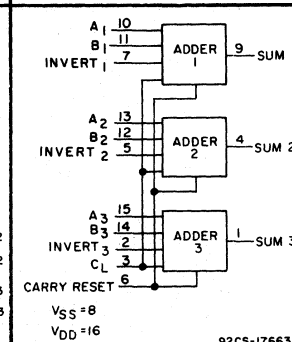
4-Word by 8-Bit Random Access NDRO Memory Binary Addressing

CD4036A (File No. 613)



Triple AND/OR Bi-Phase Pair

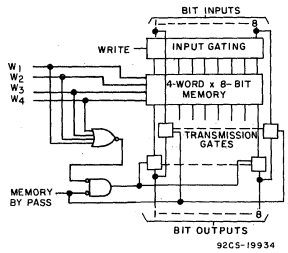
CD4037A (File No. 576)



Triple Serial Adder Negative Logic

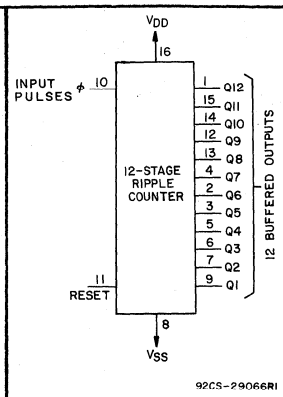
CD4038A (File No. 915)
CD4038B (Prel.)

Functional Diagrams



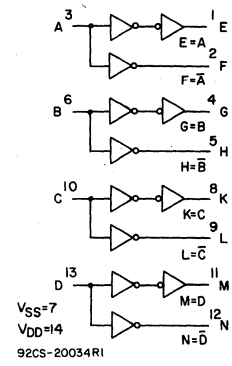
4-Word by 8-Bit Random Access NDRO Memory Direct Word-Line Addressing

CD4039A (File No. 613)



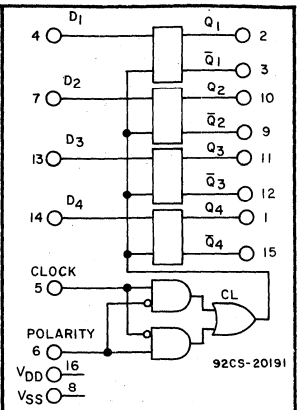
12-Stage Ripple-Carry Binary Counter/Divider

CD4040A (File No. 624)
CD4040B (Prel.)



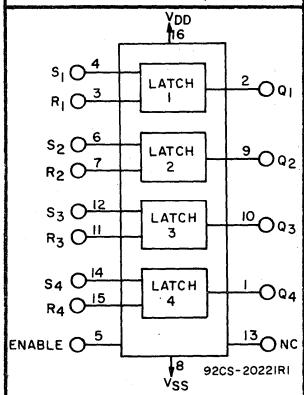
Quad True/Complement Buffer

CD4041A (File No. 572)
CD4041UB (File No. 934)



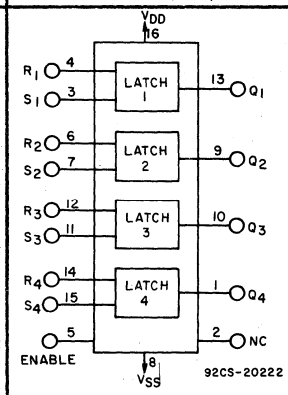
Quad Clocked "D" Latch

CD4042A (File No. 589)
CD4042B (File No. 954)



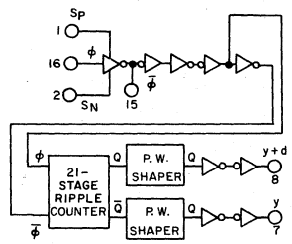
Quad 3-State NOR R/S Latch

CD4043A (File No. 590)
CD4043B (File No. 954)



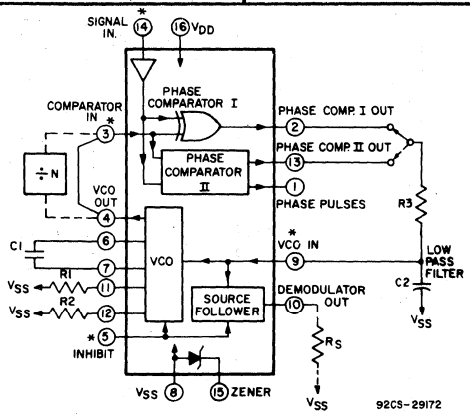
Quad 3-State NAND R/S Latch

CD4044A (File No. 590)
CD4044B (File No. 956)



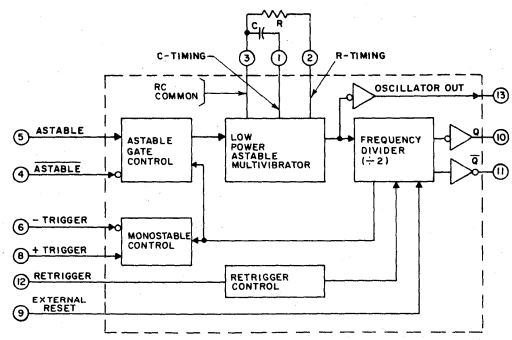
21-Stage Counter

CD4045A (File No. 614)
CD4045B (Prel.)



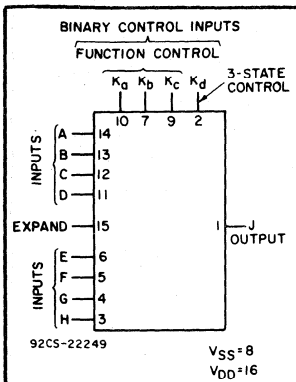
Micropower Phase-Locked Loop

CD4046A (File No. 637)
CD4046B (Prel.)



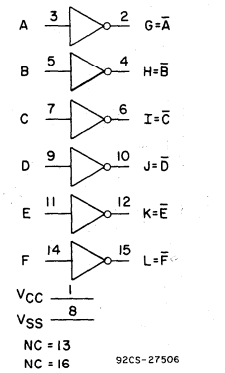
Low-Power Monostable/Astable Multivibrator

CD4047A (File No. 623)
CD4047B (Prel.)



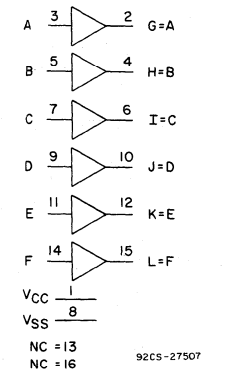
Multi-Function Expandable 8-Input Gate

CD4048A (File No. 636)
CD4048B (Prel.)



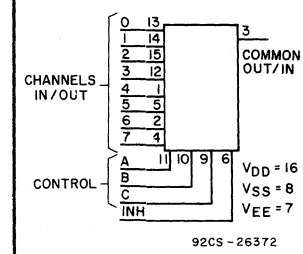
Hex Buffer/Converter Inverting Type

CD4049A (File No. 599)
CD4049UB (File No. 926)



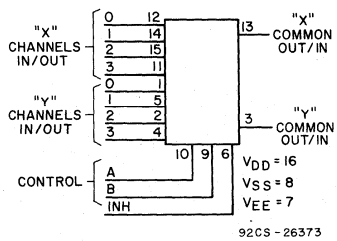
Hex Buffer/Converter Non-Inverting Type

CD4050A (File No. 599)
CD4050B (File No. 926)



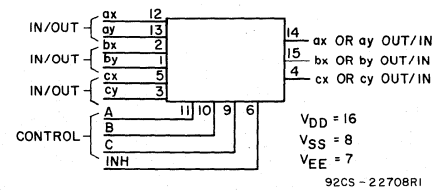
Single 8-Channel Analog Multiplexer/Demultiplexer

CD4051B (File No. 902)



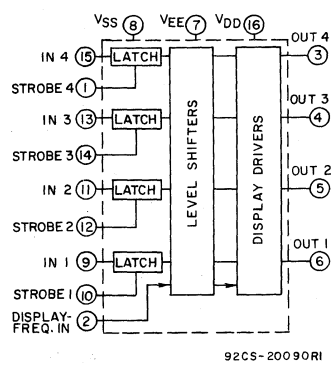
Differential 4-Channel Analog Multiplexer/Demultiplexer

CD4052B (File No. 902)



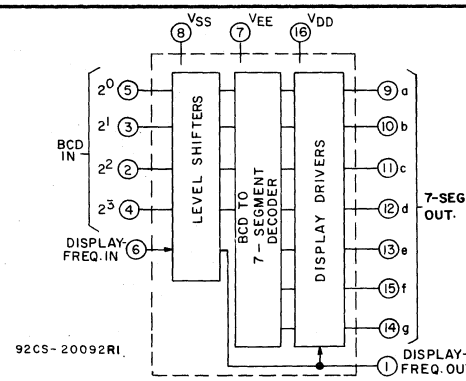
Triple 2-Channel Multiplexer/Demultiplexer

CD4053B (File No. 902)



4-Segment Liquid-Crystal Display Driver

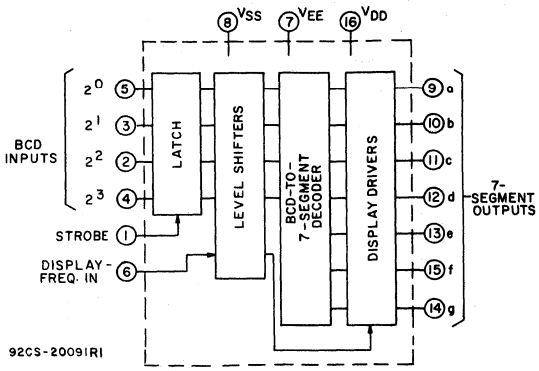
CD4054B (File No. 634)



BCD-to-7-Segment Decoder/Driver with "Display-Frequency" Output Liquid-Crystal Display Driver

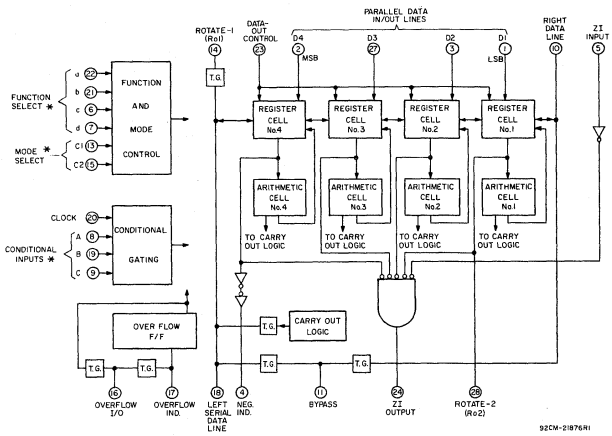
CD4055B (File No. 634)

Functional Diagrams



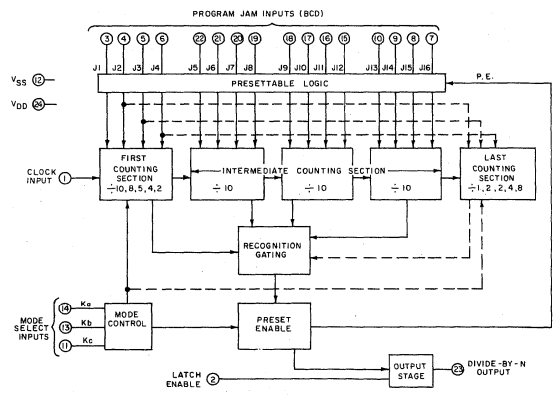
BCD-to-7-Segment Decoder/Driver with Strobed-Latch Function Liquid-Crystal Display Driver

CD4056B (File No. 634)



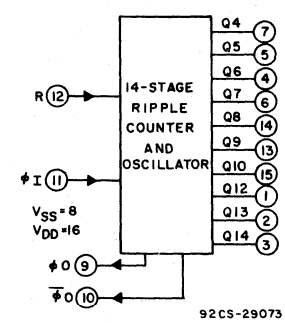
4-Bit Arithmetic Logic Unit

CD4057A (File No. 635)



Programmable Divide-by-"N" Counter

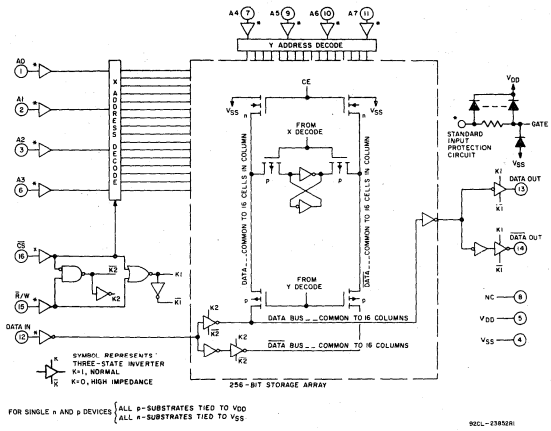
CD4059A (File No. 898)



14-Stage Ripple-Carry Binary Counter/Divider and Oscillator

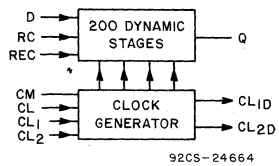
CD4060A (File No. 813)
CD4060B (Prel.)

Functional Diagrams



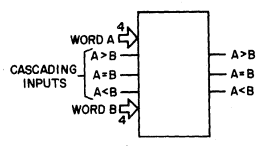
256-Word by 1-Bit Static Random-Access Memory

CD4061A (File No. 768)



200-Stage Dynamic Shift Register

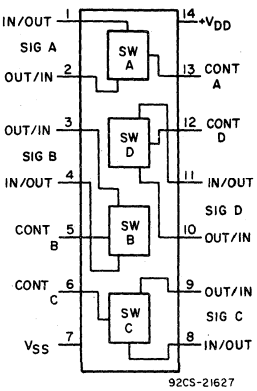
CD4062A (File No. 816)



CD4063B FUNCTIONAL DIAGRAM

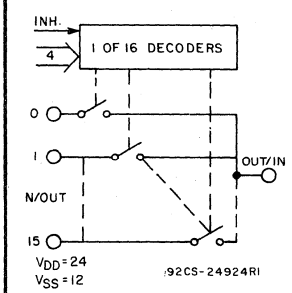
4-Bit Magnitude Comparator

CD4063B (File No. 805)



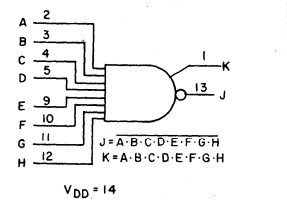
Quad Bilateral Switch

CD4066A (File No. 769)
CD4066B (Prel.)



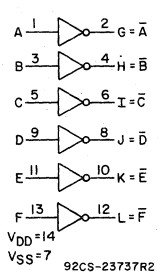
16-Channel Multiplexer/Demultiplexer

CD4067B (File No. 909)



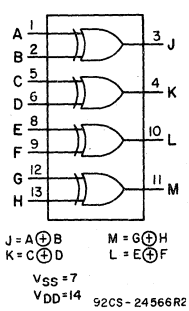
8-Input NAND/AND Gate

CD4068B (File No. 809)



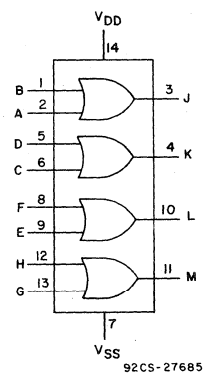
Hex Inverter

CD4069UB (File No. 804)



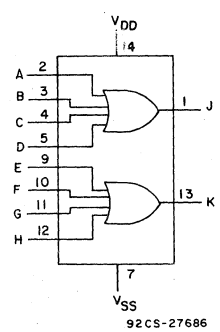
Quad Exclusive-OR Gate

CD4070B (File No. 910)



Quad 2-Input OR Gate

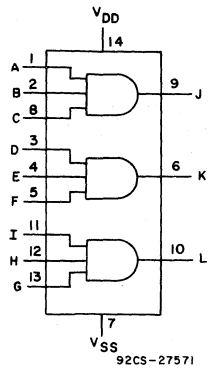
CD4071B (File No. 807)



Dual 4-Input OR Gate

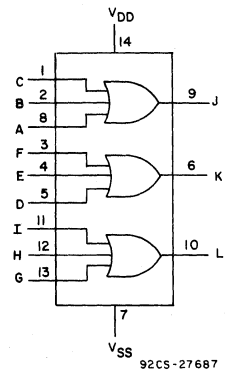
CD4072B (File No. 807)

Functional Diagrams



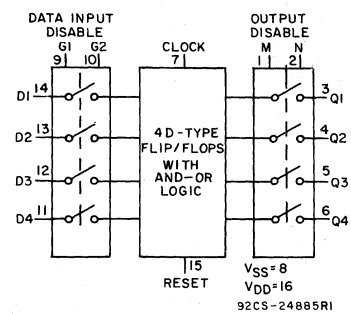
Triple 3-Input AND Gate

CD4073B (File No. 806)



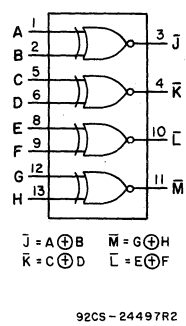
Triple 3-Input OR Gate

CD4075B (File No. 807)



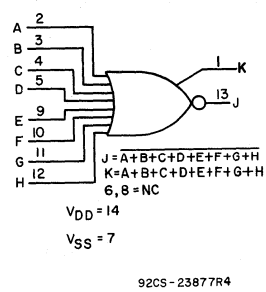
4-Bit D-Type Register

CD4076B (File No. 903)



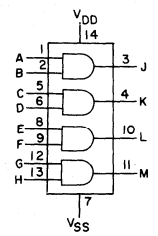
Quad Exclusive-NOR Gate

CD4077B (File No. 910)



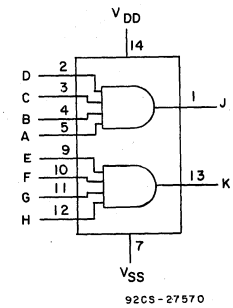
8-Input NOR/OR Gate

CD4078B (File No. 810)



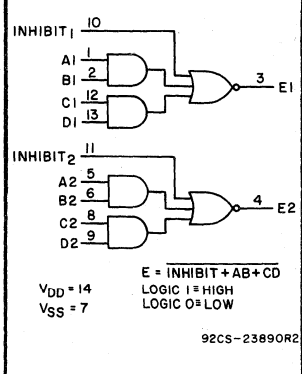
Quad 2-Input AND Gate

CD4081B (File No. 806)



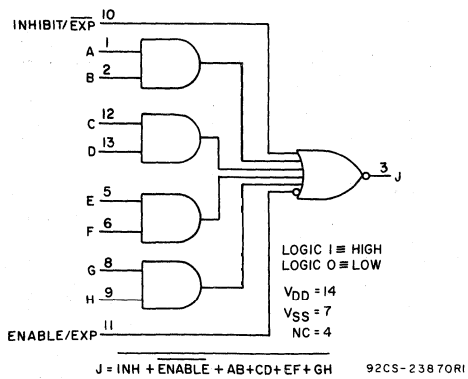
Dual 4-Input AND Gate

CD4082B (File No. 806)



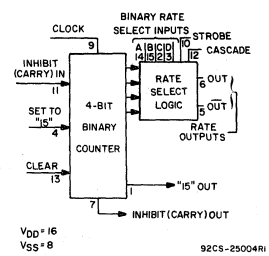
Dual 2-Wide, 2-Input AND-OR-INVERT (AOI) Gate

CD4085B (File No. 811)



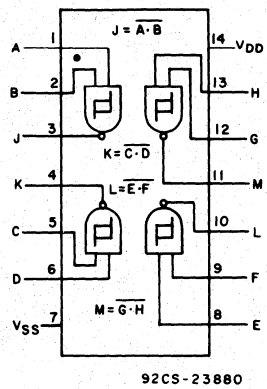
Expandable 4-Wide, 2-Input AND-OR-INVERT (AOI) Gate

CD4086B (File No. 812)



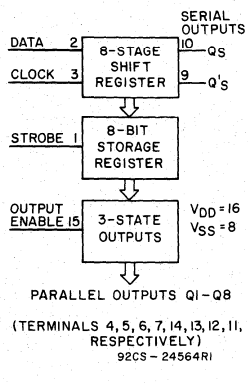
Binary Rate Multiplier

CD4089B (File No. 1003)



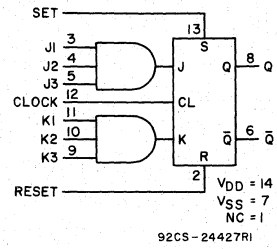
Quad 2-Input NAND Schmitt Trigger

CD4093B (File No. 836)



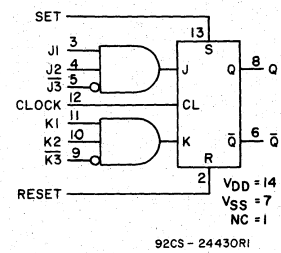
8-Stage Shift-and-Store Bus Register

CD4094B (File No. 869)



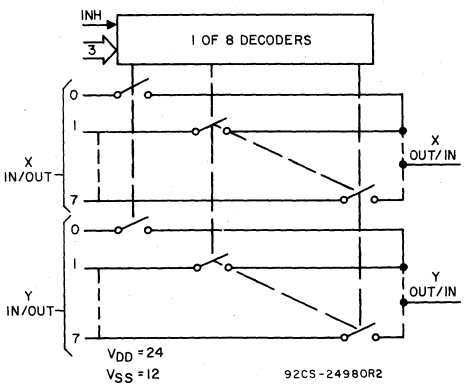
Gated J-K Master-Slave Flip-Flop, Non-Inverting Inputs

CD4095B (File No. 879)



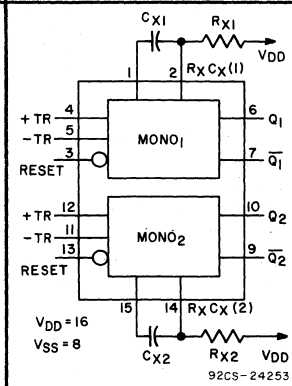
Gated J-K Master-Slave Flip-Flop, Inverting and Non-Inverting Inputs

CD4096B (File No. 879)



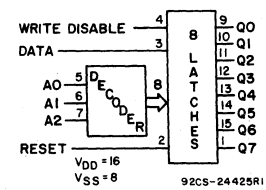
Differential 8-Channel Multiplexer/Demultiplexer

CD4097B (File No. 909)



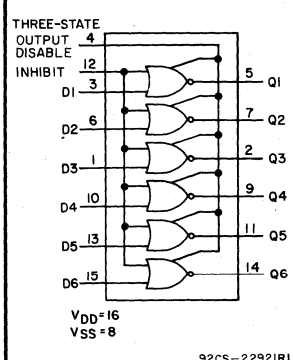
Dual Monostable Multivibrator

CD4098B (File No. 979)



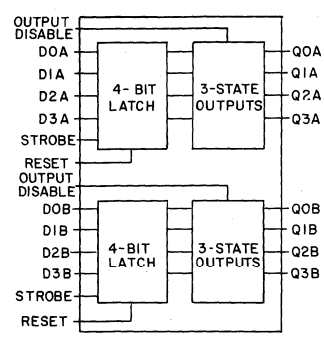
8-Bit Addressable Latch

CD4099B (File No. 948)



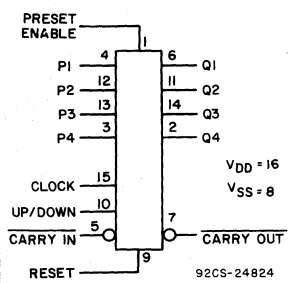
Strobed Hex Inverter/Buffer

CD4502B (File No. 1002)



Dual 4-Bit Latch

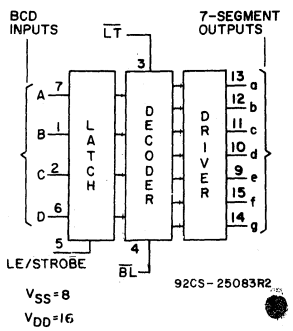
CD4508B (File No. 1009)



BCD Presettable Up/Down Counter

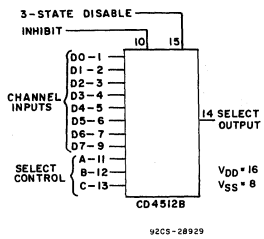
CD4510B (File No. 899)

Functional Diagrams



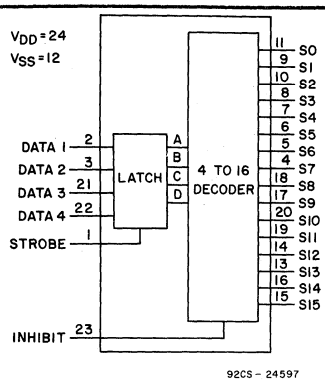
BCD-to-7-Segment Latch Decoder Driver

CD4511 (File No. 901)



8-Channel Data Selector

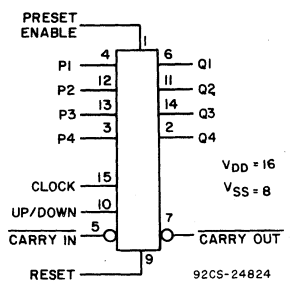
CD4512B (Prel.)



4-Bit Latch/4-to-16 Line Decoder

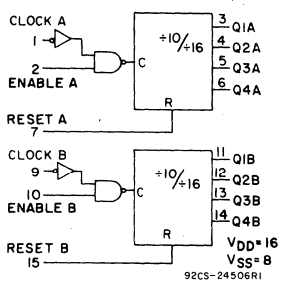
CD4514B (File No. 814) Output "High" on Select

CD4515B (File No. 814) Output "Low" on Select



Binary Presettable Up/Down Counter

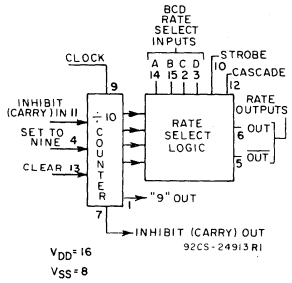
CD4516B (File No. 899)



Dual Up Counter

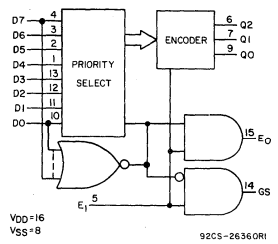
CD4518B (File No. 808) BCD

CD4520B (File No. 808) Binary



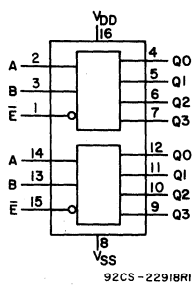
BCD Rate Multiplier

CD4527B (File No. 1006)



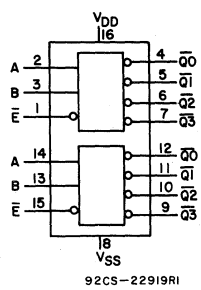
8-Bit Priority Encoder

CD4532B (File No. 876)



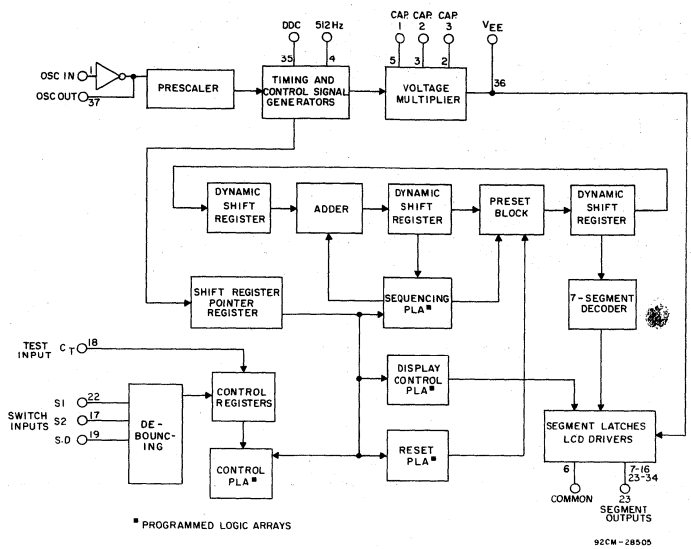
Dual Binary-to-1-of-4 Decoder/Demultiplexer Output "High" on Select

CD4555B (File No. 858)



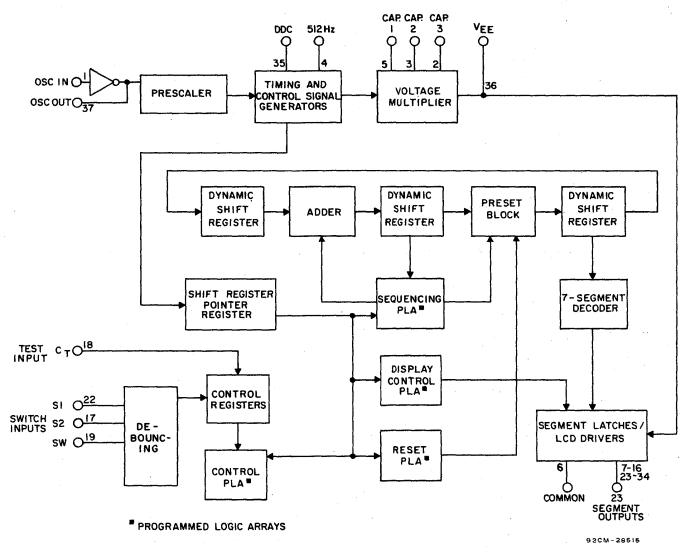
Dual Binary-to-1-of-4 Decoder/Demultiplexer Output "Low" on Select

CD4556B (File No. 858)



5-Function Liquid-Crystal Digital Watch Circuit

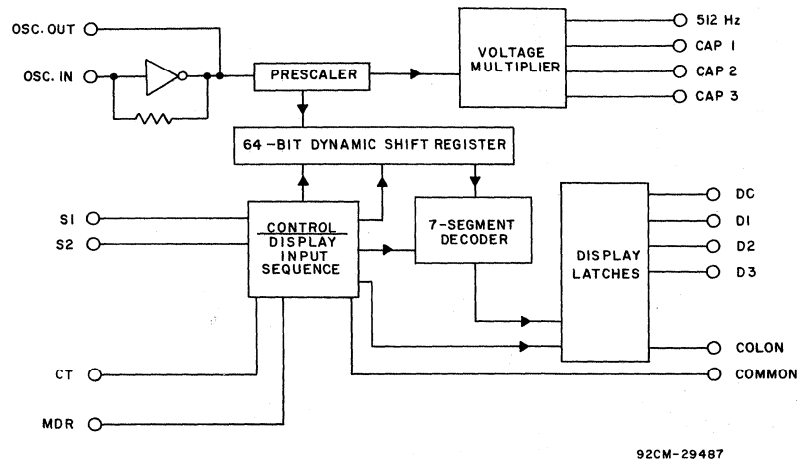
CD22001H (File No. 971)
CD22002H (File No. 971)
Automatic and Manual Reset



6-Function Liquid-Crystal Digital-Watch Circuit with Stopwatch

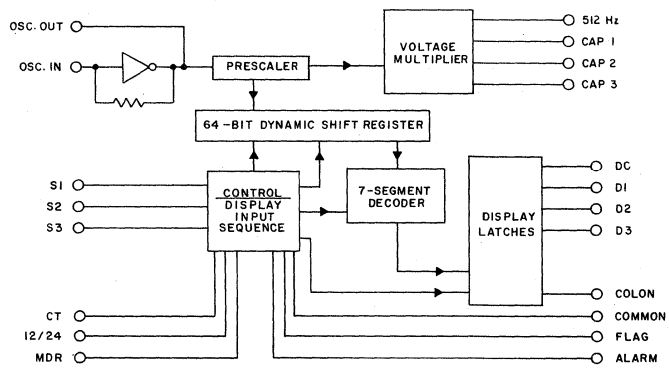
CD22003H (File No. 972)
Automatic and Manual Reset
Automatic Shutdown for Power Conservation

Functional Diagrams



6-Function Liquid-Crystal Digital-Watch Circuit

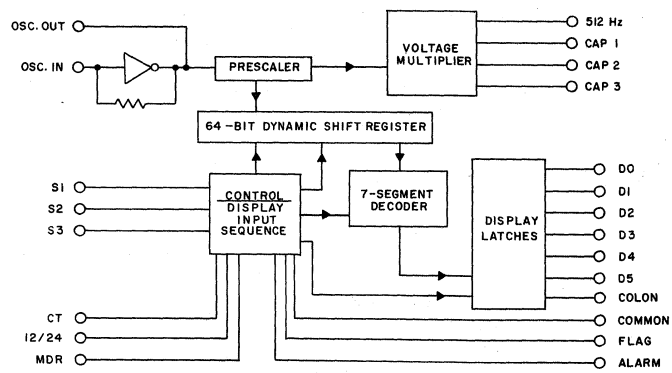
CD22006H (Objec.)
4-Year Calendar
Automatic Shutdown



NOTE:
ALARM OUTPUT NOT INCLUDED ON CD22007VIH AND CD22007H; FLAG OUTPUT AND S3 INPUT NOT INCLUDED ON CD22007H

6-Function Liquid-Crystal Digital-Watch Circuit

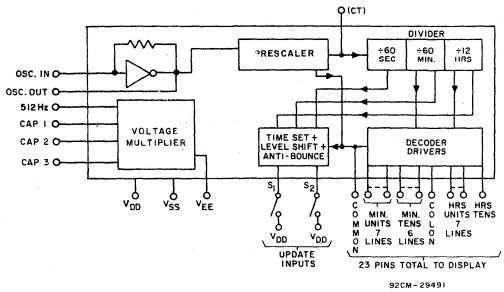
CD22007H (Objec.)
CD22007VIH (Objec.)
With Stopwatch
CD22007V2H (Objec.)
With 24-Hour Alarm



NOTE:
ALARM OUTPUT NOT INCLUDED ON CD22008VIH AND CD22008H; FLAG OUTPUT AND S3 INPUT NOT INCLUDED ON CD22008H.

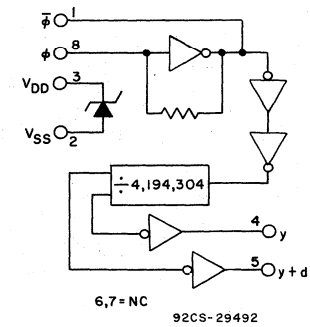
6-Function Liquid-Crystal Digital-Watch Circuit

CD22008H (Objec.)
CD22008VIH (Objec.)
With Stopwatch
CD22008V2H (Objec.)
With 24-Hour Alarm



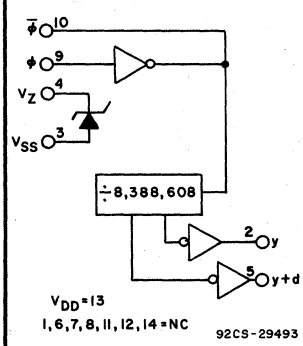
2-Function Liquid-Crystal Digital-Watch Circuit

CD22009H (Objec.)
CD22009RH (Objec.)
Mirror-Image of CD22009H



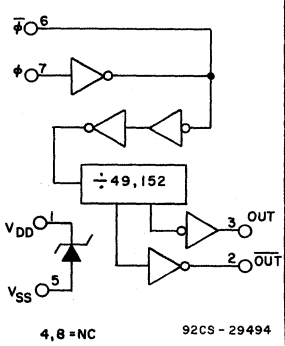
Quartz Analog Clock Circuit

CD22011E (Objec.)



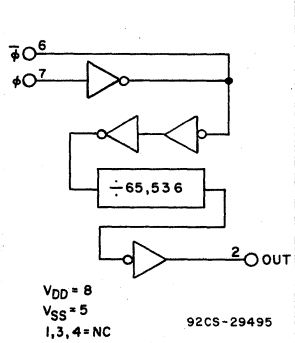
Quartz Analog Clock Circuit

CD22012E (Objec.)



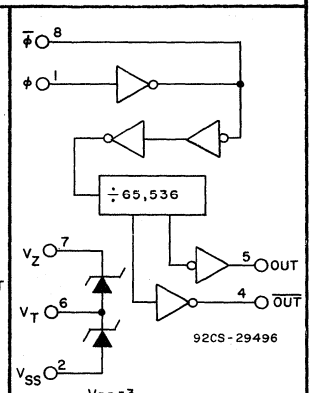
Quartz Analog Clock Circuit

CD22013E (Objec.)



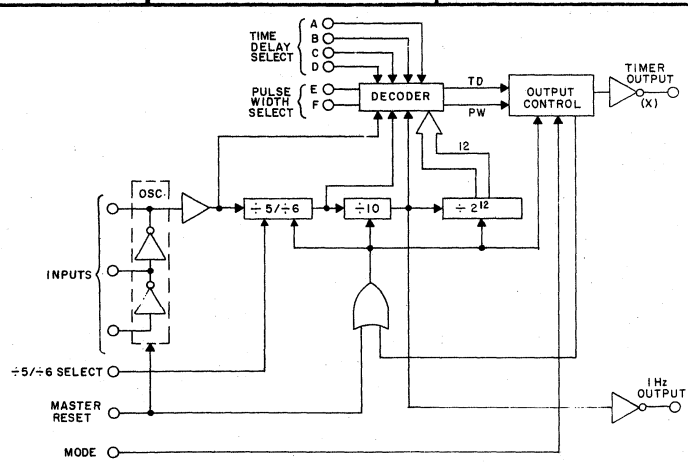
Quartz Analog Clock Circuit

CD22014E (Objec.)



Quartz Analog Clock Circuit

CD22015E (Objec.)

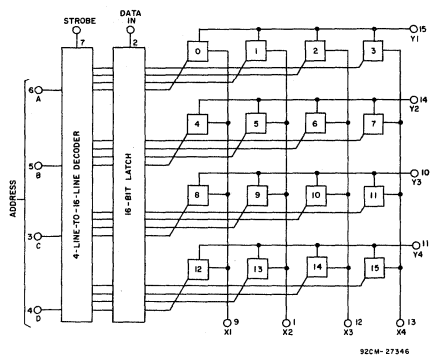


M = "0" (SINGLE TRANSITION)
M = "1" (SINGLE PULSE)
M = (X) (RECYCLE)

Industrial Timer Circuit

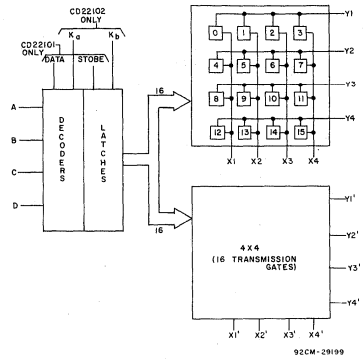
CD22017E (Objec.)

Functional Diagrams



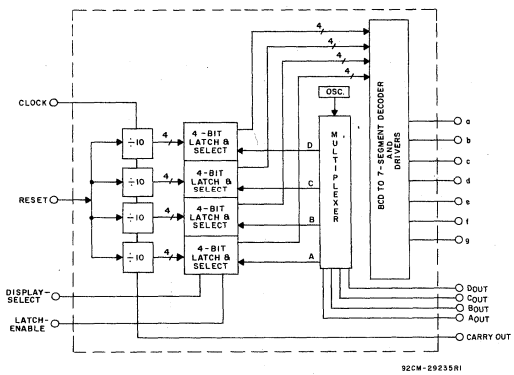
4-by-4 Crosspoint Switch with Control Memory

CD22100 (Prel.)



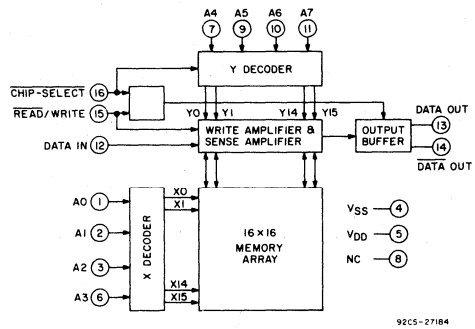
4-by-4-by-2 Crosspoint Switch with Control Memory

CD22101 (Objec.)
CD22102 (Objec.)



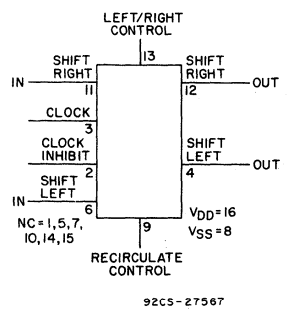
Counter and 7-Segment Decoder with Multiplexer Driver

CD22925 (Objec.) CD22927 (Objec.)
CD22926 (Objec.) CD22928 (Objec.)



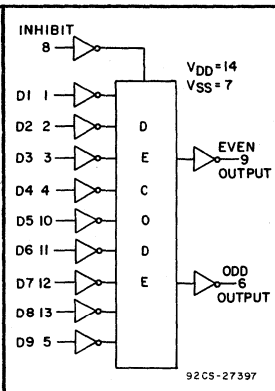
256-Word by 1-Bit Static Random-Access Memory

CD40061 (Prel.)
CD40061A (Prel.)



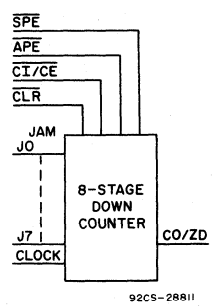
32-Stage Static Left/Right Shift Register

CD40100B (File No. 980)



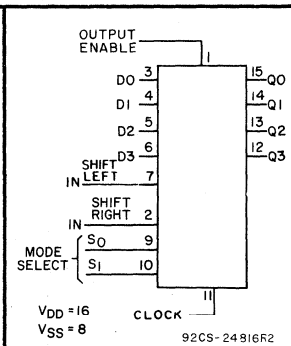
9-Bit Parity Generator/Checker

CD40101B (File No. 1000)



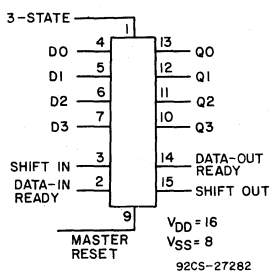
8-Stage Presettable Synchronous Down Counter

CD40102B (File No. 984)
2-Decade BCD
CD40103B (File No. 984)
8-Bit Binary



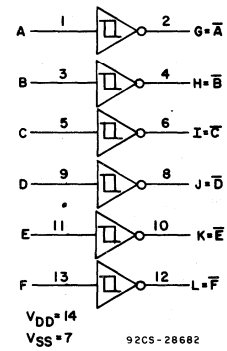
4-Bit Bidirectional Universal Register

CD40104B (Prel.)



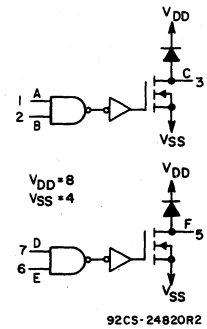
FIFO Register
4-Bits Wide by 16-Bits Long

CD40105B (Prel.)



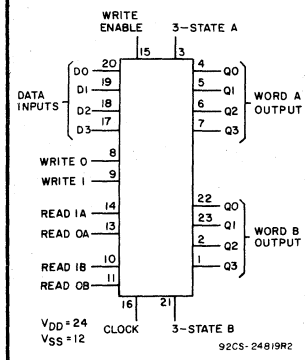
Hex Schmitt Trigger

CD40106B (File No. 1017)



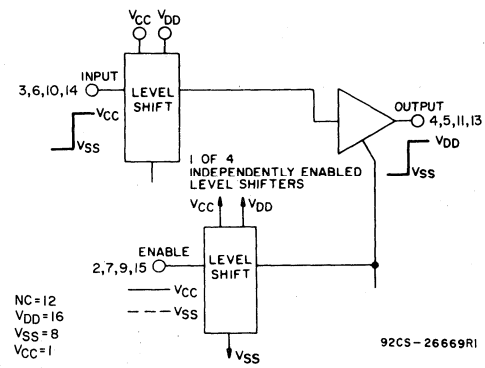
Dual 2-Input NAND
Buffer/Driver

CD40107B (File No. 1015)



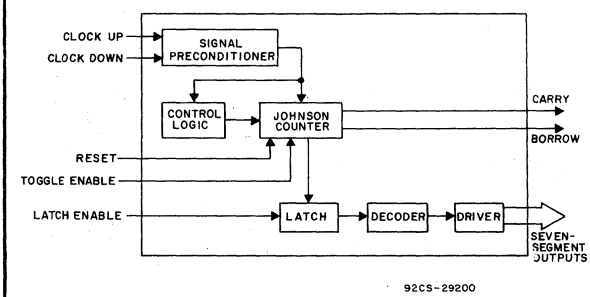
4-by-4 Multiport Register

CD40108B (File No. 1011)



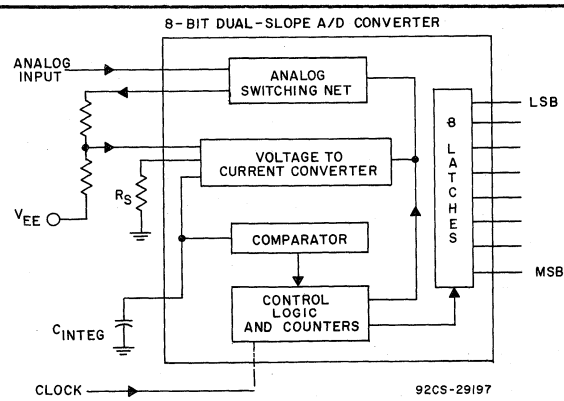
Quad Low-to-High
Voltage Level Shifter

CD40109B (File No. 1018)



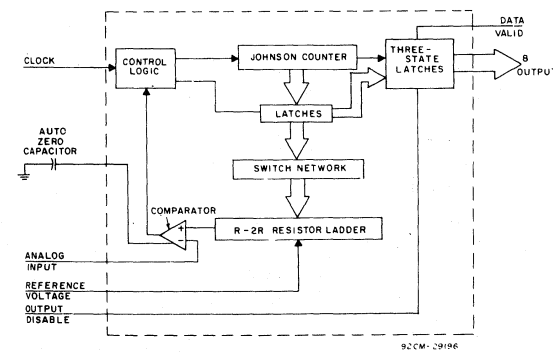
Decade Up-Down Counter/
Decoder/Latch/Driver

CD40110B (Objec.)



8-Bit Dual Slope
A/D Converter

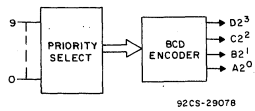
CD40112B (Objec.)



Successive Approximation
8-Bit A/D Converter

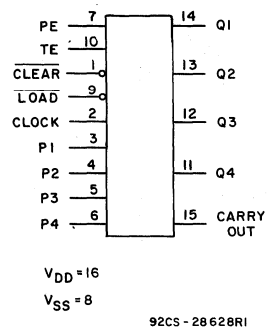
CD40113B (Objec.)

Functional Diagrams



10-Line-to-4-Line BCD Priority Encoder

CD40147B (Objec.)



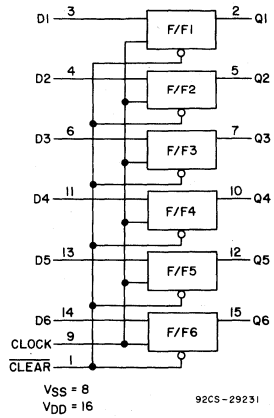
Synchronous 4-Bit Counter

CD40160B (Prel.) Decade with Asynchronous Clear

CD40161B (Prel.) Binary with Asynchronous Clear

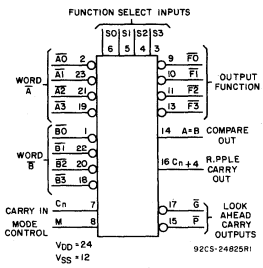
CD40162B (Prel.) Decade with Synchronous Clear

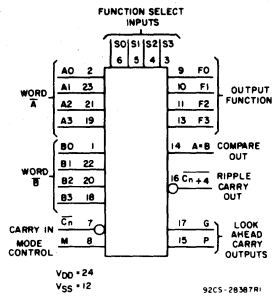
CD40163B (Prel.) Binary with Synchronous Clear



Hex "D" Type Flip-Flop

CD40174B (Prel.)

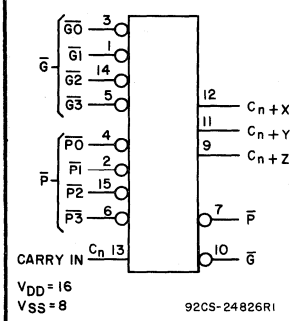




4-Bit Arithmetic Logic Unit

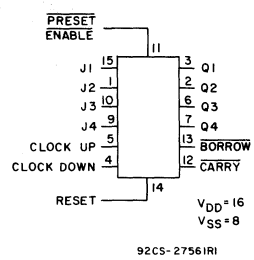
Active-Low Data **Active-High Data**

CD40181B (Prel.)



Look-Ahead Carry Generator

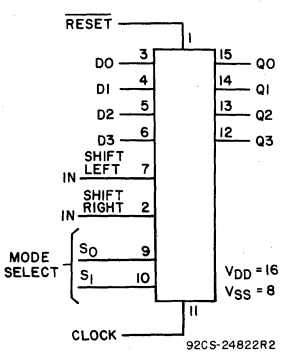
CD40182B (File No. 1008)



Presettable Up/Down Counter (Dual Clock with Reset)

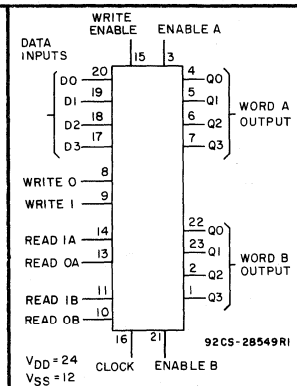
CD40192B (File No. 993) BCD

CD40193B (File No. 993) Binary



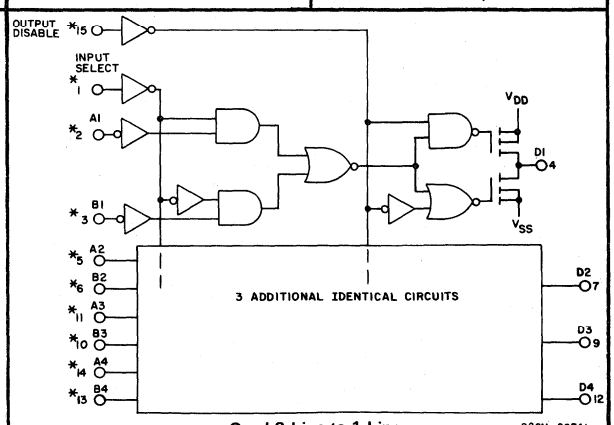
4-Bit Bidirectional Universal Shift Register

CD40194B (Prel.)



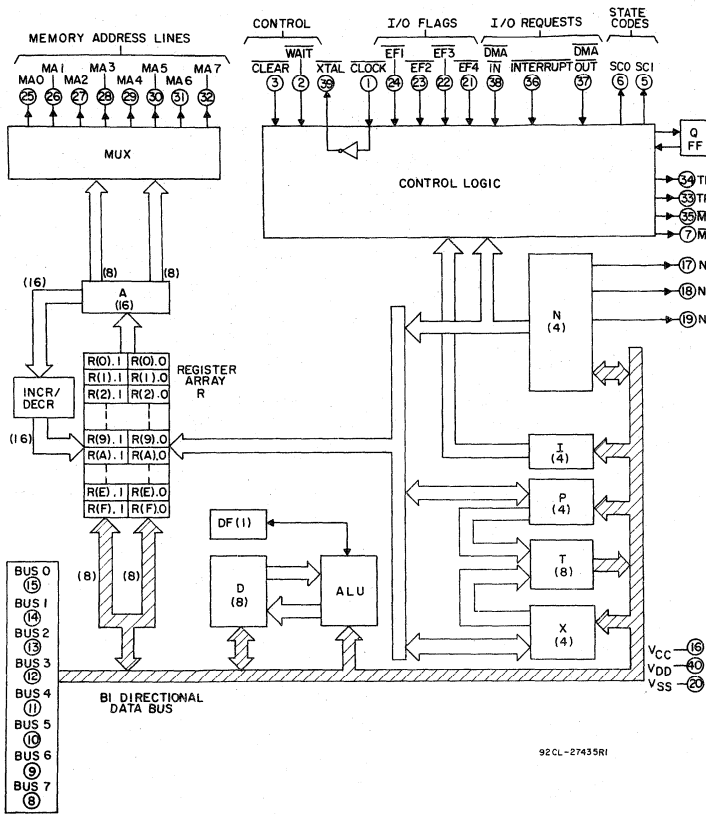
4-by-4 Multiport Register

CD40208B (File No. 1007)



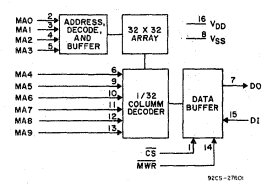
Quad 2-Line-to-1-Line Data Selector/Multiplexer

CD40257B (File No. 982)



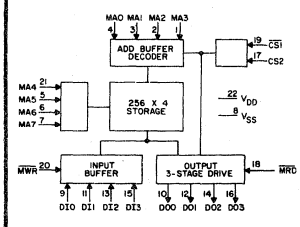
8-Bit Registered-Oriented Central Processing Unit

CDP1802C (Prel.)
CDP1802CD (Prel.)



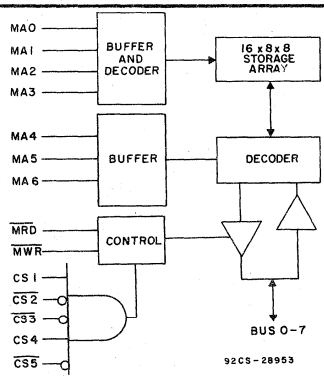
1024-Word by 1-Bit Static Random-Access Memory

CDP1821SD (Prel.)
CDP1821SCD (Prel.)



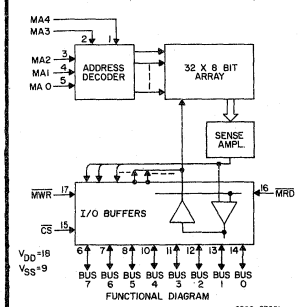
256-Word by 4-Bit Static Random-Access Memory

CDP1822SD (Prel.)
CDP1822SCD (Prel.)



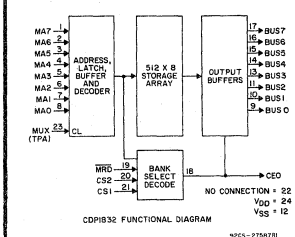
128-Word by 8-Bit Static Random-Access Memory

CDP1823SD (Prel.)
CDP1823SCD (Prel.)



32-Word by 8-Bit Static Random-Access Memory

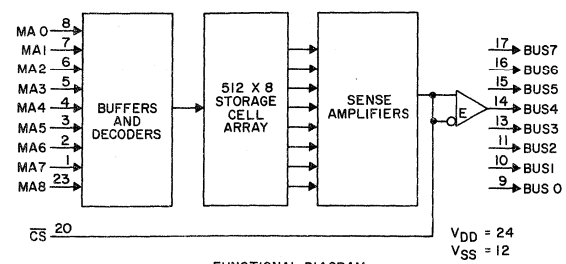
CDP1824D (Prel.)
CDP1824CD (Prel.)



512-Word by 8-Bit Static Read-Only Memory

CDP1831D (Prel.)
CDP1831CD (Prel.)

Functional Diagrams

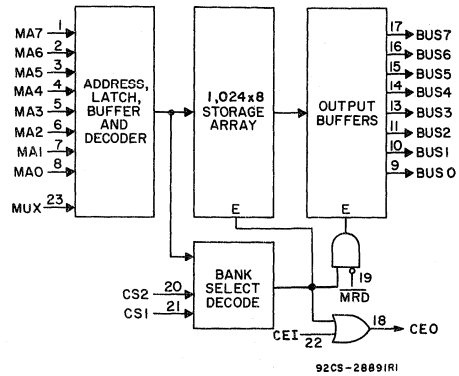


FUNCTIONAL DIAGRAM

92CS-27581

512-Word by 8-Bit Static Read-Only Memory

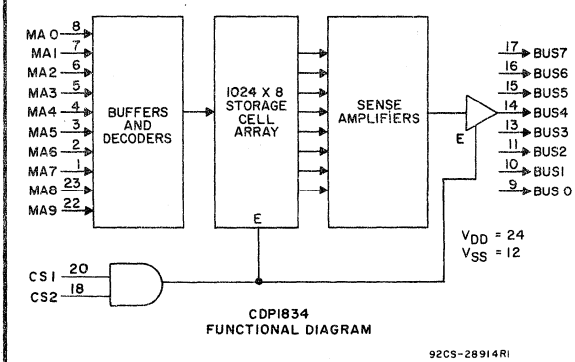
CDP1832D (Prel.)
CDP1832CD (Prel.)



92CS-28891RI

1024-Word by 8-Bit Static Read-Only Memory

CDP1833C (Prel.)
CDP1833CD (Prel.)

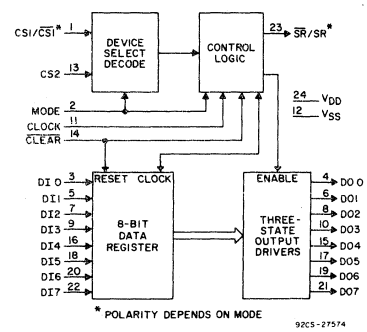


CDP1834
FUNCTIONAL DIAGRAM

92CS-28914RI

1024-Word by 8-Bit Static Read-Only Memory

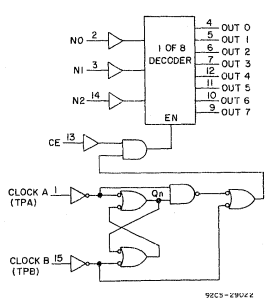
CDP1834D (Prel.)
CDP1834CD (Prel.)



92CS-27574

8-Bit Input/Output Port

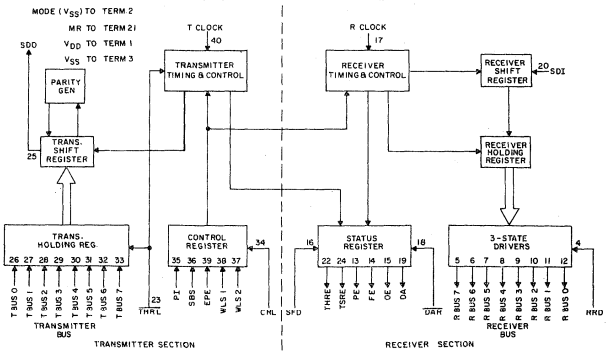
CDP1852D (Prel.)
CDP1852CD (Prel.)



92CS-28024

N-Bit 1 of 8 Decoder

CDP1853D (Prel.)
CDP1853CD (Prel.)

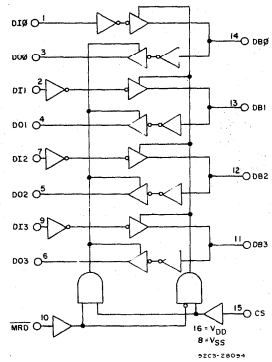


92CL-28458

Universal Asynchronous Receiver/ Transmitter (UART) (Standard Mode 0 Shown)

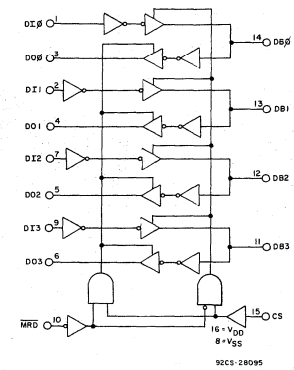
CDP1854C (Prel.)
CDP1854CD (Prel.)

Functional Diagrams



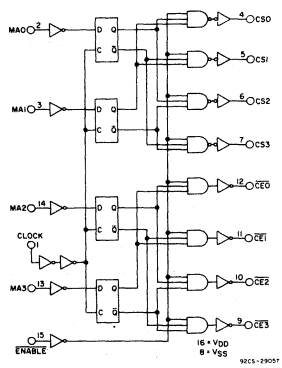
4-Bit Bus Buffer/Separator

CDP1856D (Prel.)
CDP1856CD (Prel.)



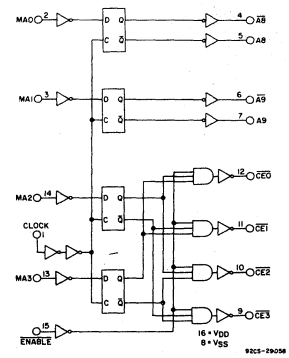
4-Bit Bus Buffer/Separator

CDP1857D (Prel.)
CDP1857CD (Prel.)



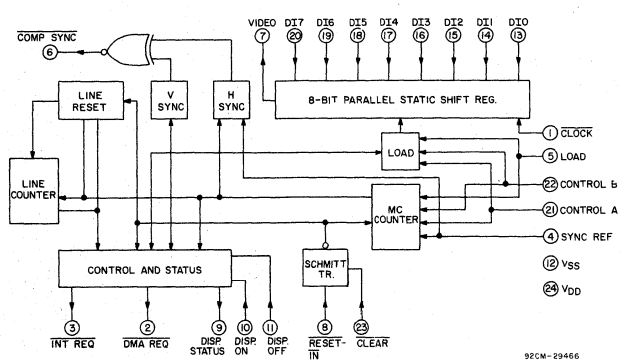
4-Bit Latch with Decode

CDP1858C (Prel.)
CDP1858CD (Prel.)



4-Bit Latch with Decode

CDP1859D (Prel.)
CDP1859CD (Prel.)

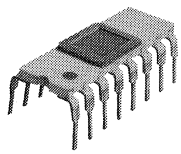


Video Display Controller

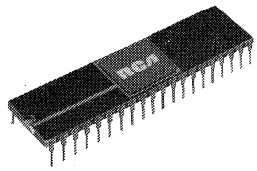
CDP1861CD (Prel.)

COS/MOS IC Packages

D Suffix
Ceramic Dual-in-Line Packages

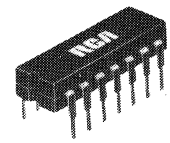


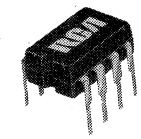
Welded-Seal
14, 16, 24,
and 28-lead
versions



Side-Brazed
14,16,18,22,24,
28, and 40-lead
versions

E Suffix
Plastic Dual-in-Line Packages

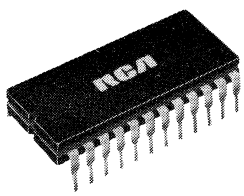




MiniDIP

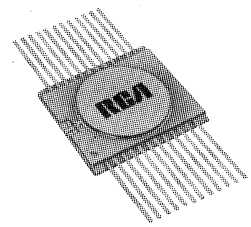
8, 14, 16, and 24-lead versions

F Suffix
Frit-Seal Ceramic Dual-in-Line Packages



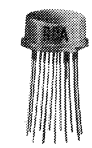
14, 16, and 24-lead versions

K Suffix
Ceramic Flat Packages



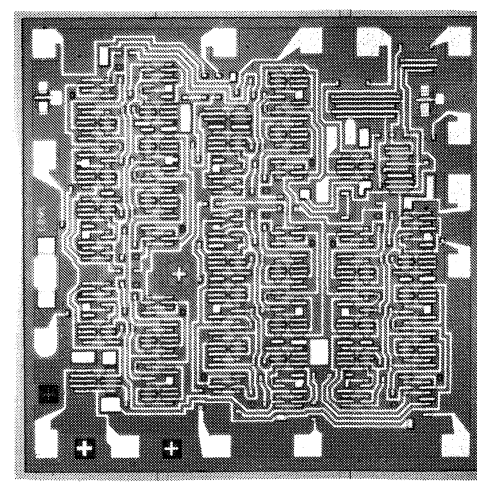
14, 16, and 24-lead versions

T Suffix
12-Lead TO-5 Style Package



CD4062A only

H Suffix
COS/MOS Chip



Ordering Information

Most RCA COS/MOS integrated circuits are available in the following package styles and are identified by the Suffix Letters indicated below: dual-in-line ceramic, dual-in-line frit-seal ceramic, dual-in-line plastic, ceramic flat package, and in chip form. Some types are only available in one or two package styles. The available package styles for any specific type are given in the technical data for that type.

When ordering COS/MOS devices, it is important that the appropriate suffix letter be affixed to the type number of the device required. For example, a CD4016B in a dual-in-line ceramic package will be identified as the CD4016BD.

Package	Suffix Letters
Dual-in-Line Ceramic	D
Dual-in-Line Frit-Seal Ceramic	F
Dual-in-Line Plastic	E
Ceramic Flat Package	K
TO-5 Style (CD4062A only)	T
Chip	H

General Operating and Application Considerations

General Operating and Application Considerations

This section is intended as a guide to circuit and equipment designers in the operation and application of MOS integrated circuits. It covers general operating and handling considerations with respect to the following critical factors:

- Operating supply-voltage range
- Power dissipation and derating
- System noise considerations
- Power-source rules
- Gate-oxide protection networks
- Input signals and ratings
- Chip assembly and storage
- Device mounting
- Testing

More specific information is then given on significant features, special design and application requirements, and standard ratings and electrical characteristics for COS/MOS A- and B-series logic circuits, COS/MOS timekeeping and special circuits, and COS/MOS microprocessor circuits (including CPU's, RAM's, ROM's, and I/O's).

GENERAL OPERATING AND HANDLING CONSIDERATIONS

The following paragraphs discuss some key operating and handling considerations that must be taken into account to achieve maximum advantage of the COS/MOS technology. Additional information on the operation and handling of COS/MOS integrated circuits is given in ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits," included in the Application Notes Section of this DATABOOK.

Operating Supply-Voltage Range

Because logic system occasionally experience transient conditions on the power-supply line which, when added to the nominal power-bus voltage, could exceed the safe limits of circuits connected to the power bus, the recommended operating supply-voltage ranges are 3 to 12 volts for A-series devices and 3 to 18 volts for B-series devices. The recommended maximum power-supply limit is substantially below the minimum primary breakdown limit for the devices to allow for limited power-supply transient and regulation limits. For circuits that operate in a linear mode over a portion of the voltage range, such as RC or crystal oscillators, a minimum supply voltage of at least 4 volts is recommended.

Power Dissipation and Derating

The power dissipation of a COS/MOS integrated circuit is the sum of a dc (quiescent) component and an ac (dynamic) component. The dc component is the sum of the net integrated-circuit reverse diode-junction current and the surface leakage current times the supply voltage. In standard A- or B-series logic devices, the dc dissipation typically ranges, depending upon device complexity, from 100 to 400 milliwatts for a supply voltage of 10 volts. Worst-case dc dissipation is the product of the maximum quiescent current (given in the data sheet on each device) and the dc supply voltage V_{DD}.

The dynamic (ac) power dissipation is approximately equal to the product CV^2f, where C is the net output capacitive load being charged and discharged by the integrated circuit, V is the supply voltage, and f is the output switching frequency. The product CV^2f accounts for approximately 90 per cent of the dynamic dissipation. The remaining 10 per cent is contributed by the momentary flow of IC switching current through the p- and n-MOS transistors to ground.

All COS/MOS devices are rated at 200 mW per package at the maximum operating ambient temperature rating (T_A) for the package type (85°C for plastic packages and 125°C for ceramic packages). Power ratings for temperatures below the maximum operating temperature are shown in the standard COS/MOS thermal derating chart in Fig. 1. This chart assumes that (a) the device is mounted and soldered (or placed in a socket) on a PC board; (b) there is natural convection cooling, with the PC board mounted horizontally; and (c) the pressure is standard (14.7 psia). In addition to the over-all package dissipation, device dissipation per output transistor is limited 100 mV maximum over the full package operating-temperature range.

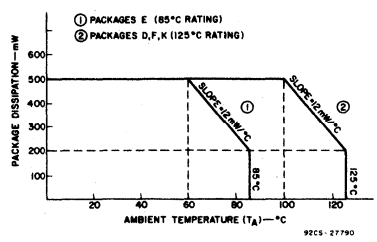


Fig. 1 – Standard COS/MOS thermal derating chart.

System Noise Considerations

In general, COS/MOS devices are much less sensitive to noise on power and ground lines than bipolar logic families (such as TTL or DTL). However, this sensitivity varies as a function of the power-supply voltage, and more importantly as a function of synchronism between noise spikes and input transitions. Good power distribution in digital systems requires that the power bus have a low dynamic impedance; for this purpose, discrete decoupling capacitors should be distributed across the power bus. A more detailed discussion of COS/MOS noise immunity is provided by ICAN-6587, "Noise Immunity of B-series COS/MOS Integrated Circuits," in the Application Notes Section.

Power-Source Rules

Fig. 2 shows the basic COS/MOS inverter and its gate-oxide protection network plus inherent diodes. The safe operating procedures listed below can be understood by reference to this inverter:

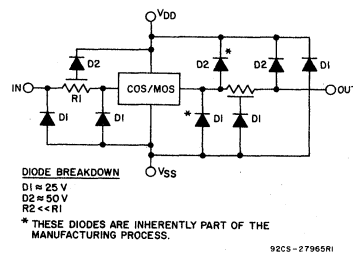


Fig. 2 – Basic COS/MOS inverter with B-series types protection network.

1. When separate power supplies are used for the COS/MOS device and for the device inputs, the device power supply should always be turned on before the independent input signal sources, and the input signals should be turned off before the power supply is turned off ($V_{SS} \leq V_I \leq V_{DD}$ as a maximum limit). This rule will prevent over-dissipation and possible damage to the the D2 input-protection diode when the device power supply is grounded. When the device power supply is an open circuit, violation of this rule can result in undersired circuit operation although device damage should not result; ac inputs can be rectified by diode D2 to act as a power supply.

2. The power-supply operating voltage should be kept safely below the absolute maximum supply rating, as indicated previously.
3. The power-supply polarity for COS/MOS circuits should not be reversed. The positive (V_{DD}) terminal should never be more than 0.5 volt negative with respect to the negative (V_{SS}) terminal ($V_{DD}-V_{SS} > -0.5$ V). Reversal of polarities will forward-bias and short the structural and protection diode between V_{DD} and V_{SS}.
4. V_{DD} should be equal to or greater than V_{CC} for COS/MOS buffers which have two power supplies (in particular, for CD4009 and CD4010 COS/MOS-to-TTL "down"-conversion devices).
5. Power-source current capability should be limited to as low a value as reasonable to assure good logic operation.
6. Large values of resistors in series with V_{DD} or V_{SS} should be avoided; transient turn-on of input protection diodes can result from drops across such resistors during switching.

Gate-Oxide Protection Network

A problem occasionally encountered in handling and testing low-power semiconductor devices, including MOS and small-geometry bipolar devices, has been damage to gate oxide and/or p-n junctions. Fig. 3 shows the gate-oxide protection circuits used to protect COS/MOS devices from static electricty damage. ICAN-6572 gives further information on protection circuits. Although these circuits are included in all COS/MOS devices, the handling precautions in ICAN-6572 and ICAN-6525 should be observed.

Input Signals and Ratings

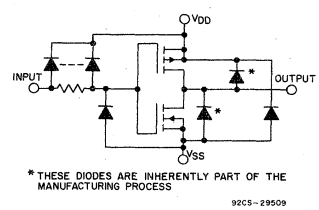
1. Input signals should be maintained within the power-supply voltage range, $V_{SS} \leq V_I \leq V_{DD}$. In applications such as astable and monostable multivibrators, input current can flow and, for optimal performance, should be limited to 100 microamperes by use of a resistor in series with the input terminal. The added protection assures proper circuit operation and prevents possible parasitic bipolar effects.
2. All COS/MOS inputs should be terminated. When COS/MOS inputs are wired to edge card connectors with COS/MOS drive coming from another PC board, a shunt resistor should be connected to V_{DD} or V_{SS} in case the inputs become unterminated with the power supply on.
3. When COS/MOS circuits are driven by TTL logic, a pull-up" resistor should be connected from the COS/MOS input to 5 volts (further information is given in ICAN-6602).
4. Input signals, should be maintained within the recommended input-signal-swing range.

Output Rules

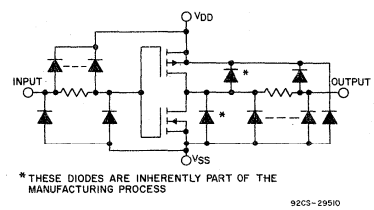
1. The power dissipation in a COS/MOS package should not exceed the rated value for the ambient temperature specified. The actual dissipation should be calculated when (a) shorting outputs directly to V_{DD} or V_{SS}, (b) driving low-impedance loads, or (c) directly driving the base of p-n-p or n-p-n bipolar transistor.
2. Output short circuits often result from testing errors or improper board assembly. Shorts on buffer outputs or across power supplies greater than 5 volts can damage COS/MOS devices.
3. COS/MOS, like active pull-up TTL, cannot be connected in the "wire-OR" configuration because an "on" PMOS and an "on" NMOS transistor could be directly shorted across the power-supply rails.
4. Paralleling inputs and outputs of gates is recommended only when the gates are within the same IC package.
5. Output loads should return to a voltage within the supply-voltage range (V_{DD} to V_{SS}).
6. Large capacitive loads (greater than 5000 pF) on COS/MOS buffers or high-current drivers act like short circuits and may over-dissipate output transistors.
7. Output transistors may be over-dissipated by operating buffers as linear amplifiers or using these types as one-shot or astable multivibrators.

Noise Immunity and Noise Margin

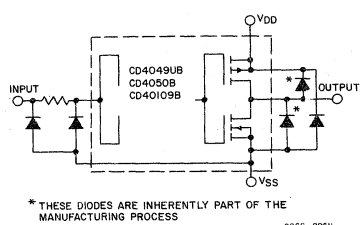
The complementary structure of the inverter, common to all COS/MOS logic devices, results in a near-ideal input-output transfer characteristic, with switching point midway (45% to 55%) between the 0 and 1 output logic levels. The result is high dc noise immunity.



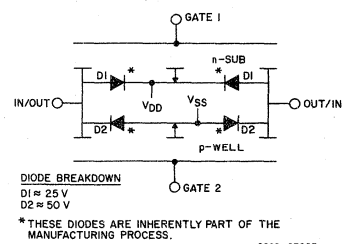
(a) For standard A-series COS/MOS product.



(b) For improved B-series COS/MOS product.



(c) For CD4049UB, CD4050B, and CD40109B COS/MOS types.



(d) For COS/MOS transmission gates.

Fig. 3 – Gate-oxide protection networks used in RCA COS/MOS integrated circuits.

General Operating and Application Considerations

Fig. 4 shows a typical transfer curve that may be use to define the noise immunity of COS/MOS integrated circuits. The noise-immunity voltage (V_{IL} or V_{IH}) is the noise voltage at any one input that does not propagate through the system. Minimum noise immunity for buffered B-series COS/MOS devices is 30, 30, and 27 per cent, respectively for supply voltages V_{DD} of 5, 10, and 15 volts and 20 per cent of V_{DD} for all unbuffered gates. The V_{IL} and V_{IH} specifications define the maximum permissible additive noise voltage at an input terminal when input signals are within 50 millivolts of the supply rails.

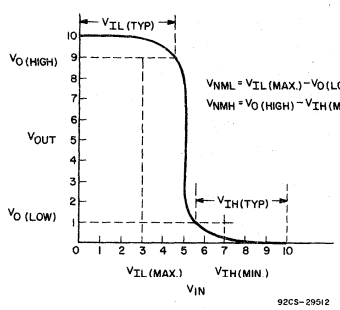


Fig. 4 — Typical transfer curve for a inverting gate at V_{DD} = 10 V.

Noise margin is the difference between the noise-immunity voltage (V_{IL} or V_{IH}) and the output voltage V_O. Noise-margin voltage is the maximum voltage that can be impressed upon an input voltage V_{IN} (where V_{IN} is the V_{OL} or V_{OH} voltage of the preceding state) at any (or all) logic I/O terminals without upsetting the logic or causing any output to exceed the output voltage (V_O) conditions specified for V_{IL} and V_{IH} ratings. Fig. 5 illustrates the noise-margin concept in a simple system. Noise margins for buffered B-series COS/MOS devices are 1, 2, and 2.5 volts, respectively, for supply voltages of 5, 10, and 15 volts.

Of the two noise-limitation specifications (noise immunity and noise margin), RCA considers noise immunity to be more practical for COS/MOS devices because COS/MOS outputs are normaliy within 50 millivolts of supply rails.

Noise immunity increases as the input pulse width becomes less than the propagation delay of the circuit. This condition is often described as ac noise immunity. (Further information on noise immunity is given in ICAN-6385).

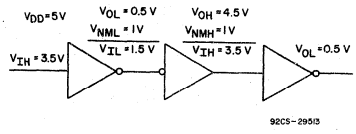


Fig. 5 — Noise margin example using inverters.

Clock Rise-and Fall-Time Requirements

Most COS/MOS clocked devices have maximum rise- and fall-time ratings (normally 5 to 15 microseconds). With longer rise of fall times, a device may not function properly because of data ripple-through, false triggering problems, etc. Whenever feasible, B-series COS/MOS counters have Schmitt-trigger shaping circuits built into the clock circuit thereby negating the restriction for input rise or fall times of 5 to 15 microseconds. Long rise and fall times on COS/MOS buffer-type inputs cause increased power dissipation which may exceed device capability for operating power-supply voltages greater than 5 volts.

Parallel Clocking

Process variations leading to differences in input threshold voltage among random device samples can cause loss of data between certain synchronously clocked sequential circuits, as shown in Fig. 6. This problem can be avoided if the clock rise time (t_rCL) is made less than the total of the fixed propagation delay plus the output transition time of the first stage, as determined from the device data for the specific loading condition in effect. Schmitt trigger circuits such as the CD4093B are an ideal solution to applications requiring wave-shaping.

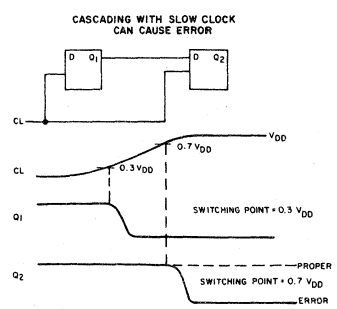


Fig. 6 — Error effect that results from a slow clock in cascaded circuits.

Three-State Logic

Three-state logic can be easily implemented by use of a transmission gate in the output circuit; this technique provides a solution to the wire-OR problem in many cases.

Chip Assembly and Storage

RCA COS/MOS integrated circuits are provided in chip form (H suffix) to allow customer design of special and complex circuits to suit individual needs. COS/MOS chips are electrically identical and offer the features of their counterparts sealed in ceramic and plastic packages. The following paragraphs describe mounting considerations, packaging, shipping and storage criteria, handling criteria, visual inspection criteria, testing criteria, and bonding pad layout and dimensions for each chip.

Mounting Considerations. All COS/MOS chips are non-gold backed and require the use of epoxy mounting. DuPont No. 5504A conductive silver paste or equivalent is recommended. In any case the manufacturer's recommendations for storage and use should be followed. If DuPont No. 5504A paste is used, the bond should be cured at temperatures between 185°C and 200° for 75 minutes.

In COS/MOS circuits MOS-transistor p-channel substrates (n-type bulk material) are connected to V_{DD}, therefore, when chips are mounted and a conductive paste is used care must be taken to keep the active substrate isolated from ground or other circuit elements.

Packing, Shipping, and Storage Criteria. Solid-state chips, unlike packaged devices, are non-hermetic devices, normally fragile and small in physical size, and therefore, require special handling considerations as follows:

1. Chips must be stored under proper conditions to insure that they are not subjected to a moist and/or contaminated atmosphere that could alter their electrical, physical, or mechanical characteristics. After the shipping container is opened, the chip must be stored under the following conditions:
   A. Storage temperature, 40°C max.
   B. Relative humidity, 50% max.
   C. Clean, dust-free environment.
2. The user must exercise proper care When handling chips to prevent even the slightest physical damge to the chip

3. During mounting and lead bonding of chips the user must use proper assembly techniques to obtain proper electrical, thermal, and mechanical performance.
4. After the chip has been mounted and bonded, any necessary procedure must be followed by the user to insure that these non-hermetic chips are not subjected to moist and contaminated atmosphere which might cause the development of electrical conductive paths across the relatively small insualting surfaces. In addition, proper consideration must be given to the protection of these devices from other harmful environments which could conceivably adversely affect their proper performance.

Handling Criteria. The user should find the following suggested precautions helpful in handling COS/MOS chips.

In any event, because of the extremely small size and fragile nature of chips, the equipment designer should exercise care in handling these devices.

For additional handling considerations for COS/MOS devices, refer to ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits."

1. **Grounding**
   a. Bonders, pellet pick-up tools, table tops, trim and form tools, sealing equipment, and other equipment used in chip handling should be properly grounded.
   b. The operator should be properly grounded.

2. **In-Process Handling**
   a. Assemblies of subassemblies of chips should be transported and stored in conductive carriers.
   b. All external leads of the assemblies or subassemblies should be shorted together.

3. **Bonding Sequence**
   a. Connect V_{DD} first to external connections, for example, terminal 14 of the CD4001AH.
   b. Remaining functions may be connected to their external connections in any sequence.

4. **Testing**
   a. Transport all assemblies of chips in conductive carriers.
   b. In testing chip assemblies or subassemblies, the operator should be properly grounded.

Visual Inspection Criteria. All standard commercial COS/MOS chips undergo a visual inspection which is patterned after MIL-STD-883, Method 2010.1, Condition B with modifications reflecting COS/MOS requirements.

Testing Criteria. COS/MOS chips are dc electrically tested 100% in accordance with the same standards prescribed for RCA devices in standard packages.

Device Testing

RCA COS/MOS circuits are 100-percent tested by circuit probe in the wafer stage and are 100-percent tested again after they have been packaged. DC tests of RCA devices are performed at 5, 10, 15, and 20 volts; functionality is checked at 3, 17, and 22 volts depending on family (i.e., A or B series). Sample testing is used to assure adherence to quality requirements and ac specifications.

Static tests, high-speed functional and dc parametric tests, are performed at wafer and package stages by means of a Teradyne J283 test set. A Teradyne S157CM test set and a Marcodata MD154 test set are used in dynamic testing. Dynamic tests are performed with 15 and 50 picofarad loads. Testing at 15 picofarads is accomplished primarily by laboratory "bench-test" techniques; automatic testing at 15 picofarads is difficult because of the high input capacitance (approximately 20 to 35 picofarads) of most automatic ac test sets.

Users should follow the sequence below when testing COS/MOS devices:

1. Insert the device into the test socket.
2. Apply V_{DD}.
3. Apply the input signal.
4. Perform the test.
5. On completion of test, remove the input signal.
6. Turn off the power supply (V_{DD}).
7. Remove the device from the test socket an insert it into a conductive carrier. COS/MOS devices under test must not be exposed to electrostatic discharge or forward biasing of the intrinsic protective diodes shown in Fig. 3.

Detailed information on the techniques employed in the testing of RCA COS/MOS integrated circuits are described in ICAN-6532 included in the Application Notes section of this DATABOOK.

Device Mounting

Integrated circuits are normally supplied with lead-tin plated leads to facilitate soldering into circuit boards. In those relatively few applications requiring welding of the device leads, rather than soldering, the devices may be obtained with gold or nickel plated Kovar leads.* It should be recognized that this type of plating will not provide complete protection against lead corrosion in the presence of high humidity and mechanical stress. The aluminum-foil-lined cardboard "sandwich pack" employed for static protection of the flat-pack also provides some additional protection against lead corrosion, and it is recommended that the devices be stored in this package until used.

In any method of mounting integrated circuits which involves bending or forming of the device leads, it is extremely important that the lead be supported and clamped between the bend and the package seal, and that bending be done with care to avoid damage to lead plating. In no case should the radius of the bend be less than the diameter of the lead, or in the case of rectangular leads, such as those used in RCA 14-lead and 16-lead flat-packages, less than the lead thickness. It is also extremely important that the ends of the bent leads be straight to assure proper insertion through the holes in the printed-circuit board.

A-SERIES COS/MOS INTEGRATED CIRCUITS

RCA CD4000A-series types have a maximum dc supply-voltage rating of −0.5 to 15 volts, and a recommended operating supply-voltage range of 3 to 12 volts. The major features of this series are as follows:

- Quiescent current specified to 15 volts
- 5-volt and 10-volt parametric ratings
- Maximum input leakage of 1 μA at 15 volts over the full package operating-temperature range
- 1-volt noise margin (full package temperature range)

Table I shows the maximum ratings and the recommended operating supply-voltage range for RCA A-series COS/MOS integrated circuits.

Static Electrical Characteristics

Table II shows the standard dc electrical characteristics for A-series types. The data sheet for each of these types contains the family characteristics shown in Table I plus additional dc characteristics that are type-dependent.

*Mil-M-38510A, paragraph 3.5.6.1 (a), lead material.

General Operating and Application Considerations

Table I — Maximum Rating and Recommend Operating Conditions for A-Series COS/MOS Integrated Circuits

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, V_{DD} (Voltages referenced to V_{SS} terminal) . . . . −0.5 to +15 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (Package Type E) . . . . . 500 mW
For T_A = +60 to +85°C (Package Type E) . . . . . Derate Linearly to 200 mW
For T_A = −55 to +100°C (Package Types D,K,H) . . . . . 500 mW
For T_A = +100 to +125°C (Package Types D,K,H) Derate Linearly to 100 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full package-temperature range (All package types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
Package Types D,K,H . . . . . −55 to +125°C
Package Type E . . . . . −40 to +85°C
STORAGE-TEMPERATURE RANGE (T_{STG}) . . . . . −65 to 150°C
LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	12	V

Table II — A-Series Static Electrical Characteristics (Full Package Temperature Range)

SYMBOL	PARAMETER	CONDITIONS				LIMITS			UNITS
		V_{IN}	V_O (volts)		V_{DD}				
		VOLTS	MIN.	MAX.	VOLTS	MIN.	TYP.	MAX.	
V_{OL}	Output Low Voltage	5	—	—	5	—	0	0.05	V
		10	—	—	10	—	0	0.05	V
V_{OH}	Output High Voltage	0	—	—	5	4.95	5	—	V
		0	—	—	10	9.95	10	—	V
V_{NL} (SSI Types)	Noise Voltage (Input Low)	—	3.6	—	5	1.5	2.25	—	V
		—	7.2	—	10	3	4.5	—	V
V_{NH} (SSI Types)	Noise Voltage (Input High)	—	—	1.4	5	1.5	2.25	—	V
		—	—	2.8	10	3	4.5	—	V
V_{NL} (MSI Types)	Noise Voltage (Input Low)	—	4.2	—	5	1.5	2.25	—	V
		—	9.0	—	10	3	4.5	—	V
V_{NH} (MSI Types)	Noise Voltage (Input High)	—	—	0.8	5	1.5	2.25	—	V
		—	—	1.0	10	3	4.5	—	V
V_{NML}	Noise Margin (Input Low)	—	4.5	—	5	1	—	—	V
		—	9.0	—	10	1	—	—	V
V_{NMH}	Noise Margin (Input High)	—	—	0.5	5	1	—	—	V
		—	—	1.0	10	1	—	—	V
I_{IL}, I_{IH}	Input Leakage Low	—	—	—	15	—	$\pm 10^{-5}$	±1	μA
I_L	Quiescent Device Leakage	—	—	—	5,10,15	See Data Sheets			μA
I_{DN}, I_{DP}	Output Source and Sink current	—	—	—	5,10	See Data Sheets			ma

Note: Logic Level Inversion Assumed in Table II.

Dynamic Electrical Characteristics

A-series dynamic electrical characteristics are specified for individual types under the following conditions: V_{DD} = 5 V and 10 V; T_A = 25°C (temperature coefficient is typically 0.3%/°C); C_L = 15 pF; t_r and t_f of inputs = 20 ns.

HIGH-VOLTAGE B-SERIES COS/MOS INTEGRATED CIRCUITS

RCA-CD4000B-series types have a maximum dc supply-voltage rating of −0.5 to 20 volts, and a recommended operating supply-voltage range of 3 to 18 volts. The major features of this series are as follows:

- High-voltage (20-V) ratings
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) =
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices

JEDEC Minimum Standard

Under the sponsorship of the Joint Electron Devices Engineering Council (JEDEC) of the Electronic Industries Association (EIA), minimum industrial standards have been established for the maximum ratings and static electrical characteristics of B-series CMOS integrated circuits. The JEDEC standard (JEDEC Tentative Standard No. 13A) defines B-series CMOS integrated circuits as a uniform family of both buffered and unbuffered types that have an absolute dc supply-voltage rating of at least 18 volts.

Buffered CMOS devices are types in which the output "on" impedance is independent of any and all valid input logic conditions, both preceding and present. All such CMOS product are designated by the suffix "B" following the basic type number.

Unbuffered CMOS devices are types that meet all B-series specifications except that the logical outputs are not buffered and the noise-immunity voltages, V_{IL} and V_{IH}, are specified as 20 and 80 per cent, respectively, of V_{DD} for operation from 5 or 10 volts and 17 and 83 per cent, respectively, of V_{DD} for operation from 15 volts. All such CMOS product are designated by the suffix "UB."

The JEDEC minimum standard also includes in the B-series CMOS types that have analog inputs or outputs and, in addition, have maximum ratings and logical input and output parameters that conform to B-series specifications wherever applicable. These CMOS devices are also designated by the suffix "B."

All B-series CMOS devices can directly replace their A-seires counterparts in most applications. The UB types are high-voltage versions of corresponding A-series (unbuffered) types.

Table III lists the JEDEC minimum standards established for the maximum ratings and recommended operating conditions for B-series CMOS integrated circuits.

Table IV shows the JEDEC standards for the static electrical characteristics of CMOS B-series integrated circuits.

Standardized RCA Ratings and Static Characteristics

RCA B-series COS/MOS integrated circuits meet or exceed the most stringent requirements of the JEDEC B-series specifications. Table V shows the standardized maximum ratings and recommended operating supply-voltage range for RCA B-series COS/MOS integrated circuits. The standardized static electrical characteristics for these devices are shown in Table VI. As with the JEDEC specifications, the RCA standardized characteristics classifies the B-series devices into three leakage (quiescent-device-current) categories. Table VII lists the RCA types in each category and indicates types that, although they are still B-series types, differ in one or more static characteristics.

Tables V and VI show that, in a number of important respects, RCA has established new performance standards for B-series COS/MOS logic circuits:

1. **Tight limits for all packages**
   RCA devices use the same set of limits for all package styles. The JEDEC standard establishes two sets of limits for most dc (static) parameters: a tight set for products having a full operating temperature range of −55°C to +125°C (normally used for ceramic packages), and a relaxed set for products having a limited temperature range of −40°C to +85°C (normally used for plastic packages). Because RCA supplies only one premium grade of B-series product in all package styles (i.e., fall-out chips are *not* used), all B-series COS/MOS devices are specified to the tight set of limits only.
2. **Improved voltage rating**
   All RCA B-series devices are tested to voltages as high as 22 volts and have an absolute maximum dc supply voltage rating of 20 volts. This higher rating permits greater derating for reliable 15-volt operation, permits greater 15-

Table III – JEDEC Minimum Standards for Maximum Ratings and Recommended Operating Conditions for B-Series CMOS Integrated Circuits*

Absolute Maximum Ratings (Voltages referenced to V_{SS}):			
DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Input Voltage	V_{IN}	−0.5 to V_{DD} +0.5	Vdc
DC Input Current (any one input)	I_{IN}	±10	mAdc
Storage Temperature Range	T_S	−65 to +150	°C
Recommended Operating Conditions:			
DC Supply Voltage	V_{DD}	+3 to +15	Vdc
Operating-Temperature Range:	T_A		
Military-Range Devices		−55 to +125	°C
Commercial-Range Devices		−40 to +85	°C

* Reprinted from JEDEC Tentative Standard No. 13-A, "Standard Specifications for Description of B-Series CMOS Devices."

Table IV – JEDEC Standard for Static Characteristics of B-Series CMOS Integrated Circuits▲

PARAMETER		TEMP. RANGE	V_{DD} (Vdc)	CONDITIONS	LIMITS T_{LOW}* Min	T_{LOW}* Max	+25°C Min	+25°C Typ	+25°C Max	T_{HIGH}* Min	T_{HIGH}* Max	Units
I_{DD}	Quiescent Device Current GATES	Mil	5 10 15	$V_{IN} = V_{SS}$ or V_{DD}		0.25 0.5 1.0			0.25 0.5 1.0		7.5 15 30	uAdc
		Comm	5 10 15	All valid input combinations		1.0 2.0 4.0			1.0 2.0 4.0		7.5 15 30	
	BUFFERS, FLIP-FLOPS	Mil	5 10 15	$V_{IN} = V_{SS}$ or V_{DD}		1.0 2.0 4.0			1.0 2.0 4.0		30 60 120	uAdc
		Comm	5 10 15	All valid input combinations		4 8 16			4.0 8.0 16.0		30 60 120	
	MSI	Mil	5 10 15	$V_{IN} = V_{SS}$ or V_{DD}		5 10 20			5 10 20		150 300 600	uAdc
		Comm	5 10 15	All valid input combinations		20 40 80			20 40 80		150 300 600	
V_{OL}	Low-Level Output Voltage	All	5 10 15	$V_{IN} = V_{SS}$ or V_{DD} $\|I_O\| < 1uA$		0.05 0.05 0.05			0.05 0.05 0.05		0.05 0.05 0.05	Vdc
V_{OH}	High-Level Output Voltage	All	5 10 15	$V_{IN} = V_{SS}$ or V_{DD} $\|I_O\| < 1uA$	4.95 9.95 14.95		4.95 9.95 14.95			4.95 9.95 14.95		Vdc
V_{IL}	Input Low Voltage	All	5 10 15	$V_O = 0.5V$ or $4.5V$ $V_O = 1.0V$ or $9.0V$ $V_O = 1.5V$ or $13.5V$ $\|I_O\| < 1uA$		1.5 3.0 4.0			1.5 3.0 4.0		1.5 3.0 4.0	Vdc
V_{IH}	Input High Voltage	All	5 10 15	$V_O = 0.5V$ or $4.5V$ $V_O = 1.0V$ or $9.0V$ $V_O = 1.5V$ or $13.5V$ $\|I_O\| < 1uA$	3.5 7.0 11.0		3.5 7.0 11.0			3.5 7.0 11.0		Vdc
I_{OL}	Output Low (Sink) Current	Mil	5 10 15	$V_O = 0.4V$ $V_{IN} = 0$ or $5V$ $V_O = 0.5V$, $V_{IN} = 0$ or $10V$ $V_O = 1.5V$, $V_{IN} = 0$ or $15V$	0.64 1.6 4.2		0.51 1.3 3.4			0.36 0.9 2.4		mAdc
		Comm	5 10 15	$V_O = 0.4V$, $V_{IN} = 0$ or $5V$ $V_O = 0.5V$, $V_{IN} = 0$ or $10V$ $V_O = 1.5V$, $V_{IN} = 0$ or $15V$	0.52 1.3 3.6		0.44 1.1 3.0			0.36 0.9 2.4		mAdc
I_{OH}	Output High (Source) Current	Mil	5 10 15	$V_O = 4.6V$, $V_{IN} = 0$ or $5V$ $V_O = 9.5V$, $V_{IN} = 0$ or $10V$ $V_O = 13.5V$, $V_{IN} = 0$ or $15V$	−0.25 −0.62 −1.8		−0.2 −0.5 −1.5			−0.14 −0.35 −1.1		mAdc

Table IV – JEDEC Standard for Static Characteristics of B-Series CMOS Integrated Circuits▲ (cont'd)

PARAMETER		TEMP. RANGE	V_{DD} (Vdc)	CONDITIONS	LIMITS							Units
					T_{LOW}*		+25°C			T_{HIGH}*		
					Min	Max	Min	Typ	Max	Min	Max	
I_{OH}	Output High (Source) Current (cont'd)	Comm	5	V_O = 4.6V, V_{IN} = 0 or 5V	-0.2		-0.16			-0.12		mAdc
			10	V_O = 9.5V, V_{IN} = 0 or 10V	-0.5		-0.4			-0.3		mAdc
			15	V_O = 13.5V, V_{IN} = 0 or 15V	-1.4		-1.2			-1.0		mAdc
I_{IN}	Input Current	Mil	15	V_{IN} = 0 or 15V		±0.1			±0.1		±1.0	uAdc
		Comm	15	V_{IN} = 0 or 15V		±0.3			±0.3		±1.0	uAdc
C_{IN}	Input Capacitance per Unit Load	All	–	Any Input					7.5			pF

*T_{LOW} = -55°C for Military Temp. Range device, -40°C for Commercial Temp. Range device
*T_{HIGH} = +125°C for Military Temp. Range device, +85°C for Commercial Temp. Range device
▲Reprinted from JEDEC Tentative Standard No. 13-A, "JEDEC Standard Specification for Description of B-Series CMOS Device."

Table V – RCA Standardized Maximum Ratings and Recommended Operating Conditions for B-Series COS/MOS Integrated Circuits

Maximum Ratings, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . -0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . -55 to +125°C
PACKAGE TYPE E . . . . . -40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

Recommended Operating Conditions:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

volt supply tolerance and peak transients, and permits system use to 18-volts with confidence.

3. Wider operating range

All RCA B-series devices have a recommended maximum operating voltage of 18-volts. This higher limit permits 18-volt system supply operation, and also permits wider power-source tolerances and transients for supplies normally set up to 18 volts.

4. Lower leakage current

The JEDEC standard establishes three sets of limits for quiescent device current (I_{DD}) intended to match chip complexity to device leakage current as realistically as possible. For all three levels of chip complexity, all RCA B-series devices (regardless of package) conform to the tighter set of limits established in the standard. In addition, a maximum rating is specified at 20V, as well as at 5V, 10V, and 15V. As a result:

Table VI – RCA B-Series COS/MOS Standardized Electrical Characteristics

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at -55, +25, +125 Apply to D,K,F,H Packages Values at -40, +25, +85 Apply to E Package							UNITS
									+25		
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max. Gates, Inverters▲	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Buffers, Flip-Flops, Latches, Multi-Level Gates (MSI-1 Types)▲		0,5	5	1	1	30	30	–	0.02	1	
		0,10	10	2	2	60	60	–	0.02	2	
		0,15	15	4	4	120	120	–	0.02	4	
		0,20	20	20	20	600	600	–	0.04	20	
Complex Logic (MSI-2 Types)▲		0,5	5	5	5	150	150	–	0.04	5	
		0,10	10	10	10	300	300	–	0.04	10	
		0,15	15	20	20	600	600	–	0.04	20	
		0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	–	
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	–	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	–	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max. B Types	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5, 13.5	–	15	4				–	–	4	
UB Types	0.5, 4.5	–	5	1				–	–	1	
	1, 9	–	10	2				–	–	2	
	1.5, 13.5	–	15	2.5				–	–	2.5	
Input High Voltage, V_{IH} Min. B Types	0.5, 4.5	–	5	3.5				3.5	–	–	
	1, 9	–	10	7				7	–	–	
	1.5, 13.5	–	15	11				11	–	–	
UB Types	0.5, 4.5	–	5	4				4	–	–	
	1, 9	–	10	8				8	–	–	
	1.5, 13.5	–	15	12.5				12.5	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA
3-State Output Leakage Current I_{OUT} Max.	0, 18	0,18	18	±0.4	±0.4	±12	±12	–	$\pm 10^{-4}$	±4	μA

▲Classifications of RCA COS/MOS B-Series Types are shown in Table VII.

Table VII – Classification of RCA B-Series COS/MOS Integrated Circuits

Gates/ Inverters		Buffers/Flip-Flop/ Latches/Multi-Level Gates (MSI-1)		Complex Logic (MSI-2)		
CD4000B	**CD4023UB**	**CD4009UB■**	**CD4070B**	CD4006B	**CD4051B■**	**CD4527B**
CD4000UB	CD4025B	**CD4010B■**	**CD4077B**	**CD4008B**	**CD4052B■**	**CD4532B**
CD4001B	**CD4025UB**	**CD4013B**	**CD4085B**	CD4014B	**CD4053B■**	**CD4555B**
CD4001UB	**CD4066B**	CD4019B	**CD4086B**	CD4015B	**CD4054B■**	**CD4556B**
CD4002B	**CD4068B**	**CD4027B**	**CD4093B**	CD4017B	**CD4055B■**	**CD40100B**
CD4002UB	**CD4069UB**	CD4030B	**CD4095B**	CD4018B	**CD4056B■**	**CD40101B**
CD4007UB	**CD4071B**	**CD4041UB**	**CD4096B**	CD4020B	CD4060B	**CD40102B**
CD4011B	**CD4072B**	**CD4042B**	**CD4098B**	CD4021B	**CD4063B**	**CD40103B**
CD4011UB	**CD4073B**	**CD4043B**	**CD4502B**	CD4022B	**CD4067B■**	**CD40104B**
CD4012B	**CD4075B**	**CD4044B**	CD40106B	CD4024B	**CD4076B**	**CD40105B**
CD4012UB	**CD4078B**	CD4047B	**CD40107B■**	CD4026B	**CD4089B**	CD40108B
CD4016B■	**CD4081B**	**CD4049UB■**	**CD40109B**	CD4028B	**CD4094B**	CD40110B
CD4023B	**CD4082B**	**CD4050B■**	CD40174B	CD4029B	**CD4097B■**	CD40160B
				CD4031B	**CD4099B**	CD40161B
				CD4032B	**CD4508B**	CD40162B
				CD4033B	**CD4510B**	CD40163B
				CD4034B	**CD4511B■**	**CD40181B**
				CD4035B	CD4512B	**CD40182B**
				CD4038B	**CD4514B**	**CD40192B**
				CD4040B	**CD4515B**	**CD40193B**
				CD4045B	**CD4516B**	**CD40194B**
				CD4046B	**CD4518B**	**CD40208B**
				CD4048B	**CD4520B**	**CD40257B**

■Indicated types for which, because of special design requirements, one or more static characteristics difffer from the standardized data. Refer to RCA data pages on these types for specific differences.

(a) In current-limited applications, COS/MOS users can depend on one tight leakage limit independent of package style selected.

(b) Customer use of COS/MOS product up through 18 volts is protected by a published tight leakage current specification at 20 volts (as well as by an input leakage specification at 18 volts).

5. Symmetrical output

All RCA B-series devices have balanced complementary output drive (i.e., the output high current I_{OH} rating is the same as the output low current I_{OL} rating) specified to the tighter set of limits established in the JEDEC standard. The balanced output provides uniform rise and fall time performance, improved system noise energy (dynamic) immunity, optimum device speed for both output switching low-to-high (t_{PLH}) and output switching high-to-low (t_{PHL}), and in general the identical high and low dc and ac characteristics normally associated with a good complementary output drive circuit. MOS system design, simulation, and performance are significantly enhanced by equal high and low dc and ac performance ratings and one tight specification limit for all package styles.

6. Improved input current (leakage) ratings

All RCA B-series devices (regardless of package) have a maximum input leakage current (I_{IN}) rating of 100 nA specified at voltages up to 18V, and a maximum limit of 1 μA st the upper limit of the package-temperature range. Actually, the 100 nA rating is a practical specification limited by the capability of commercial test equipment to measure lower currents. Laboratory tests show that input leakage currents of RCA B-series COS/MOS devices are significantly lower than this limit, typically ranging from 10 to 100 pA.

7. Buffered and unbuffered gates

The new industry standard establishes a suffix "UB" for CMOS products that meet all B-series specifications except that the logical outputs of the devices are not buffered and the V_{IL} and V_{IH} specifications are relaxed. The suffix "B" defines only buffered-output devices in which the output "on" impedance is independent of any and all valid input logic conditions, both preceding and present.

RCA will supply both buffered ("B") and unbuffered ("UB") versions of the popular NOR and NAND gates to make available to designers the advantages of both. The chart below briefly compares the features of the two versions (a more detailed coverage of the special features of B- and UB-series COS/MOS gates is provided by ICAN-6558 in the Application-Notes section):

Characteristic	Buffered Version ("B")	Unbuffered Version ("UB")
Propagation Delay (Speed)	Moderate	Fast
Noise Immunity/Margin	Excellent	Good
Output Impedance and Output Transition Time	Constant	Variable
AC Gain	High	Low
Output Oscillation for Slow Inputs	Yes	No
Input Capacitance	Low	High

General Operating and Application Considerations

8 Reliability

RCA B-Series COS/MOS integrated cir- incorporate the latest improvements in processing technology and plastic and ceramic packaging techniques. Product quality is real-time controlled using accelerated-temperature group quality screening in which tight B-series limits for dc parameters are criticized as test points.

Fig. 7 through 10 show the standardized n- and p-channel drain characteristics for B-series COS/MOS devices, and Figs. 11 through 14 show the normalized variation of output source and sink currents with respect to temperature and voltage in these devices.

B-Series Dynamic Electrical Characteristics

B-series dynamic electrical characteristics are specified for individual types under the following conditions: V_{DD} = 5 V; 10 V, and 15 V; T_A = 25°C; C_L = 50 pF; R_L = 200 kΩ; t_r and t_f = 20 ns. Table VIII lists dynamic characteristics specified for RCA B-series COS/MOS integrated circuits Figs. 15 through 18 show the variation of B-series dynamic parameters with temperature. Figs. 19 and 20 show the variation of output transition time with supply voltage. Fig. 21 shows the variation of the standardized output transition time with load capacitance.

Maximum propagation delay or transition times for values of C_L other than the specified 50 picofarads can be determined by use of the multiplication factor (usually 2) between the typical and maximum values given in the dynamic characteristics chart included in the technical data for each device applied to the typical curves, also shown in the device technical data.

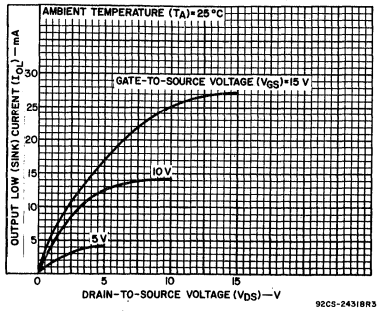


Fig. 7 – Typical output low (sink) current characteristics.

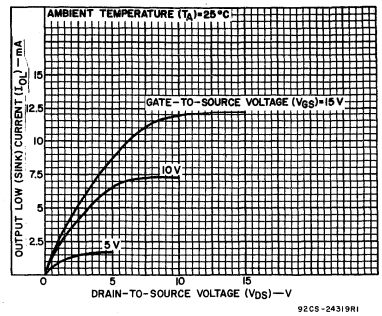


Fig. 8 – Minimum output low (sink) current characteristics.

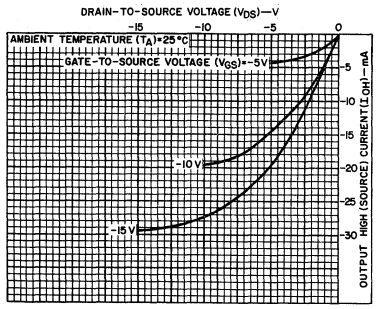


Fig. 9 – Typical output high (source) current characteristics.

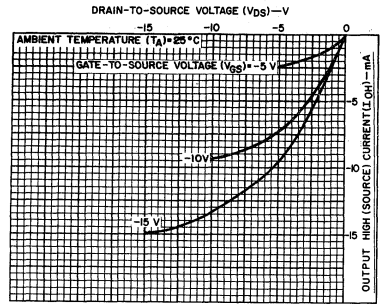


Fig. 10 – Minimum output high (source) current characteristics.

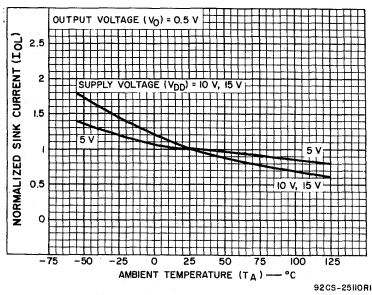


Fig. 11 – Variation of normalized output low (sink) current (I_{OL}) with temperature.

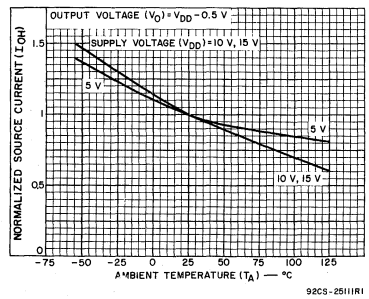


Fig. 12 – Variation of normalized output high (source) current (I_{OH}) with temperature.

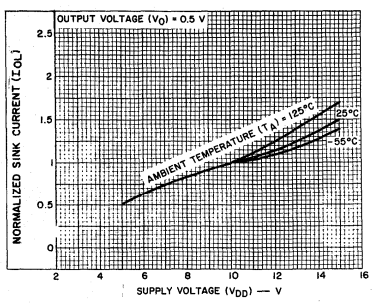


Fig. 13 – Variation of normalized output low (sink) current (I_{OL}) with supply voltage.

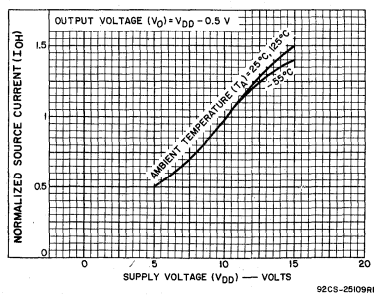


Fig. 14 – Variation of normalized output high (source) current (I_{OH}) with supply voltage.

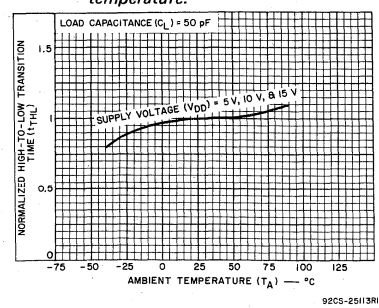


Fig. 15 – Variation of high-to-low transition time (t_{THL}) with temperature.

Table VIII - Dynamic Electrical Characteristics - Definitions

Characteristic	Symbol	Limits Max.	Limits Min.	Notes
Propagation Delay:				
Outputs going high to low	t_{PHL}	X		
Outputs going low to high	t_{PLH}	X		
Output Transition Time:				
Outputs going high to low	t_{THL}	X		
Outputs going low to high	t_{TLH}	X		
Pulse Width-Set, Reset, Preset Enable, Disable, Strobe, Clock	t_{WL} or t_{WH}		X	1
Clock Input Frequency	f_{CL}	X		1, 2
Clock Input Rise and Fall Time	t_{rCL}, t_{fCL}	X		
Set-Up Time	t_{SU}		X	1
Hold Time	t_H		X	1
Removal Time - Set, Reset, Preset-Enable	t_{REM}		X	1
Three State Disable Delay Times:				
High level to high impedance	t_{PHZ}	X		
High impedance to low level	t_{PZL}	X		
Low level to high impedance	t_{PLZ}	X		
High impedance to high level	t_{PZH}	X		

NOTE: (1) By placing a defining min. or max. in front of definition, the limits can change from min. to max., or vice versa.

(2) Clock input waveform should have a 50% duty cycle and be such as to cause the outputs to be switching from 10% V_{DD} to 90% V_{DD} in accordance with the divice truth table.

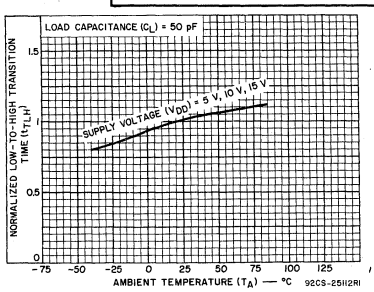


Fig. 16 – Variation of low-to-high transition time (t_{TLH}) with temperature.

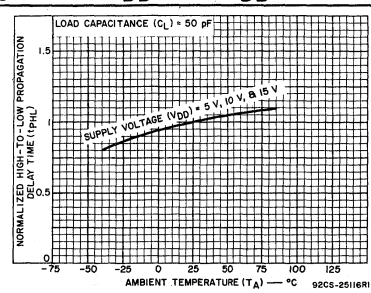


Fig. 17 – Variation of high-to-low propagation delay time (t_{PHL}) with temperature.

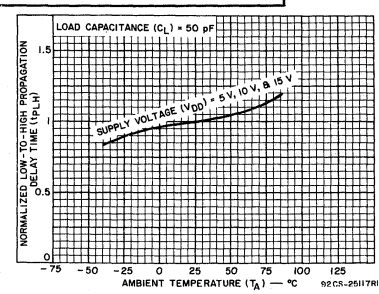


Fig. 18 – Variation of low-to-high propagation delay time (t_{PLH}) with temperature.

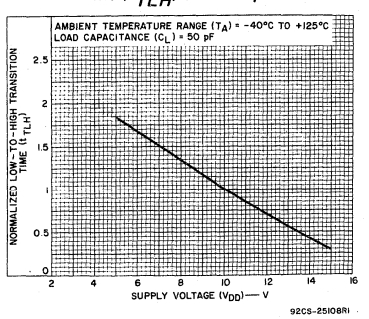


Fig. 19 – Variation of low-to-high transition time (t_{TLH}) with supply voltage.

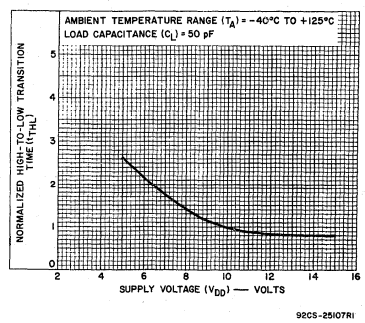


Fig. 20 – Variation of high-to-low transition time (t_{THL}) with supply voltage.

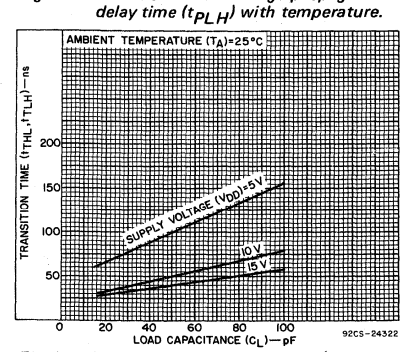


Fig. 21 – Variation of transition time (t_{THL}, t_{TLH}) with load capacitance of three levels of supply voltage.

General Operating and Application Considerations

B-Series Dynamic (AC) Switching Parameters

Table VIII defines the major COS/MOS ac characteristics, with reference to the waveforms shown in Figs. 22 through 25. Test conditions of V_{DD}, low capacitance (C_L), and input conditions are given for individual types in the published data.

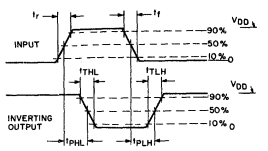
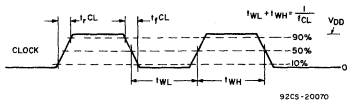


Fig. 22 – Tansition times and propagation delay times, combination logic.



Outputs should be switching from 10% V_{DD} to 90% V_{DD} in accordance with device truth table.

Fig. 23 – Clock-pulse rise and fall times and pulse width.

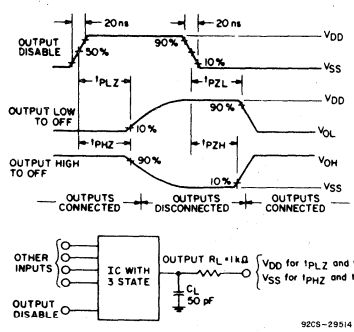


Fig. 24 – Three-state propagation delay wave shapes and test circuit.

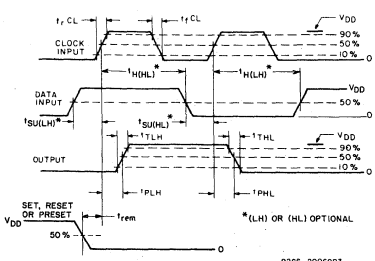


Fig. 25 – Setup times, hold times, removal time, and propagation delay times for positive-edge triggered sequential logic circuits.

COS/MOS TIMEKEEPING AND SPECIAL PRODUCTS

RCA supplies a variety of COS/MOS timekeeping products and a group of special COS/MOS products that have operating supply-voltage ranges and other characteristics that differ from the standardized data specified for A- and B-series COS/MOS integrated circuits.

COS/MOS Timekeeping Products

The RCA line of COS/MOS timekeeping circuits (CD220XX types) includes types that are designed for use as watch circuits, as wall- or auto-clock circuits, and as industrial times.

Watch Circuits. RCA standard commercial COS/MOS watch products include a line of liquid-crystal-display watch circuits that range from a 3½-digit, 2-function chip to a 6-digit, 6-function circuit with various additional features such as stopwatch and alarm circuitry. These circuits are designed to operate from a single battery cell.

Several RCA watch-circuit chips are offered in both direct and mirror-image versions to allow mounting on either side of a module board.

Wall-Clock Circuits. RCA COS/MOS wall-clock circuits are intended for operation from one or two battery cells under crystal control and designed to drive stepping motors. Standard commercial types include a 32-kHz circuit that is designed to drive a pulse-width-controlled Portescap motor and a 4-MHz silicon-on-sapphire circuit that operates from a single 1.5-volt cell.

Auto-Clock Circuits. RCA standard commercial auto-clock circuits include a line of stepping-motor-drive clock circuits that operate with crystal frequencies of 2, 3, and 4 MHz. All types are designed to meet the voltages and other conditions associated with the automobile environment.

Industrial Timers. Although RCA timekeeping products are usually intended primarily for use in watches, wall clocks, and auto clocks, they can also be used in a variety of industrial timing applications. Several standard COS/MOS timekeeping products have been used in industrial applications as appliance and thermostat-control timers. In addition, the CD22017E is specifically designed for use as an industrial timer.

Special COS/MOS Products

RCA COS/MOS integrated circuits classified as special types include a group of crosspoint switches (CD221XX types) intended for use in telephone and PBX systems, in studio audio switching applications, and as multisystem bus interconnects, and a series of low-voltage counter/decoder/drivers (CD229XX types) for use as general-purpose counters with a numeric display, as display drivers, and in clock, watch, and timer applications.

CDP 1800-SERIES MICROPROCESSOR PRODUCTS

The CDP1800 series consists of a comprehensive line of COS/MOS integrated circuit that, in addition to the CDP1802 central processing unit (CPU), includes a wide variety of types for use as ROM's, RAM's, and I/O circuits in microprocessor systems. Fig. 26 illustrate the interrelation of the CDP1802 central processing unit with the three additional circuit functions — program memory (ROM), data memory (RAM), and input/output (I/O) electronics — usually required in a microprocessor system.

The CDP1800 series is an all-COS/MOS family of integrated circuits. A CDP1800-series microprocessor system, therefore, provides all the advantages attendant to any CMOS system, including:

- minimal power-supply requirements
- completely static circuitry
- wide temperature range
- high noise immunity
- CMOS, TTL, NMOS compatibility. .

CDP1802 Central Processing Unit

The CDP1802 is an 8-bit silicon-gate COS/MOS integrated circuit designed for use as a general-purpose central processing unit in a COSMAC microprocessing system. It provides the following basic features:

- Standard 8-bit bidirectional data bus
- 16 x 16 matrix of registers for flexible programming
- DC to 6.4-MHz clock (single phase)
- Fast 2.5- or 3.75-μs instruction time
- 91 basic instructions, 255 operation codes
- Minimal power-supply requirements — low current drain, single-supply, unregulated
- Split-power-supply option that allows for 10 V on internal parts of CPU and 5 V on interfacing lines
- On-chip, single-phase clock
- Memory addressing to 65K bytes
- Adaptability to any combination of standard RAM, ROM, or PROM memories

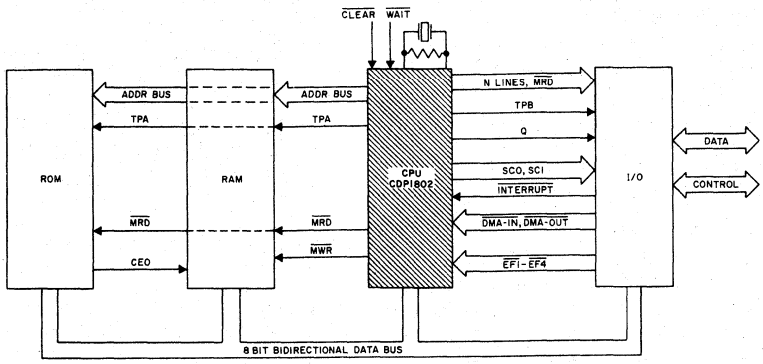


Fig. 26 – Typical CDP1802-based microprocessor system.

- Maskable interrupt and 4 testable external flag lines
- On-chip DMA controls
- Simple RESET, LOAD, PAUSE controls
- Programmable serial output (Q)

All CDP1800 Series ICs are available in two performance selections:

A type without a "C" suffix is the high-performance device. For example, the CDP1802 has:

- 3 V to 12 V recommended operating voltage range
- 2.5- or 3.75-μs instruction time
- 40-mW power dissipation (typical)
- 6.4-MHz maximum clock input frequency at 10 V.

A type with a "C" suffix is the commercial device. For example, the CDP 1802C has:

- 4 V to 6 V recommended operating voltage range
- 8 mW power dissipation (typical)
- 5- or 7.5-μs instruction time
- 3.2-MHz maximum clock input frequency at 5 V

Fig. 27 shows the COSMAC architecture for the CDP1802. The principal feature of this architecture is a register matrix consisting of sixteen 16-bit scratchpad registers. Individual registers in the array (R) are designated or selected by the 14-bit binary code from one of the 4-bit designators P, X, or N. The contents of any register can be directed to any one of the following three paths:

1. to the external memory (multiplexed, higher-order byte first, on to 8 memory address lines);
2. to the accumulator (either of the two bytes can be gated to it);
3. to the increment/decrement circuit where it is increased or decreased by one and stored back in the selected 16-bit register.

The three paths, depending on the nature of the instruction, may operate independently or in various combinations in the same machine cycle.

The registers in R can be used by a programmer in three different ways: as program counters, as data pointers, or as scratchpad locations (data registers) to hold two bytes of data.

Program Counters. Any register can be used as the main program counter; the number of the selected register is held in the P designator. Other registers in R can be used as subroutine program counters. By a single instruction, the contents of the P register can be changed to effect a "call" to a subroutine. When interrupts are being serviced, register R(1) is used as the program counter for the interrupt servicing routine. At all other times the register designated as program counter is at the discretion of the user.

Data Pointers. The registers in R may be used as data pointers to indicate a location in memory. The register designated by X (i.e., R(X)) points to memory for the following instructions (See Instruction Summary included with Technical Data on CDP1802.)

1. ALU operations F0-F5, F7, 74, 75, 77;
2. output instructions 61 through 67;
3. input instructions 69 through 6F;
4. certain miscellaneous instructions – 70-73, 78.

The register designated by N(i.e., R(N)) points to memory for the "load D from memory" instructions 0N and 4N and the "Store D" instruction 5N. The register designated by P (i.e., the program counter) is used as the data pointer for ALU instructions (F8-FD, FF, 7C, 7D, 7F). During these instruction executions, the operation is referred to as "data immediate."

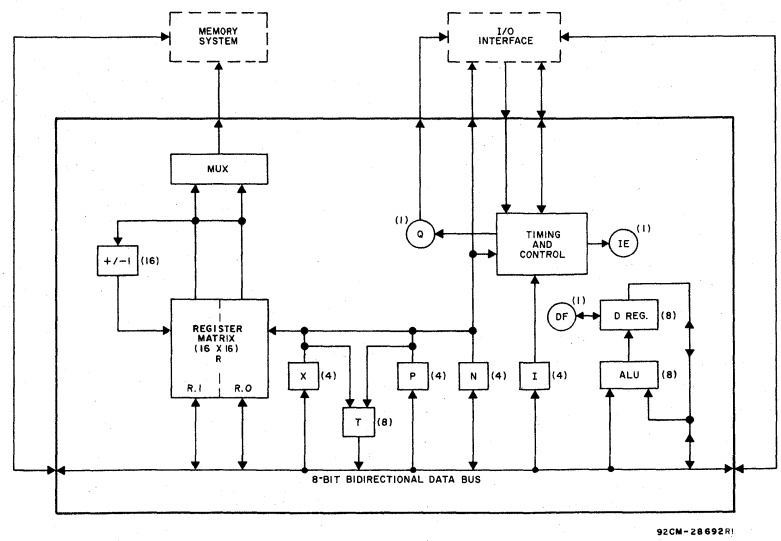


Fig. 27 – CDP1802 architecture.

General Operating and Application Considerations

Data Registers. When registers in R are used to store bytes of data, four instructions are provided (AN, BN, 8N, 9N) which allow D to receive from or write into either the higher-order to lower-order byte portions of the register designated by N. By this mechanism (together with loading by data immediate) program pointer and data pointer designations are initialized. Also, this technique allows scratchpad registers in R to be used to hold general data. By employing increment or decrement instructions, such registers may be used as loop counters.

DMA. Another important use of R as a data pointer supports the built-in Direct-Memory-Access (DMA) function. When a DMA-in or DMA-out request is received, the current instruction cycles is completed before anything happens. Upon entering the DMA state, the contents of R(O) are sent to memory to determine the address the data is written into (DMA-in) or read from (DMA-out). At the completion of each DMA cycle, which is one machine cycle, the contents of R(O) are incremented by 1 so that it points to the next memory cell. Thus, R(O) is a dedicated DMA data pointer; if the DMA feature is not used, R(O) is available for any other function. (Since the CDP1802 is a static machine and no refreshing is needed, there is no maximum number of DMA cycles that can be done consecutively.) This feature is the COSMAC architecture saves a substantial amount of logic when fast exchange of blocks of data are required, such as with magnetic disks or during CRT-display-refresh cycles.

Load Mode. A program load facility, using the DMA-In channel, is provided to enable users to load program into memory. This facility provides a simple, one-step means for initially entering programs into the microprocessor system and eliminates the requirement for specialized "bootstrap" programs.

Interrupt Servicing. Register R(1) is always used as the program counter when interrupt servicing is initiated. When an interis request comes in and the interrupt is allowed by the program (again, nothing takes place until the completion of the current instruction) the contents of the X and P registers are stored in the temporary register T, and X and P are set to new values: hex digit 2 in X and hex digit 1 in P. Interrupt enable is automatically deactivated to inhibit further interruptions. The user written interrupt routine is now in control; the contents of T are saved by means of a single instruction (78) in the memory location pointed to by R(X). At the conclusion of the interrupt, the return routine restores the pre-interrupted values of X and P with a single instruction (70 or 71). The interrupt-enable flip-flop can be activated to permit further interrupts or can be disabled to prevent them.

Accumulator. The D register is an 8-bit accumulator. Connected directly to the ALU, the D register provides one operand for any arithmetic or logic function. The second operand is found on the data bus from one of several sources. Results from the ALU's operation are then stored back into D, appropriately setting the 1-bit data flag register (DF). A series of branch, shift, and arithmetical instructions are provided for operations based on either the value of D or DF.

The Q Flip-Flop. An internal flip-flop, Q, can be set or reset by instruction and can be sensed by conditional branch instructions. The output of Q is also available as a bit serial output line.

Instruction Cycles. COSMAC instructions consist of two machine cycles, a fetch cycle and an execute cycle (except for CN instructions, which require two execute cycles). Each machine cycle is 8 clock pulses long. During the fetch cycle, the four bits in the P designator select one of the 16 registers R(P) as the current program counter. The selected register R(P) contains the address of the memory location from which the instruction is to be fetched. When the instruction is read out from the memory, the higher-order 4 bits of the instruction byte are loaded into the I register and the lower-order 4 bits into the N register. The content of the program counter is automatically incremented by 1 so that R(P) is now "pointing" to the next byte in the memory.

The X designator selects one of the 16 registers R(X) to "point" to memory for an operand (or data) in certain ALU or I/O operations.

The N designator can perform the following five functions depending on the type of instruction fetched:

1. designate one of the 16 registers in R to be acted upon during register operations;
2. select an input or output port for data transfer;
3. indicate the specific operation to be executed during the ALU instructions, types of test to be performed during the Branch instructions, etc.,
4. indicate the value to be loaded into P to designate a new register to be used as the program counter R(P);
5. indicate the value to be loaded into X to designate a new register to be used as data pointer R(X).

Supply-Voltage Levels. The internal voltage supply V_{DD} is isolated from the Input/Output voltage supply V_{CC} so that the processor may operate at high speed while interfacing with various external circuit technologies, including TTL at 5 volts. V_{CC} must be less than or equal to V_{DD}. All outputs swing from V_{SS} to V_{CC}. The recommended input voltage swings is V_{SS} to V_{CC}.

CDP1800-Series Memories (ROM's and RAM's)

The CDP1800 series offers various types of COS/MOS memories for use in microprocessor systems. Data memory is written into in the course of a program; therefore, it is implemented in a random access memory (RAM), a read/write memory that is volatile (i.e., it loses its data when the power supply is removed). Program memory, on the other hand, must usually be non-volatile and is not altered during normal microprocessor operation, so that program storage, in a production system, is normally a read-only memory (ROM). However, if the application allows or requires reloading of the program, the program may be stored in a RAM. This memory may also be used during initial development of a system, where frequent program changes are required. Another possible form of program storage is the programmable ROM (PROM), which may be used in prototype systems or in small-quantity production systems where a mask-programmed ROM is not economical.

The RCA CDP1800-series memories provide the following basic features:

- Low power consumption
- All fully static parts
- Single power supply
- Direct interfacing with 1800-series microprocessor systems
- 3-state outputs
- TTL drive capability
- Small MOQ on custom ROM patterns

- Industry standard pin-outs
- Different parts designed for small, medium, or large memory systems

CDP1800-Series I/O Circuits

The input/output, or I/O, portion of the microprocessor provides information as words on the data bus with additional controls available separately. The I/O electronics is responsible for interfacing these signals with whatever input/output devices the system uses. Broadly, the the functions of the I/O electronics include synchronization of data transfer, selection and activation of one of a number of I/O devices, and the formating of data so that it is compatible with the device selected. The functions available on the control lines have a marked effect on the complexity of the I/O electronics. The I/O electronics may also be required to do logic-level conversion as part of the interfacing function if this facility is not provided within the microprocessor itself.

The following basic features are typical of RCA CDP1800-series COS/MOS I/O circuits.

- 4 CPU-tested flag inputs (EF) for slowly varying binary inputs or for I/O-to-CPU signalling
- Interrupt request; maskable for flexibility
- 2 DMA request lines, In and Out, with Memory pointer and control logic on the CDP1802
- 2 state-code output lines to tell I/O devices what the CPU is doing
- Programmable output bit Q
- 3 I/O command lines (N) for programmed control of memory-I/O transfer
- Memory data strobe (TPB) for clean and easy capture of data by I/O device

COS/MOS High-Voltage B-Series Integrated Circuits

Technical Data

COS/MOS NOR Gates

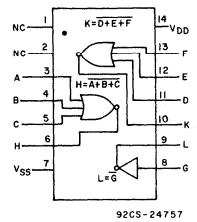
High-Voltage Types (20-Volt Rating)
Dual 3 Input
plus Inverter – CD4000B
Quad 2 Input – CD4001B
Dual 4 Input – CD4002B
Triple 3 Input – CD4025B

RCA-CD4000B, CD4001B, CD4002B, and CD4025B NOR gates provide the system designer with direct implementation of the NOR function and supplement the existing family of COS/MOS gates. All inputs and outputs are buffered.

The CD4000B, CD4001B, CD4002B, and CD4025B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

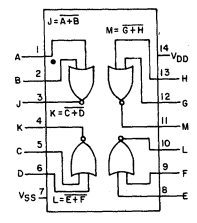
Features:

- **Propagation delay time = 60 ns (typ.) at C_L = 50 pF, V_{DD} = 10 V**
- **Buffered inputs and outputs**
- **Standardized symmetrical output characteristics**
- **100% tested for maximum quiescent current at 20 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (over full package temperature range):**
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- **Meets all requirements of JEDEC Tentative Standard No.13A, "Standard Specifications for Description of "B" Series CMOS Devices"**



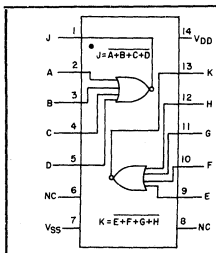
92CS-24757

CD4000B
FUNCTIONAL DIAGRAM



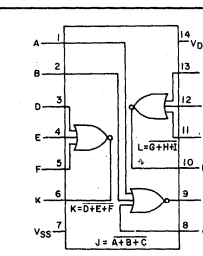
92CS-24762

CD4001B
FUNCTIONAL DIAGRAM



92CS-24758

CD4002B
FUNCTIONAL DIAGRAM



92CS-24760

CD4025B
FUNCTIONAL DIAGRAM

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				—	—	1.5	V
	1,9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5	–	5	3.5				3.5	—	—	
	1	–	10	7				7	—	—	
	1.5	–	15	11				11	—	—	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200kΩ

CHARACTERISTIC	TEST CONDITIONS		ALL TYPES LIMITS		UNITS
		V_{DD} VOLTS	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH}		5	125	250	ns
		10	60	120	
		15	45	90	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input		5	7.5	pF

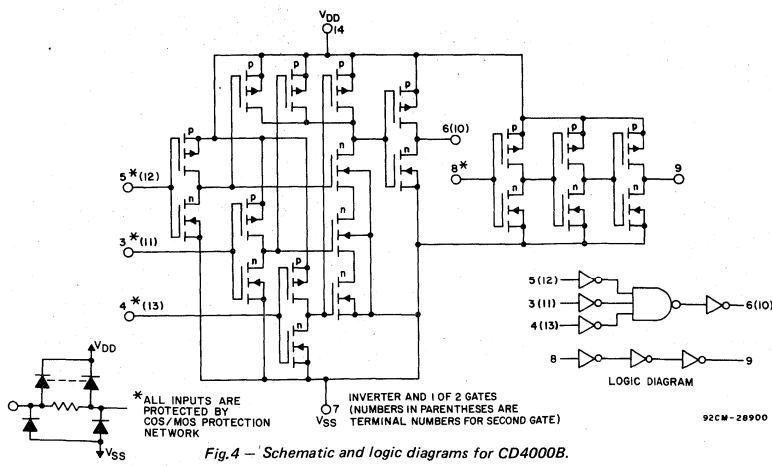


Fig.4 — Schematic and logic diagrams for CD4000B.

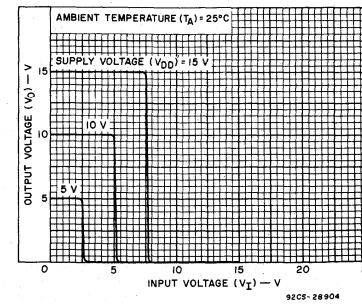


Fig.1 — Typical voltage transfer characteristics.

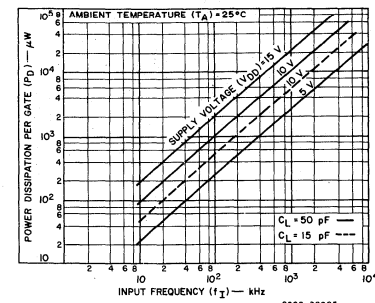


Fig.2 — Typical power dissipation vs. frequency.

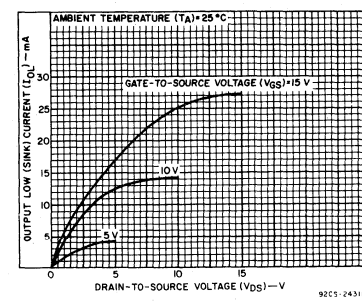


Fig.3 — Typical output low (sink) current characteristics.

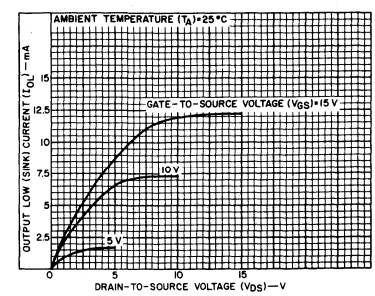


Fig.5 — Minimum output low (sink) current characteristics.

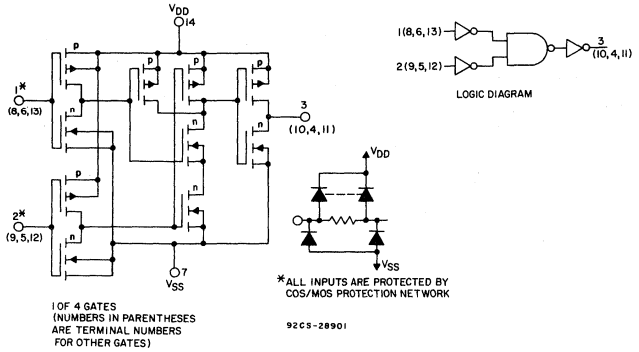


Fig.6 – Schematic and logic diagrams for CD4001B.

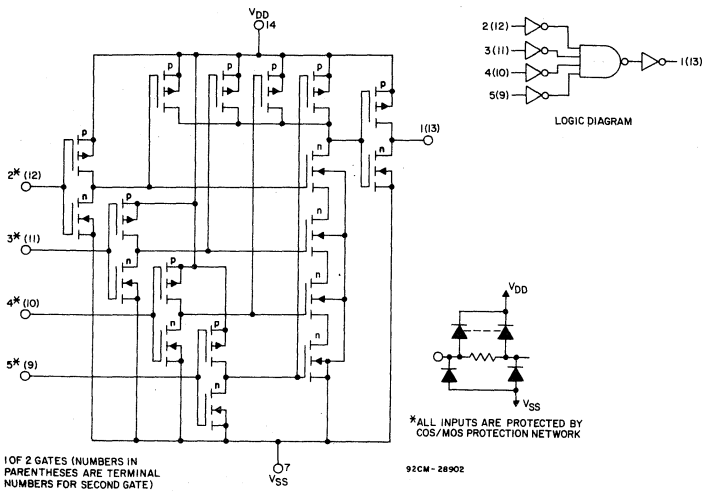


Fig.7 – Schematic and logic diagrams for CD4002B.

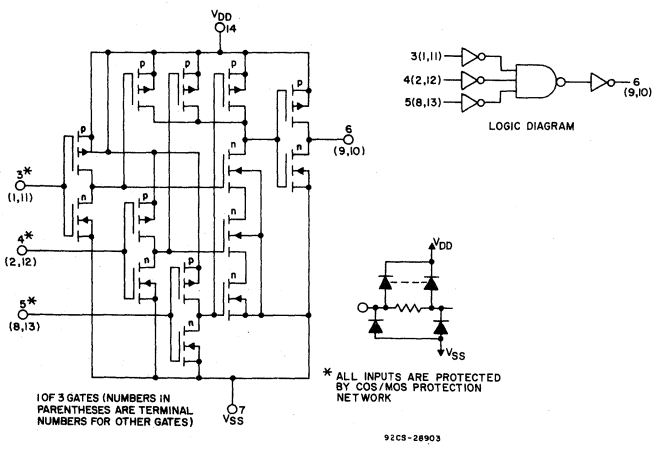


Fig.8 – Schematic and logic diagrams for CD4025B.

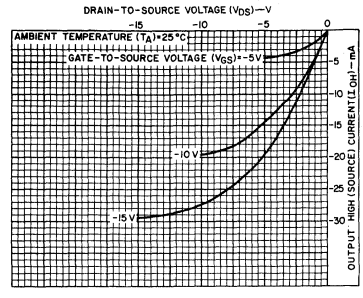


Fig.9 – Typical output high (source) current characteristics.

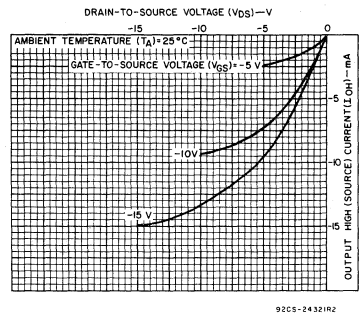


Fig.10 – Minimum output high (source) current characteristics.

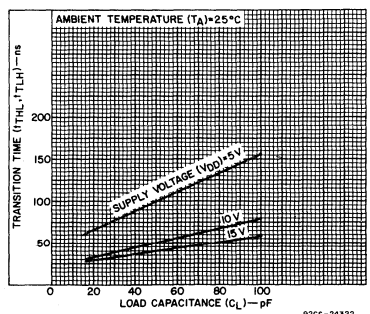


Fig.11 – Typical transition time vs. load capacitance.

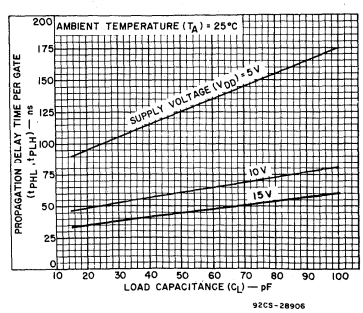


Fig.12 – Typical propagation delay time vs. load capacitance.

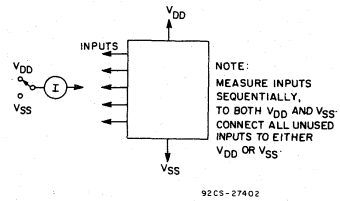


Fig. 13 – Input leakage current test circuit.

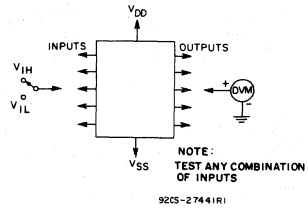


Fig. 14 – Input-voltage test circuit.

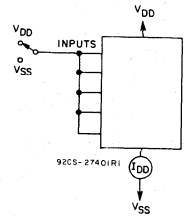
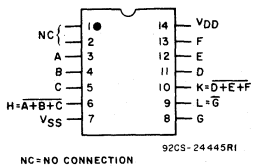
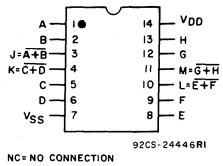


Fig. 15 – Quiescent-device current test circuit.

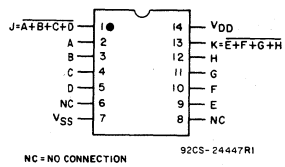
TERMINAL ASSIGNMENTS (TOP VIEW)



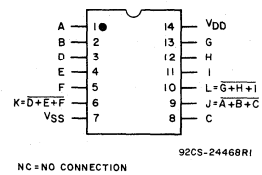
CD4000B



CD4001B

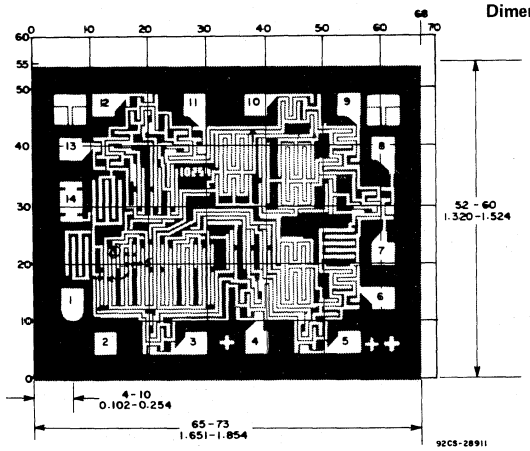


CD4002B



CD4025B

CHIP PHOTOGRAPHS
Dimensions and Pad Layouts



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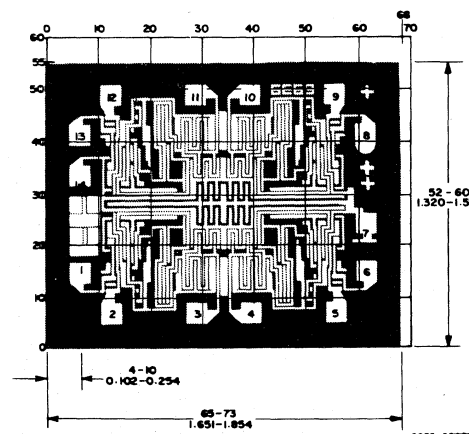

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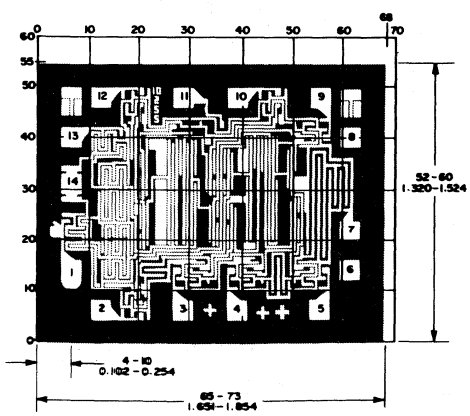
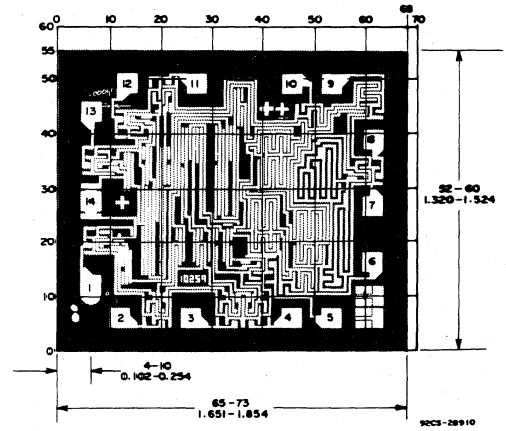


CD4002B



CD4025B

COS/MOS NOR Gates

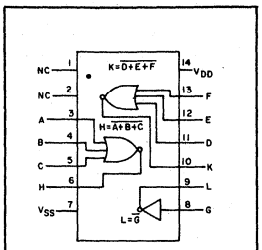
High-Voltage Types (20-Volt Rating)
Dual 3 Input plus Inverter—CD4000UB
Quad 2 Input-CD4001UB
Dual 4 Input—CD4002UB
Triple 3 Input—CD4025UB

RCA-CD4000UB, CD4001UB, CD4002UB, and CD4025UB NOR gates provide the system designer with direct implementation of the NOR function and supplement the existing family of COS/MOS gates.

The CD4000UB, CD4001UB, CD4002UB, and CD4025UB types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

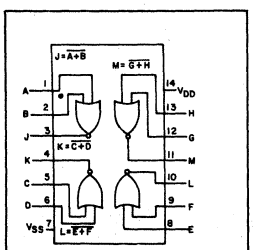
Features:

- Propagation delay time = 30 ns (typ.) at C_L = 50 pF, V_{DD} = 10 V
- Standardized symmetrical output characteristics
- 100% tested for maximum quiescent current at 20 V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings



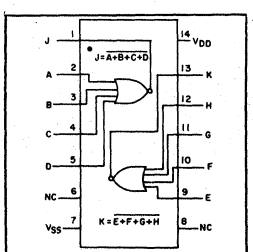
92CS-24757

CD4000UB FUNCTIONAL DIAGRAM



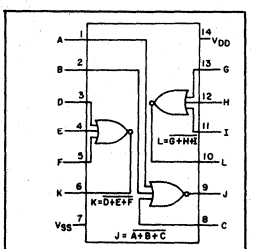
92CS-24762

CD4001UB FUNCTIONAL DIAGRAM



92CS-24758

CD4002UB FUNCTIONAL DIAGRAM



92CS-24760

CD4025UB FUNCTIONAL DIAGRAM

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1				–	–	1	V
	1, 9	–	10	2				–	–	2	
	1.5,13.5	–	15	2.5				–	–	2.5	
Input High Voltage, V_{IH} Min.	0.5	–	5	4				4	–	–	
	1	–	10	8				8	–	–	
	1.5	–	15	12.5				12.5	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . –0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = –40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K). . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
PACKAGE TYPE E . . . . . –40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, and C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC	TEST CONDITIONS		ALL TYPES LIMITS		UNITS
		V_{DD} Volts	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH}		5	60	120	ns
		10	30	60	
		15	25	50	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input		10	15	pF

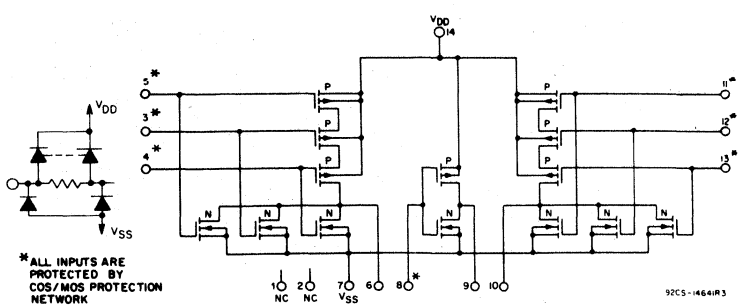


Fig. 4 – Schematic diagram for type CD4000UB.

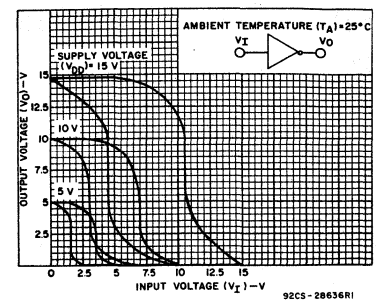


Fig. 1 – Minimum and maximum voltage transfer characteristics.

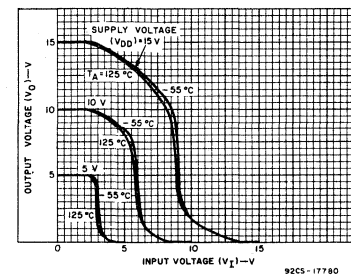


Fig. 2 – Typical voltage transfer characteristics as a function of temperature.

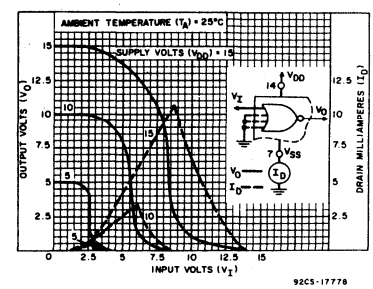


Fig. 3 – Typical current & voltage transfer characteristics.

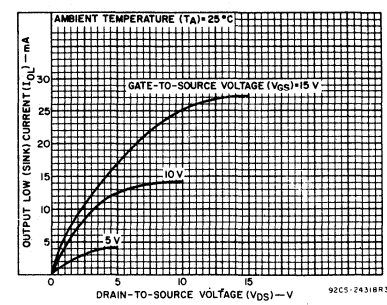


Fig. 5 – Typical output low (sink) current characteristics.

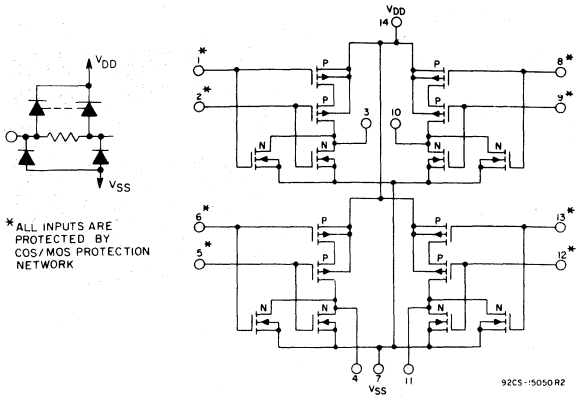


Fig. 6 – Schematic diagram for type CD4001UB.

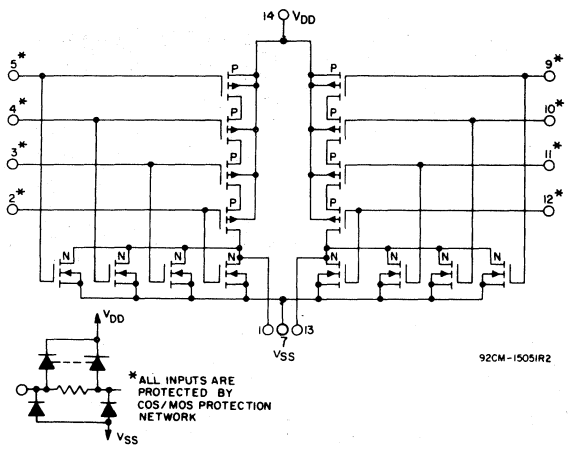


Fig. 7 – Schematic diagram for type CD4002UB.

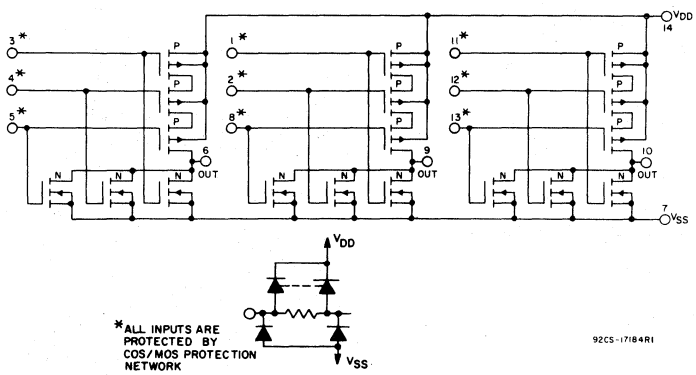


Fig. 8 – Schematic diagram for type CD4025UB.

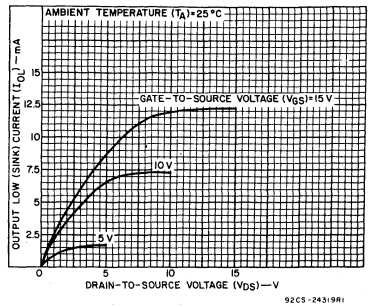


Fig. 9 – Minimum output low (sink) current characteristics.

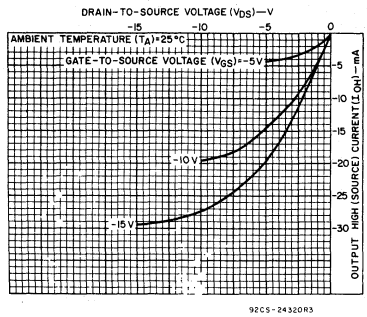


Fig. 10 – Typical output high (source) current characteristics.

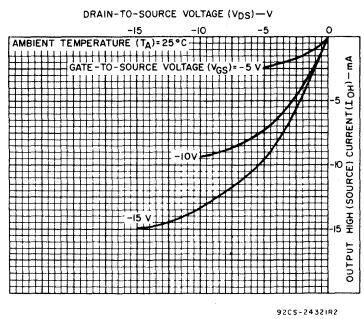


Fig. 11 – Minimum output high (source) current characteristics.

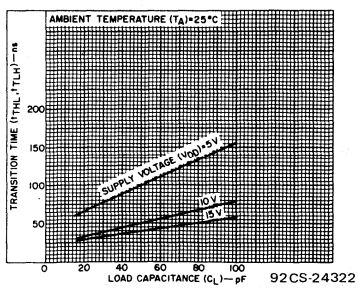


Fig. 12 – Typical transition time vs. load capacitance.

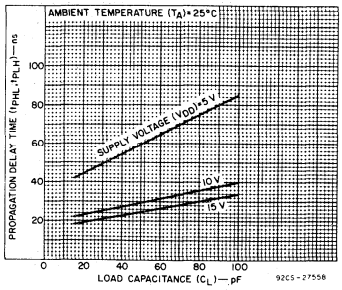


Fig. 13 – Typical propagation delay time vs. load capacitance.

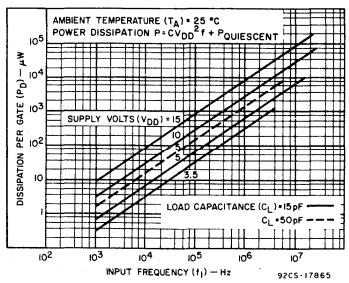


Fig. 14 – Typical power dissipation vs. frequency.

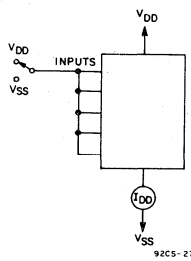


Fig. 15 – Quiescent-device-current test circuit.

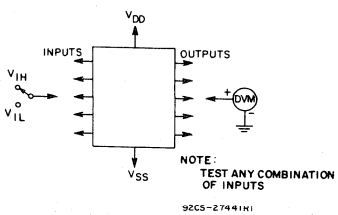


Fig. 16 – Input-voltage test circuit.

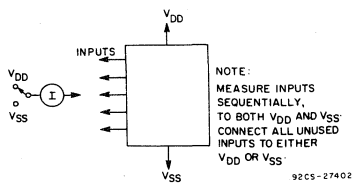
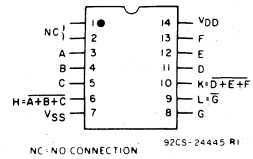
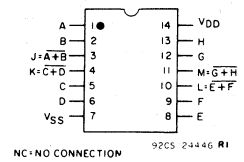


Fig. 17 – Input leakage current test circuit.

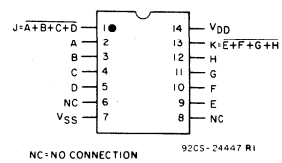
TERMINAL ASSIGNMENTS



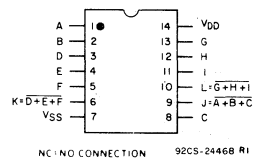
CD4000UB



CD4001UB

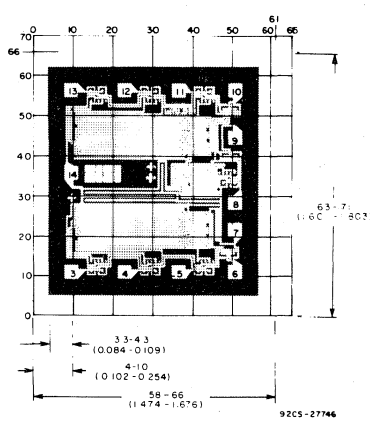


CD4002UB

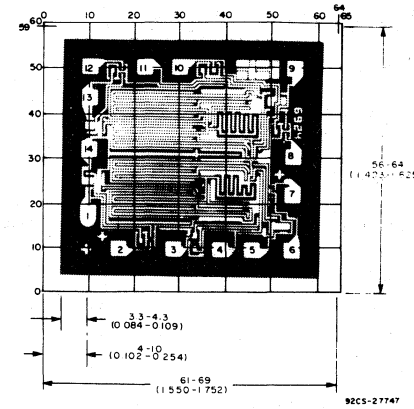


CD4025UB

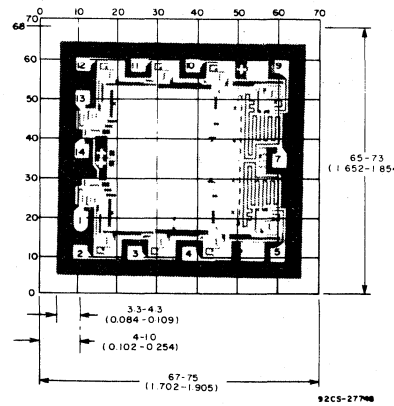
CHIP PHOTOGRAPHS
Dimensions and Pad Layouts



CD4000UB



CD4001UB



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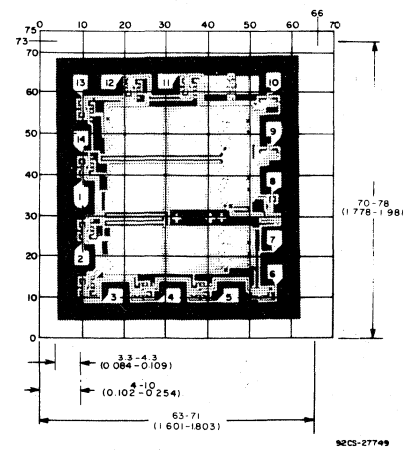


CD4025UB

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS 18-Stage Static Shift Register

High-Voltage Types (20-Volt Rating)

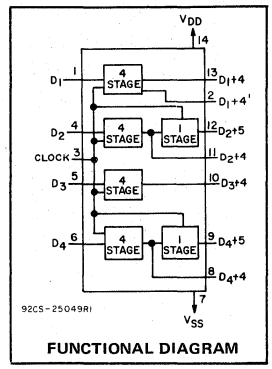
Preliminary Data

Features:

- Fully static operation
- Shifting rates up to 12 MHz @ 10 V (typ.)
- Permanent register storage with clock line high or low — no information recirculation required
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Serial shift registers
- Time delay circuits
- Frequency division



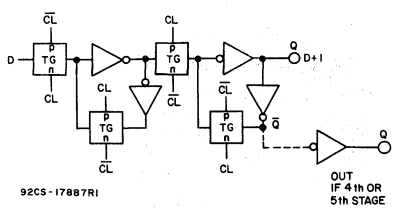
FUNCTIONAL DIAGRAM

The RCA-CD4006B types are composed of 4 separate shift register sections: two sections of four stages and two sections of five stages with an output tap at the fourth stage. Each section has an independent single-rail data path.

A common clock signal is used for all stages. Data are shifted to the next stage on negative-going transitions of the clock. Through appropriate connections of inputs and outputs, multiple register sections of 4, 5, 8, and 9 stages or single register sections of 10, 12, 13, 14, 16, 17 and 18 stages can be implemented using one CD4006B package. Longer shift register sections can be assembled by using more than one CD4006B.

To facilitate cascading stages when clock rise and fall times are slow, an optional output (D_1+4') that is delayed one-half clock-cycle, is provided (see Truth Table for Output from Term. 2).

The CD4006B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).



TRUTH TABLE FOR OUTPUT FROM TERM.2

D_1+4	CL▲	D_1+4'
0	⎍	0
1	⎍	1
X	⎎	NC

TRUTH TABLE FOR SHIFT REGISTER STAGE

D	CL▲	D + 1
0	⎎	0
1	⎎	1
X	⎍	NC

1 = HIGH
0 = LOW
NC = NO CHANGE
X = DON'T CARE
▲ = LEVEL CHANGE

Fig. 1 — Logic diagram and truth table (one register stage).

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
									+25		
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	-	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

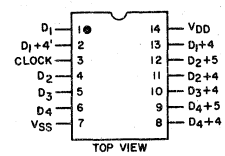
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

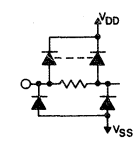
DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ*

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	TYPICAL VALUES	UNITS
Propagation Delay Time, t_{PHL}, t_{PLH}	5	200	ns
	10	100	
	15	80	
Transition Time, t_{THL}, t_{TLH}	5	100	ns
	10	50	
	15	40	
Minimum Data Setup Time, t_S	5	50	ns
	10	25	
	15	20	
Minimum Clock Pulse Width, t_W	5	100	ns
	10	45	
	15	30	
Maximum Clock Input Frequency, f_{CL}	5	5	MHz
	10	12	
	15	16	
Maximum Clock Input Rise or Fall Time t_rCL, t_fCL*	5	15	μs
	10	15	
	15	15	
Input Capacitance, C_{IN}	Any Input	5	pF

* If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.



TERMINAL ASSIGNMENT



ALL INPUTS (TERMINALS 1,3,4,5,6) PROTECTED BY COS/MOS PROTECTION NETWORK

92CS-28974

COS/MOS Dual Complementary Pair Plus Inverter

High-Voltage Types (20-Volt Rating)

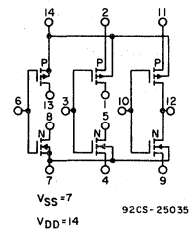
The RCA-CD4007UB types are comprised of three n-channel and three p-channel enhancement-type MOS transistors. The transistor elements are accessible through the package terminals to provide a convenient means for constructing the various typical circuits as shown in Fig. 2.

More complex functions are possible using multiple packages. Numbers shown in parentheses indicate terminals that are connected together to form the various configurations listed.

The CD4007UB types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- Standardized symmetrical output characteristics
- Medium Speed Operation – t_{PHL}, t_{PLH} = 30 ns (typ.) at 10 V
- 100% tested for quiescent current at 20 V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C



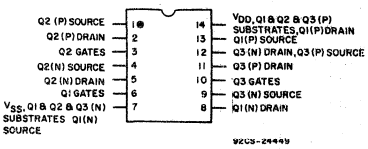
Terminal No.14 – V_{DD}
Terminal No. 7 – V_{SS}

FUNCTIONAL DIAGRAM

Applications:

- Extremely high-input impedance amplifiers
- Shapers
- Inverters
- Threshold detector
- Linear amplifiers
- Crystal oscillators

TERMINAL DIAGRAM
Top View



RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D,K,F,H Packages Values at –40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	–40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	4.5	–	5	1				—	—	1	V
	9	–	10	2				—	—	2	
	13.5	–	15	2.5				—	—	2.5	
Input High Voltage, V_{IH} Min.	0.5	–	5	4				4	—	—	
	1	–	10	8				8	—	—	
	1.5	–	15	12.5				12.5	—	—	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC		CONDITIONS	ALL TYPES LIMITS		UNITS
		V_{DD} Volts	Typ.	Max.	
Propagation Delay Time:		5	55	110	ns
	t_{PHL}, t_{PLH}	10	30	60	
		15	25	50	
Transition Time		5	100	200	ns
	t_{THL}, t_{TLH}	10	50	100	
		15	40	80	
Input Capacitance	C_{IN}	Any Input	10	15	pF

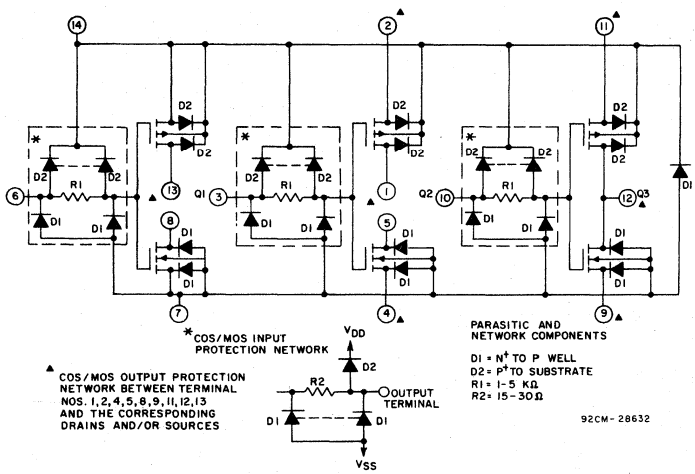
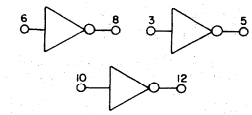


Fig. 1 – Detailed schematic diagram of CD4007UB showing input, output, and parasitic diodes.

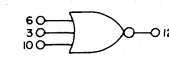
a) Triple Inverters



(14,2,11); (8,13); (1,5); (7,4,9)

92CS-15350

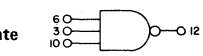
b) 3-Input NOR Gate



92CS-15349

(13,2); (1,11); (12,5,8); (7,4,9)

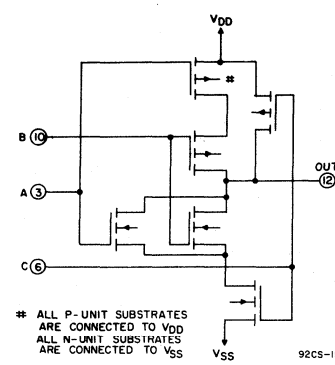
c) 3-Input NAND Gate

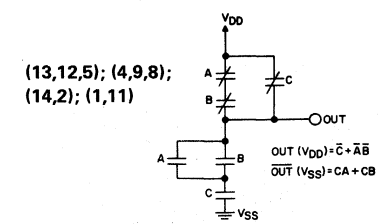


92CS-15348

(1,12,13); (2,14,11); (4,8); (5,9)

d) Tree (Relay) Logic

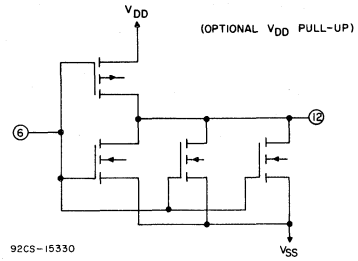




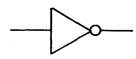
(13,12,5); (4,9,8); (14,2); (1,11)

Fig. 2 – Sample COS/MOS logic circuit arrangements using type CD4007UB.

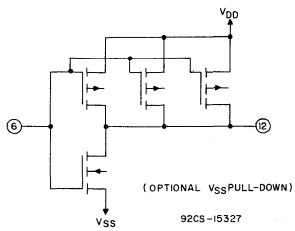
e) High Sink-Current Driver



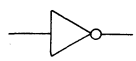
(6,3,10); (8.5, 12); (11,14); 7,4,9)



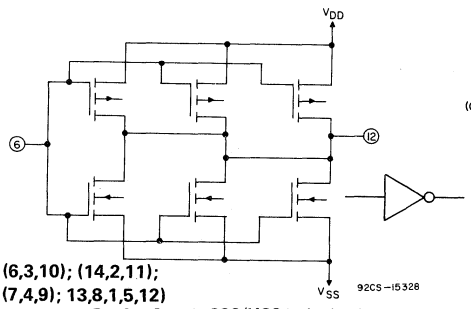
f) High Source-Current Driver



(6,3,10); (13,1,12); (14,2,11); (7,9)

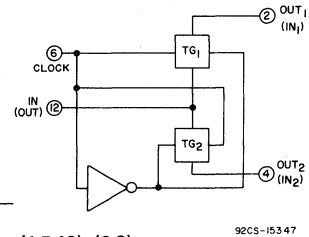


g) High Sink - and Source-Current Driver



(6,3,10); (14,2,11); (7,4,9); 13,8,1,5,12)

h) Dual Bi-Directional Transmission Gating



(1,5,12); (2,9); (11,4); (8,13,10); (6,3)

Fig. 2 – Sample COS/MOS logic circuit arrangements using type CD4007UB (Cont'd).

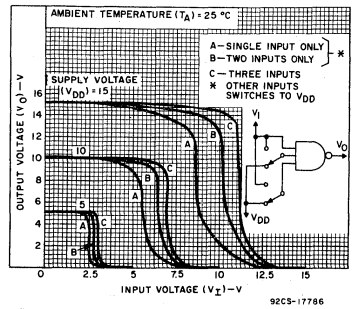


Fig. 3 – Typical voltage-transfer characteristics for NAND gate.

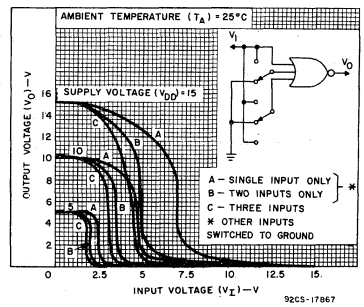


Fig. 4 – Typical voltage-transfer characteristics for NOR gate.

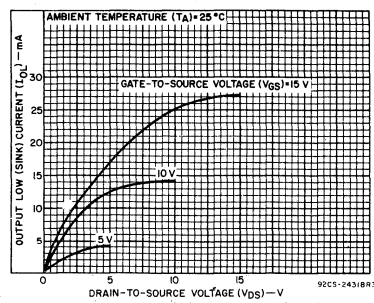


Fig. 5 – Typical output low (sink) current characteristics.

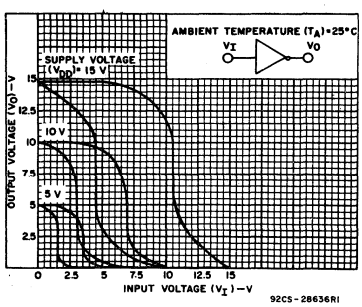


Fig. 6 – Minimum and maximum voltage-transfer characteristics for inverter.

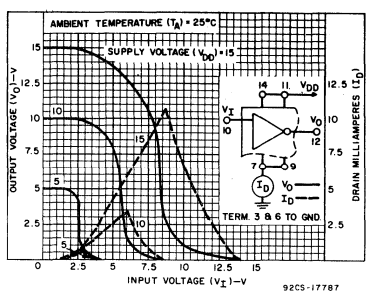


Fig. 7 – Typical current and voltage-transfer characteristics for inverter.

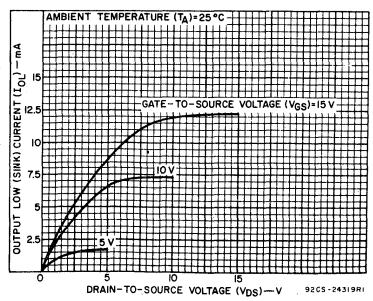


Fig. 8 – Minimum output low (sink) current characteristics.

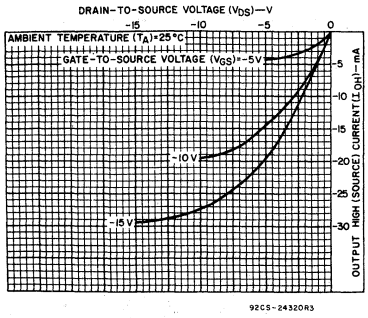


Fig. 9 – Typical output high (source) current characteristics.

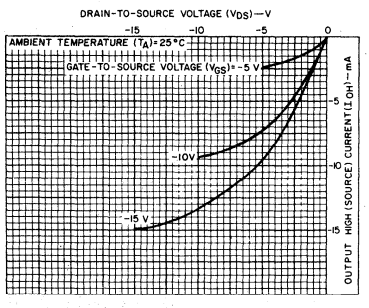


Fig. 10 – Minimum output high (source) current characteristics.

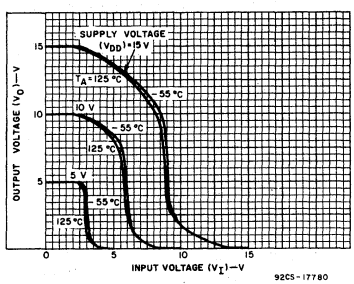


Fig. 11 – Typical voltage-transfer characteristics as a function of temperature.

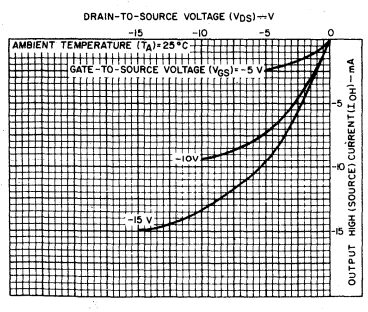


Fig. 12 – Typical propagation delay time vs. load capacitance.

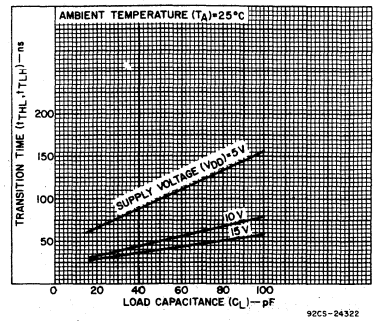


Fig. 13 – Typical transition time vs. load capacitance.

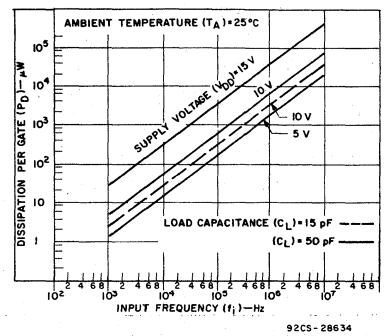


Fig. 14 – Typical dissipation vs. frequency characteristics.

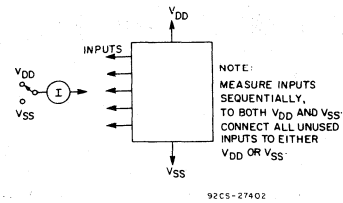


Fig. 15 – Input current test circuit.

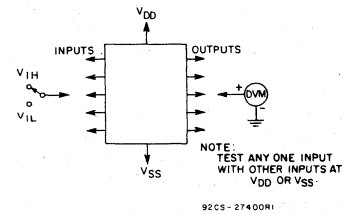


Fig. 16 – Input voltage test circuit.

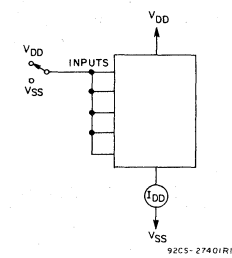
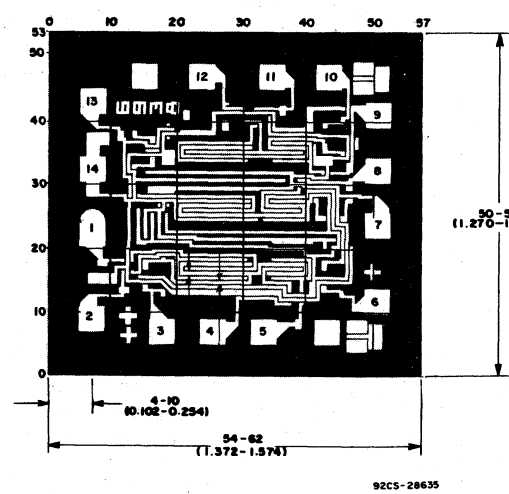


Fig. 17 – Quiescent device current test circuit.



DIMENSIONS AND PAD LAYOUT FOR CD4007UBH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS 4-Bit Full Adder

With Parallel Carry Out

High-Voltage Types (20-Volt Rating)

The RCA-CD4008B types consist of four full adder stages with fast look ahead carry provision from stage to stage. Circuitry is included to provide a fast "parallel-carry-out" but to permit high-speed operation in arithmetic sections using several CD4008B's.

CD4008B inputs include the four sets of bits to be added, A_1 to A_4 and B_1 to B_4, in addition to the "Carry In" bit from a previous section. CD4008B outputs include the four sum bits, S_1 to S_4. In addition to the high speed "parallel-carry-out" which may be utilized at a succeeding CD4008B section.

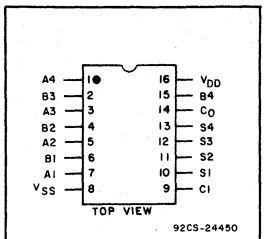
The CD4008B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **4 sum outputs plus parallel look-ahead carry-output**
- **High-speed operation — sum in-to-sum out, 100 ns typ; carry in-to-carry out, 55 ns typ. at V_{DD} = 10 V, C_L = 50 pF**
- **Standardized, symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (over full package temperature range): 1 V at V_{DD} = 5 V, 2 V at V_{DD} = 10 V, 2.5 V at V_{DD} = 15 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

- **Binary addition/arithmetic units**



CD4008B
TERMINAL ASSIGNMENT

TRUTH TABLE

A_i	B_i	C_i	C_0	SUM
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
									+25		
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

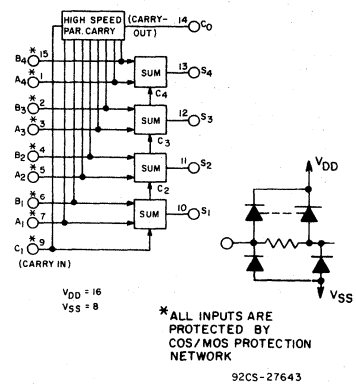


Fig.1 — CD4008B logic diagram.

RECOMMENDED OPERATING CONDITIONS *at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:*

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . –0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = –40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
PACKAGE TYPE E . . . . . –40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS
At T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200kΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS ALL TYPES		UNITS
		TYP.	MAX.	
Propagation Delay Time: t_{PHL}, t_{PLH}	5	400	800	ns
Sum In to Sum Out	10	160	320	
	15	115	230	
Carry In to Sum Out	5	370	740	ns
	10	155	310	
	15	115	230	
Sum In to Carry Out	5	200	400	ns
	10	90	180	
	15	65	130	
Carry In to Carry Out	5	100	200	ns
	10	50	100	
	15	40	80	
Transition Time: t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Input Capacitance, C_{IN}	–	5	7.5	pF

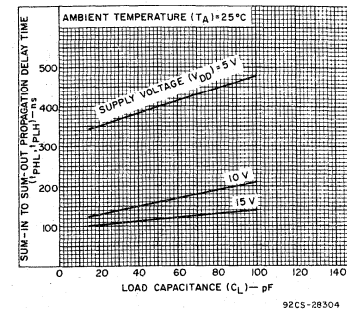


Fig.2 – Typical sum-in to sum-out propagation delay time vs. load capacitance.

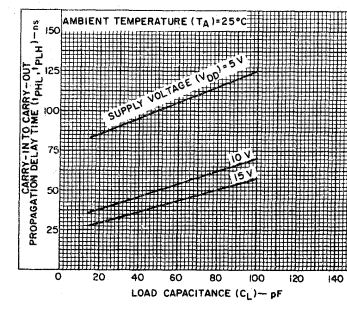


Fig.3 – Typical carry-in to carry-out propagation delay time vs. load capacitance.

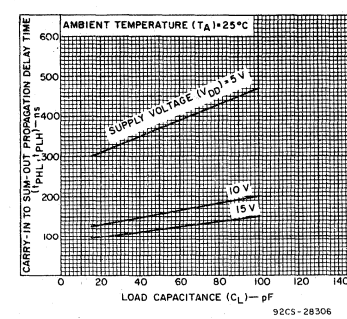


Fig.4 – Typical carry-in to sum-out propagation delay time vs. load capacitance.

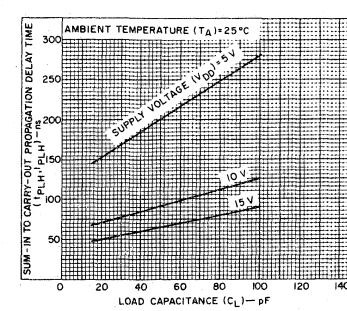


Fig.5 – Typical sum-in to carry-out propagation delay time vs. load capacitance.

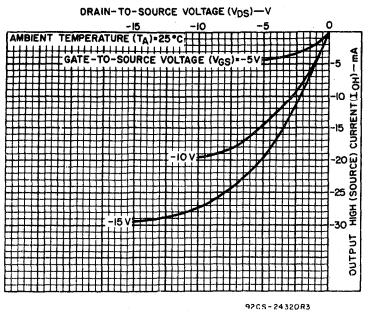


Fig.6 – Typical output high (source) current characteristics.

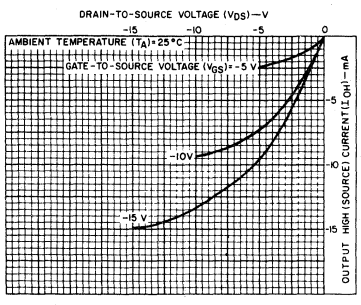


Fig.7 – Minimum output high (source) current characteristics.

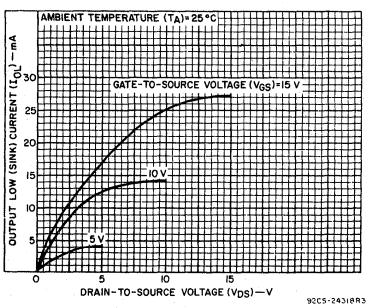


Fig.8 – Typical output low (sink) current characteristics.

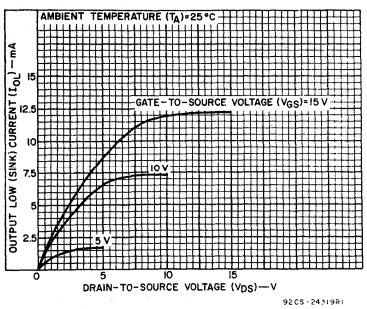


Fig.9 – Minimum output low (sink) current characteristics.

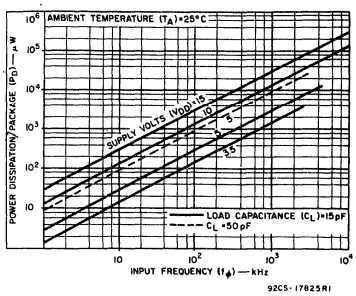


Fig.10 – Typical dissipation characteristics.

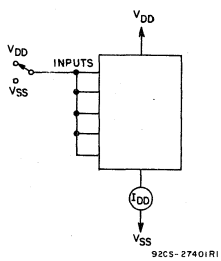


Fig.11 – Quiescent-device-current test circuit.

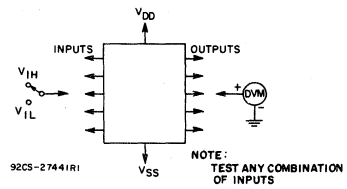


Fig.12 – Input-voltage test circuit.

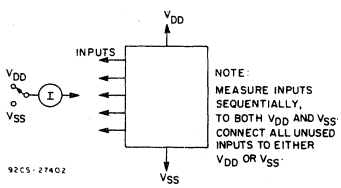
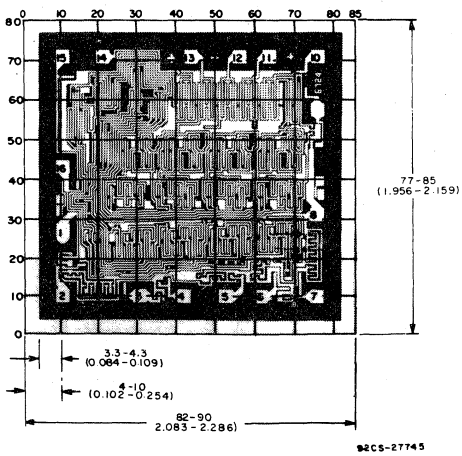


Fig.13 – Input current test circuit.

Dimensions and Pad Layout for CD4008BH



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS
Hex Buffers/Converters

High-Voltage Types (20-Volt Rating)

Inverting Type: CD4009UB
Non-Inverting Type: CD4010B

The RCA-CD4009UB and CD4010B Hex Buffer/Converters may be used as COS/MOS to TTL or DTL logic-level converters or COS/MOS high-sink-current drivers.

The CD4049UB and CD4050B are preferred hex buffer replacements for the CD4009UB and CD4010B, respectively, in all applications except multiplexers. For applications not requiring high sink current or voltage conversion, the CD4069UB Hex Inverter is recommended.

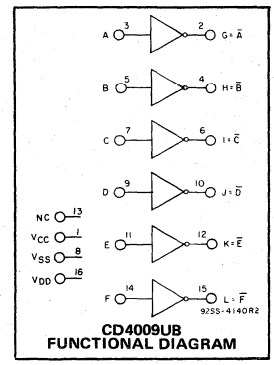
The CD4009UB and CD4010B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packs (K suffix), and in chip form (H suffix).

Features:

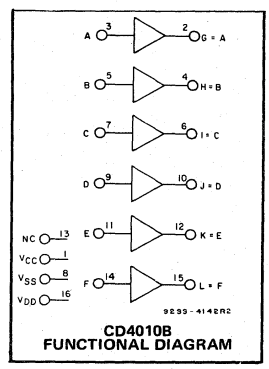
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings

Applications:

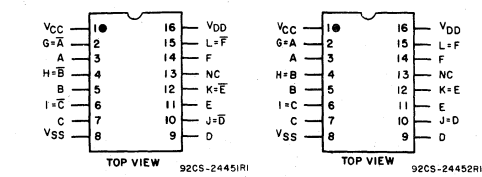
- COS/MOS to DTL/TTL hex converter
- COS/MOS current "sink" or "source" driver
- COS/MOS high-to-low logic-level converter
- Multiplexer – 1 to 6 or 6 to 1



CD4009UB
FUNCTIONAL DIAGRAM



CD4010B
FUNCTIONAL DIAGRAM



TERMINAL ASSIGNMENTS

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}, V_{CC}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

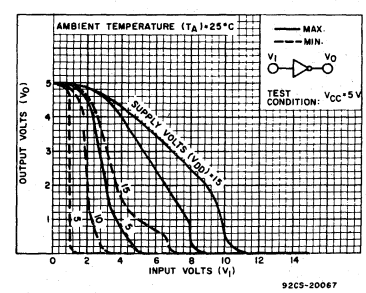


Fig. 1 – Minimum and maximum voltage transfer characteristics–CD4009UB.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range), V_{DD}	3	18	V
V_{CC}*	3	V_{DD}	
Input Voltage Range (V_I)	V_{CC}*	V_{DD}	V

*The CD4009UB and CD4010B have high-to-low level voltage conversion capability but not low-to-high level, therefore it is recommended that $V_{DD} \geq V_I \geq V_{CC}$.

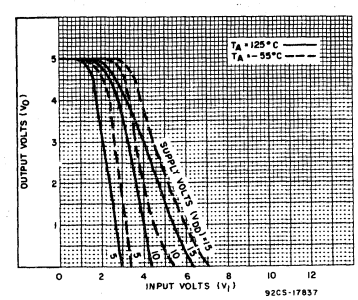


Fig. 2 – Typical voltage transfer characteristics as function of temp.–CD4009UB.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55,+25,+125 Apply to D,K,F,H Pkgs. Values at −40,+25,+85 Apply to E Pkgs.							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

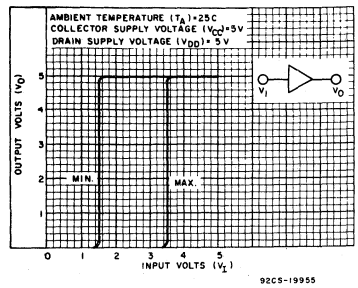


Fig. 3 – Minimum and maximum voltage transfer characteristics (V_{DD}=5)–CD4010B.

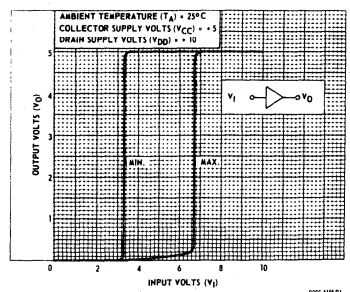


Fig. 4 – Minimum and maximum voltage transfer characteristics (V_{DD}=10)–CD4010B.

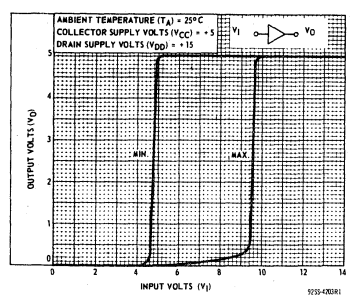


Fig. 5 – Minimum and maximum voltage transfer characteristics (V_{DD}=15)–CD4010B.

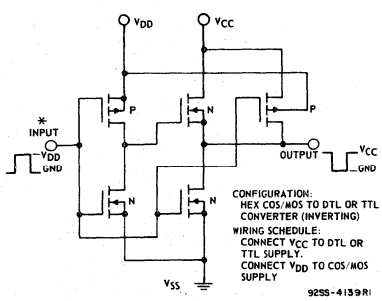
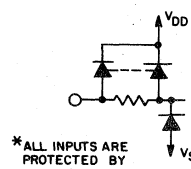


Fig. 6 – Schematic diagram of CD4009UB– 1 of 6 identical stages.



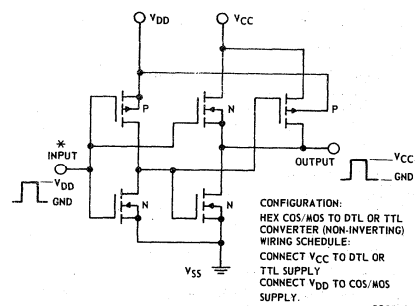


Fig. 7 – Schematic diagram of CD4010B– 1 of 6 identical stages.

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A=25°C; Input t_r, t_f=20 ns, C_L=50 pF, R_L=200 KΩ*

CHARACTERISTIC	CONDITIONS V_{DD} (V)	V_I (V)	V_{CC} (V)	LIMITS ALL PKGS TYP.	MAX.	UNIT
Propagation Delay Time: Low-to-High, t_{PLH}	5	5	5	70	140	
	10	10	10	40	80	
CD4009UB	10	10	5	35	70	ns
	15	15	15	30	60	
	15	15	5	30	60	
	5	5	5	100	200	
	10	10	10	50	100	
CD4010B	10	10	5	50	100	ns
	15	15	15	35	70	
	15	15	5	35	70	
High-to-Low, t_{PHL}	5	5	5	30	60	
	10	10	10	20	40	
CD4009UB	10	10	5	15	30	ns
	15	15	15	15	30	
	15	15	5	10	20	
	5	5	5	65	130	
	10	10	10	35	70	
CD4010B	10	10	5	30	70	ns
	15	15	15	25	50	
	15	15	5	20	40	
Transition Time: Low-to-High, t_{TLH}	5	5	5	150	350	
	10	10	10	75	150	ns
	15	15	15	55	110	
High-to-Low, t_{THL}	5	5	5	35	70	
	10	10	10	20	40	ns
	15	15	15	15	30	
Input Capacitance, C_{IN} CD4009UB	–	–	–	15	22.5	pF
CD4010B	–	–	–	5	7.5	

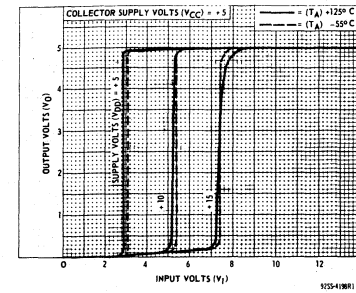


Fig. 8 – Typical voltage transfer characteristics as a function of temperature–CD4010B.

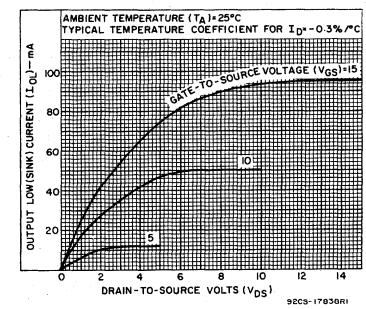


Fig. 9 – Typical output low (sink) current characteristics.

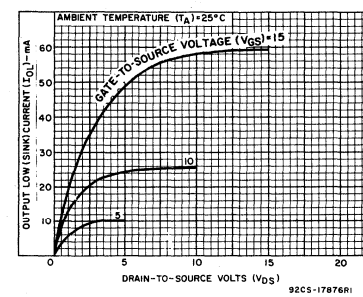


Fig. 10 – Minimum output low (sink) current characteristics.

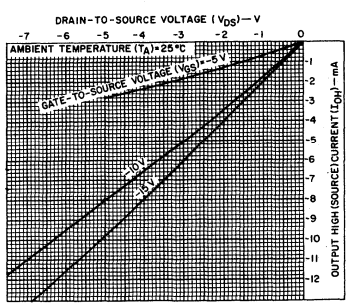


Fig. 11 – Typical output high (source) current characteristics.

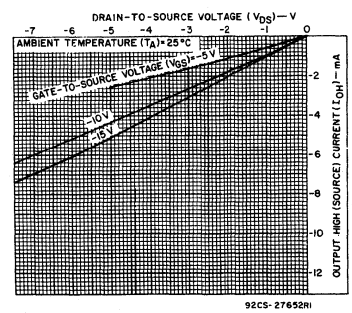


Fig. 12 – Minimum output high (source) current characteristics.

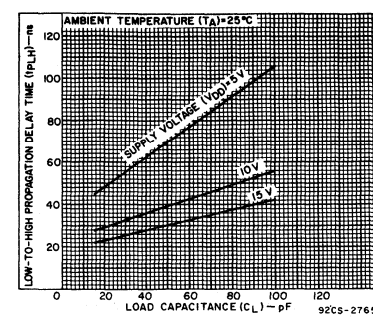


Fig. 13 – Typical low-to-high propagation delay time vs. load capacitance (CD4009UB).

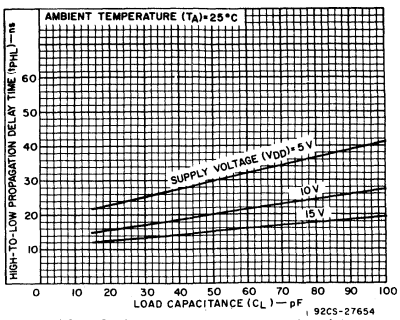


Fig. 14 — Typical high-to-low propagation delay time vs. load capacitance (CD4009UB).

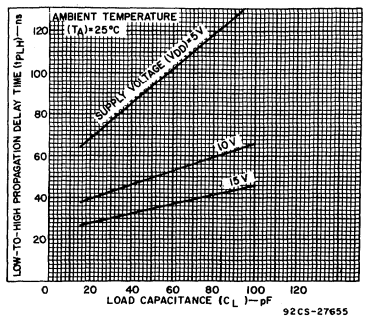


Fig. 15 — Typical low-to-high propagation delay time vs. load capacitance (CD4010B).

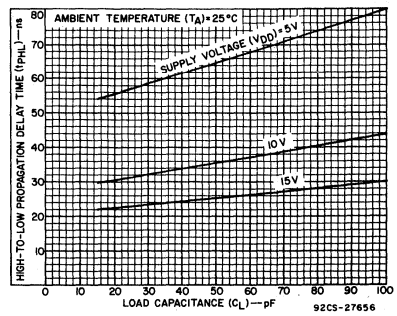


Fig. 16 — Typical high-to-low propagation delay time vs. load capacitance (CD4010B).

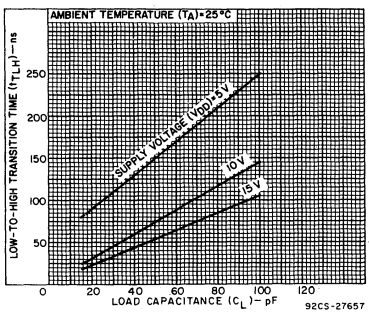


Fig. 17 — Typical low-to-high transition time vs. load capacitance.

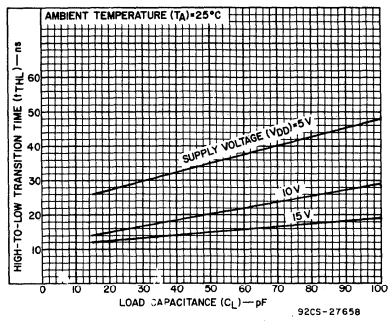


Fig. 18 — Typical high-to-low transition time vs. load capacitance.

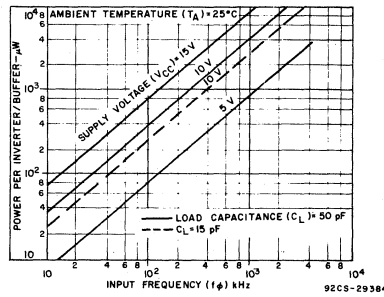


Fig. 19 — Typical dissipation characteristics.

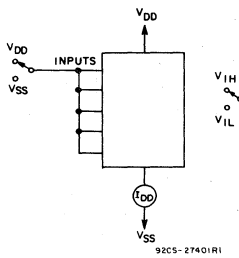


Fig. 20 — Quiescent device current test circuit.

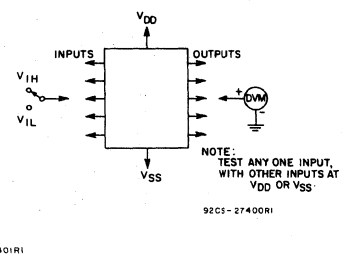


Fig. 21 — Noise immunity test circuit.

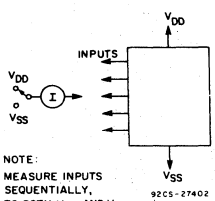
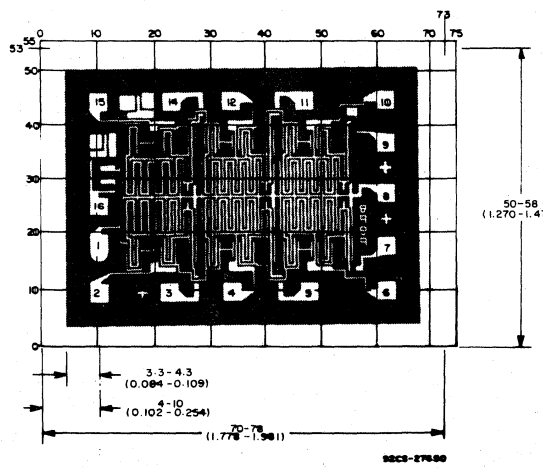


Fig. 22 — Input current test circuit.



Photograph of chip for CD4009UB. Dimensions and pad layout for CD4010B are identical.

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid Graduations Are In Mils (10^{-3} Inch)

COS/MOS NAND Gates

High-Voltage Types (20-Volt Rating)

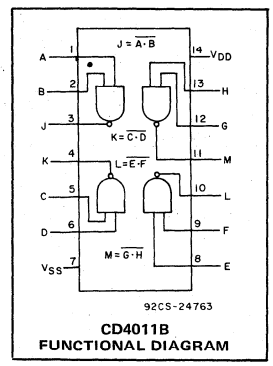
Quad 2 Input – CD4011B
Dual 4 Input – CD4012B
Triple 3 Input – CD4023B

RCA-CD4011B, CD4012B, and CD4023B NAND gates provide the system designer with direct implementation of the NAND function and supplement the existing family of COS/MOS gates. All inputs and outputs are buffered.

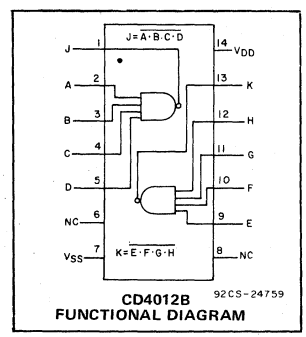
The CD4011B, CD4012B, and CD4023B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

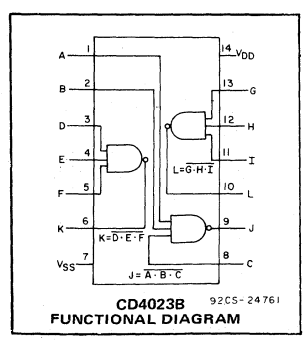
- **Propagation delay time = 60 ns (typ.) at C_L = 50 pF, V_{DD} = 10 V**
- **Buffered inputs and outputs**
- **Standardized symmetrical output characteristics**
- **Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C**
- **100% tested for quiescent current at 20 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Noise margin (over full package temperature range:**
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- **Meets all requirements of JEDEC Tentative Standard No.13A, "Standard Specifications for Description of "B" Series CMOS Devices"**



CD4011B
FUNCTIONAL DIAGRAM



CD4012B
FUNCTIONAL DIAGRAM



CD4023B
FUNCTIONAL DIAGRAM

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D,K,F,H Packages Values at –40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	–40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	4.5	–	5	1.5				—	—	1.5	V
	9	–	10	3				—	—	3	
	13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	—	—	
	1,9	–	10	7				7	—	—	
	1.5,13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200kΩ

CHARACTERISTIC	TEST CONDITIONS	ALL TYPES LIMITS		UNITS
	V_{DD} VOLTS	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH}	5	125	250	ns
	10	60	120	
	15	45	90	
Transition Time, t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Input Capacitance, C_{IN}	Any Input	5	7.5	pF

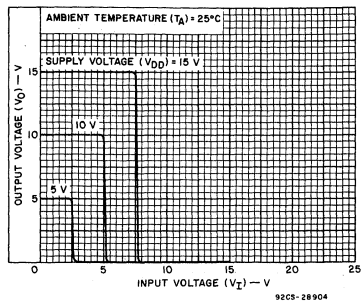


Fig.1 – Typical voltage transfer characteristics.

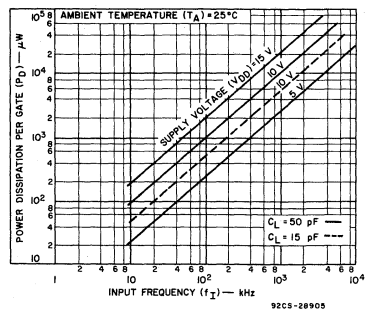


Fig.2 – Typical power dissipation characteristics.

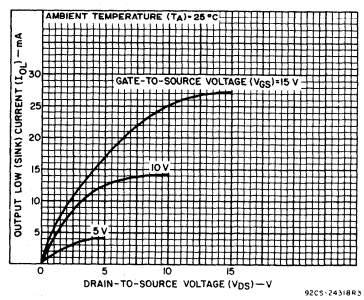


Fig.3 – Typical output low (sink) current characteristics.

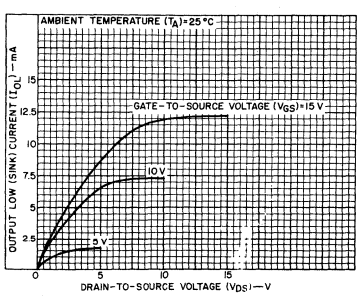


Fig.4 – Minimum output low (sink) current characteristics.

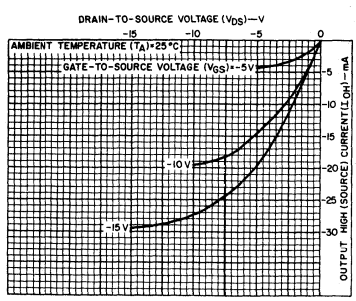


Fig.5 – Typical output high (source) current characteristics.

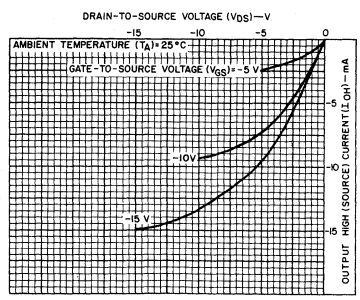


Fig.6 – Minimum output high (source) current characteristics.

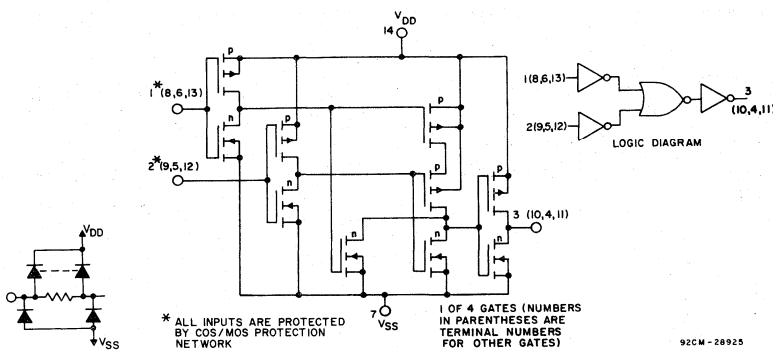


Fig.7 – Schematic and logic diagrams for CD4011B.

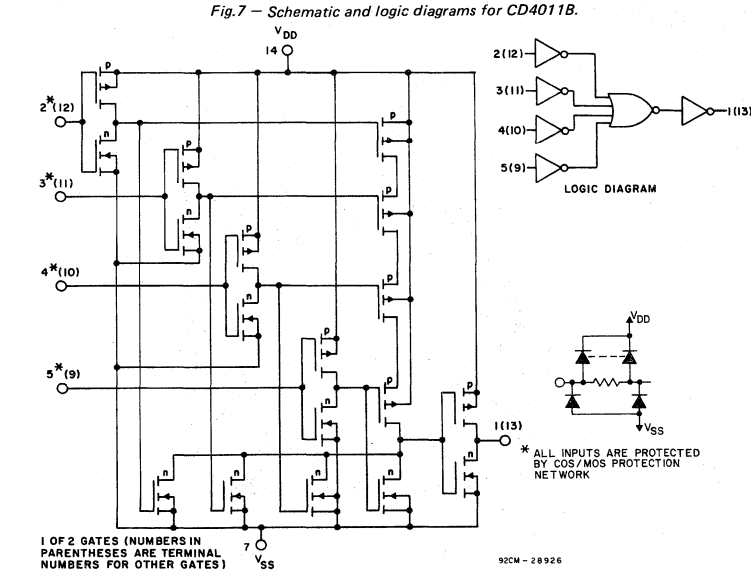


Fig.8 – Schematic and logic diagrams for CD4012B.

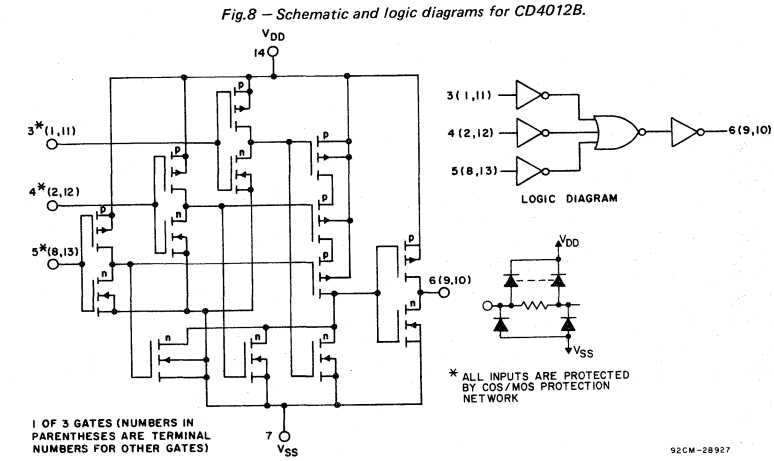


Fig.9 – Schematic and logic diagrams for CD4023B.

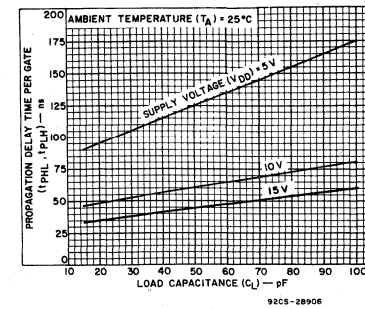


Fig.10 – Typical propagation delay time per gate as a function of load capacitance.

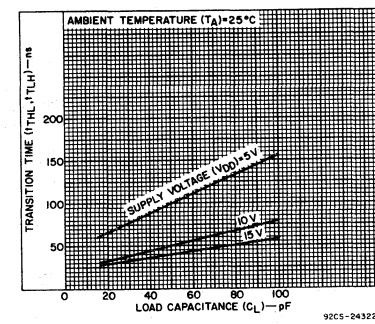


Fig.11 – Typical transition time as a function of load capacitance.

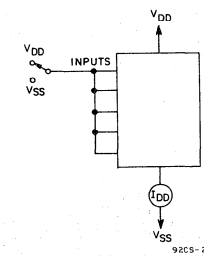


Fig.12 – Quiescent-device-current test circuit.

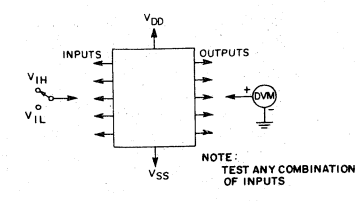


Fig.13 – Input-voltage test circuit.

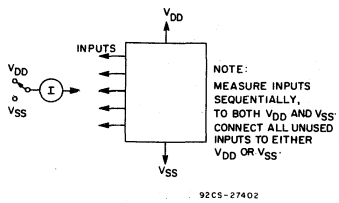
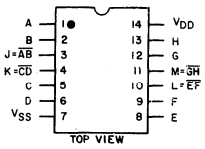
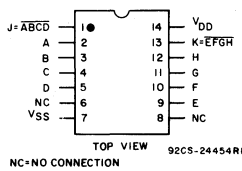


Fig. 14 – Input-current test circuit.

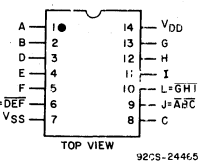
TERMINAL ASSIGNMENTS



CD4011B

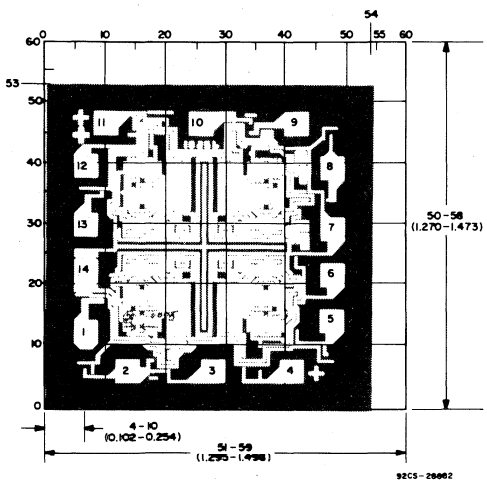


CD4012B

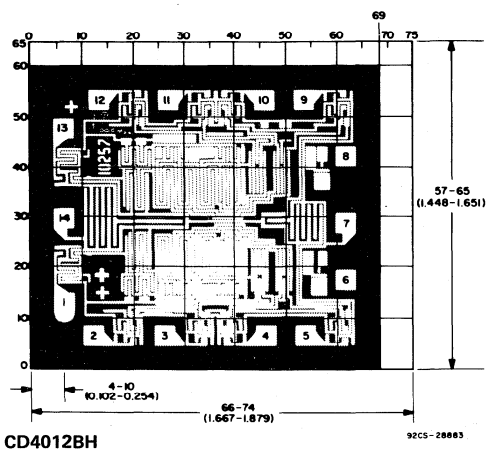


CD4023B

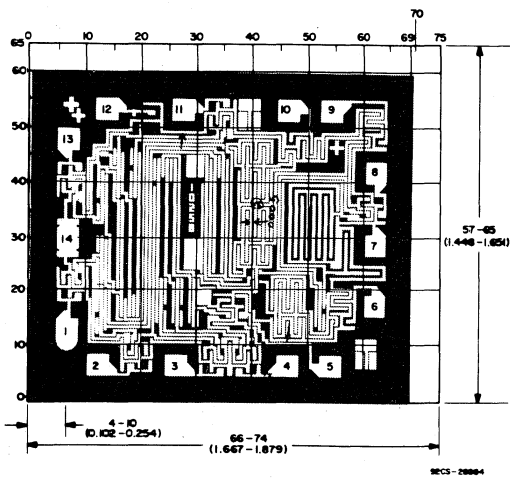
CHIP PHOTOGRAPHS
Dimensions and Pad Layouts



CD4011BH



CD4012BH



CD4023BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17mm) larger in both dimensions.

COS/MOS NAND Gates

High-Voltage Types (20-Volt Rating)

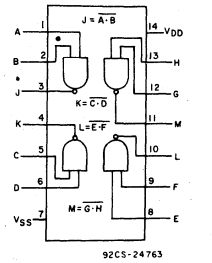
Quad 2 Input – CD4011UB
Dual 4 Input – CD4012UB
Triple 3 Input – CD4023UB

The RCA-CD4011UB, CD4012UB, and CD4023UB NAND gates provide the system designer with direct implementation of the NAND function and supplement the existing family of COS/MOS gates.

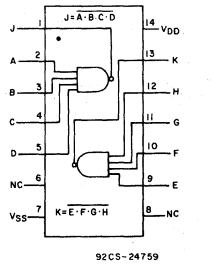
The CD4011UB, CD4012UB, and CD4023UB types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

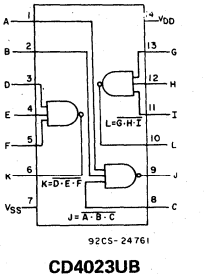
- **Propagation delay time = 30 ns (typ). at C_L = 50 pF, V_{DD} = 10 V**
- **Standardized symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**



CD4011UB FUNCTIONAL DIAGRAM



CD4012UB FUNCTIONAL DIAGRAM



CD4023UB FUNCTIONAL DIAGRAM

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D,K,F,H Packages Values at –40, +25, +85 Apply to E Package							UNITS
									+25		
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	–40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	4.5	–	5	1				—	—	1	V
	9	–	10	2				—	—	2	
	13.5	–	15	2.5				—	—	2.5	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	4				4	—	—	
	1,9	–	10	8				8	—	—	
	1.5,13.5	–	15	12.5				12.5	—	—	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	MIN.	MAX.	UNITS
Supply Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . –0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = –40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
PACKAGE TYPE E . . . . . –40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

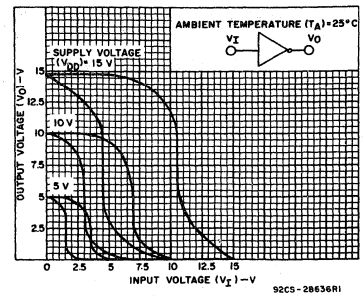


Fig.1 – Minimum and maximum voltage transfer characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C, Input t_r, t_f = 20 ns, and C_L = 50 pF, R_L = 200kΩ

CHARACTERISTIC	TEST CONDITIONS	ALL TYPES LIMITS		UNITS
	V_{DD} VOLTS	TYP.	MAX	
Propagation Delay Time, t_{PHL}, t_{PLH}	5	60	120	ns
	10	30	60	
	15	25	50	
Transition Time, t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Input Capacitance, C_{IN}	Any Input	10	15	pF

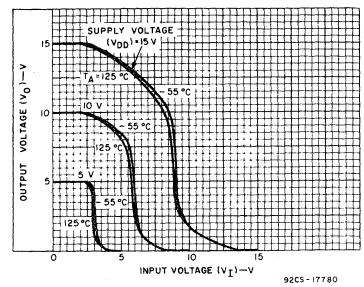


Fig.2 – Typical voltage transfer characteristics as a function of temperature.

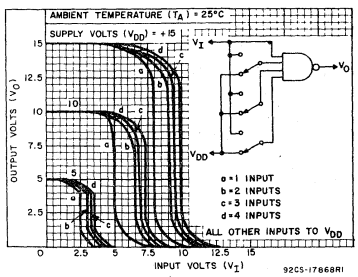


Fig.3 – Typical multiple input switching transfer characteristics for CD4012UB.

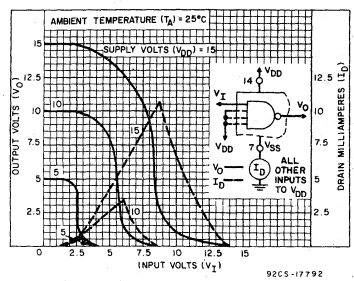


Fig.4 – Typical current and voltage transfer characteristics.

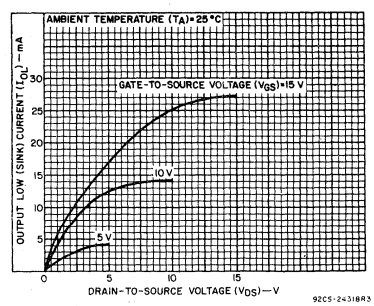


Fig.5 – Typical output low (sink) current characteristics.

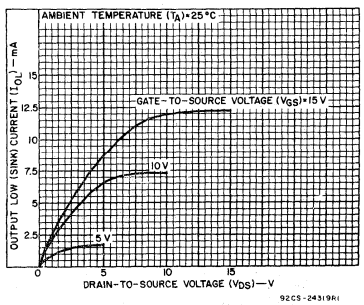


Fig.6 – Minimum output low (sink) current characteristics.

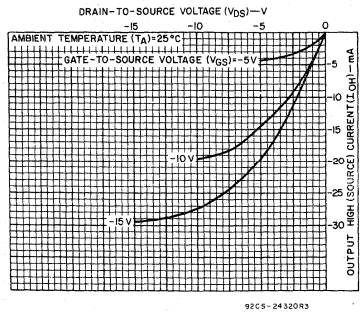


Fig.7 – Typical output high (source) current characteristics.

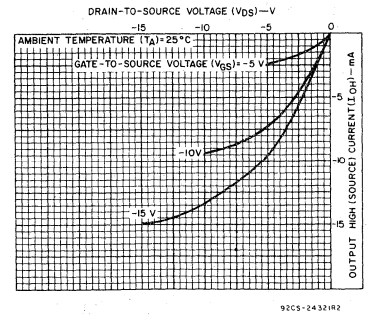


Fig.8 – Minimum output high (source) current characteristics.

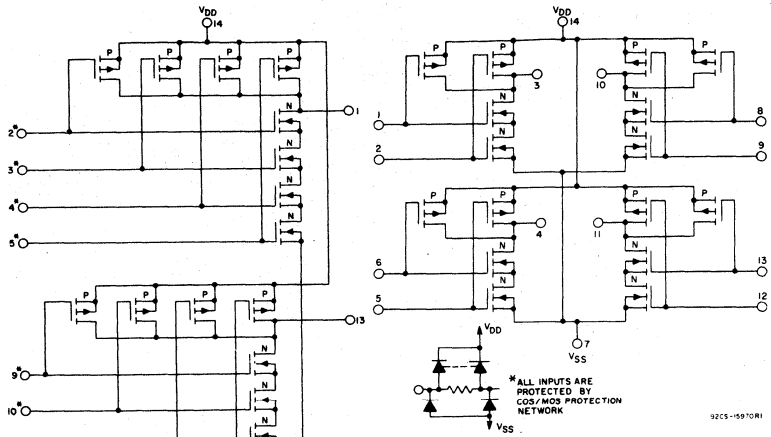


Fig.10 – Schematic diagram for type CD4011UB.

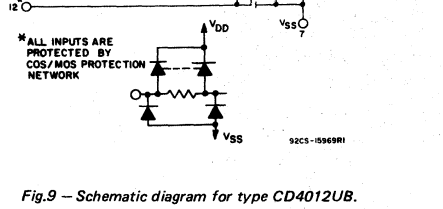
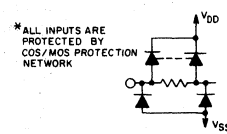


Fig.9 – Schematic diagram for type CD4012UB.



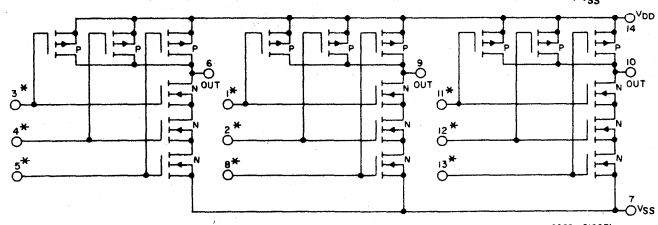


Fig.11 – Schematic diagram for type CD4023UB.

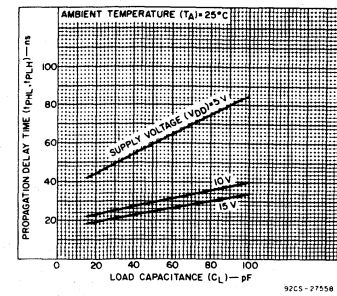


Fig.12 – Typical propagation delay time vs. load capacitance.

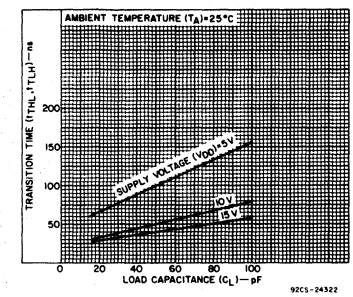


Fig.13 – Typical transition time vs. load capacitance.

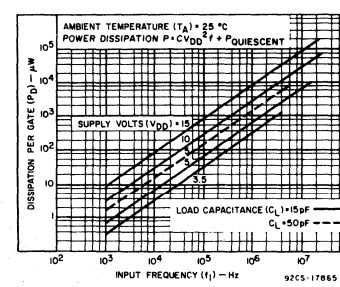


Fig.14 – Typical power dissipation vs. frequency characteristics.

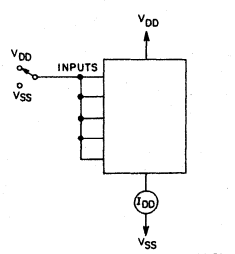


Fig.15 – Quiescent device current test circuit.

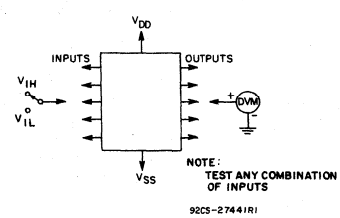


Fig.16 – Input voltage test circuit.

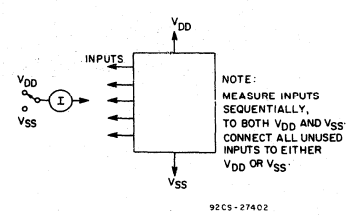
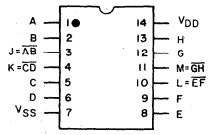


Fig.17 – Input current test circuit.

CD4011UB, CD4012UB, CD4023UB Types

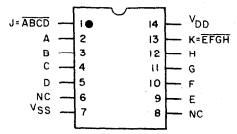
TERMINAL ASSIGNMENTS



92CS-24453

TOP VIEW

CD4011UB

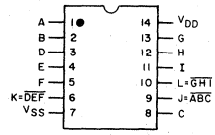


NC=NO CONNECTION

92CS-24454R1

TOP VIEW

CD4012UB

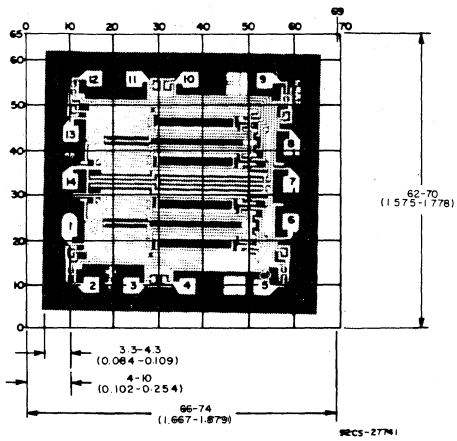


92CS-24465

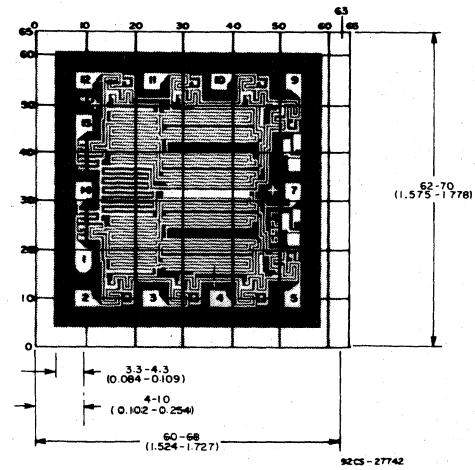
TOP VIEW

CD4023UB

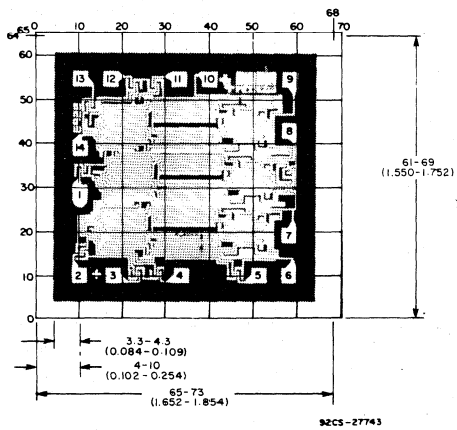
CHIP PHOTOGRAPHS
Dimensions and Pad Layouts



CD4011UBH



CD4012UBH



CD4023UBH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS Dual 'D'-Type Flip-Flop

High-Voltage Types (20-Volt Rating)

The RCA-CD4013B consists of two identical, independent data-type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs and Q and $\overline{Q}$ outputs. These devices can be used for shift register applications, and, by connecting $\overline{Q}$ output to the data input, for counter and toggle applications. The logic level present at the D input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line, respectively.

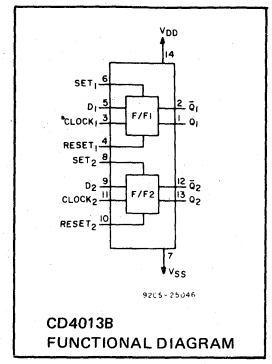
The CD4013B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- Set-Reset capability
- Static flip-flop operation – retains state indefinitely with clock level either "high" or "low"
- Medium-speed operation – 16 MHz (typ.) clock toggle rate at 10V
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range): 1 V at V_{DD}=5 V; 2 V at V_{DD}=10 V; 2.5 V at V_{DD}=15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Registers, counters, control circuits



CD4013B
FUNCTIONAL DIAGRAM

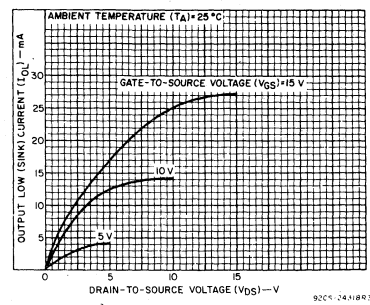


Fig. 1 – Typical output low (sink) current characteristics.

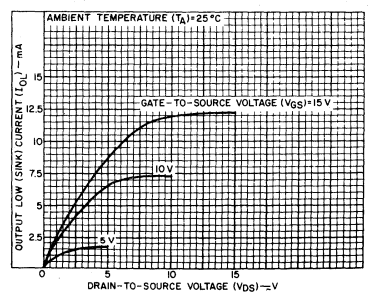


Fig. 2 – Minimum output low (sink) current characteristics.

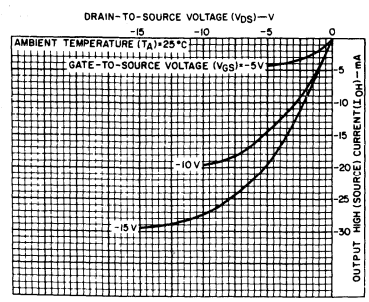


Fig. 3 – Typical output high (source) current characteristics.

RECOMMENDED OPERATING CONDITIONS

At T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	–	3	18	V
Data Setup Time t_S	5	40	–	ns
	10	20	–	
	15	15	–	
Clock Pulse Width t_W	5	140	–	ns
	10	60	–	
	15	40	–	
Clock Input Frequency f_{CL}	5	dc	3.5	MHz
	10		8	
	15		12	
Clock Rise or Fall Time t_rCL,* t_fCL	5	–	15	μs
	10	–	4	
	15	–	1	
Set or Reset Pulse Width t_W	5	180	–	ns
	10	80	–	
	15	50	–	

*If more than one unit is cascaded in a parallel clocked operation, t_rCL should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55,+25,+125 Apply to D,K,F,H Pkgs. Values at −40,+25,+85 Apply to E Pkgs.							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

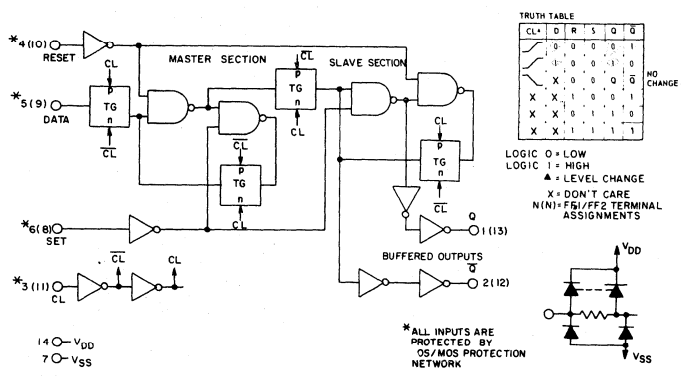


Fig. 7 — Logic diagram and truth table for CD4013B (one of two identical flip-flops).

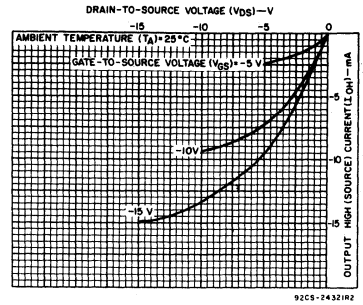


Fig. 4 — Minimum output high (source) current characteristics.

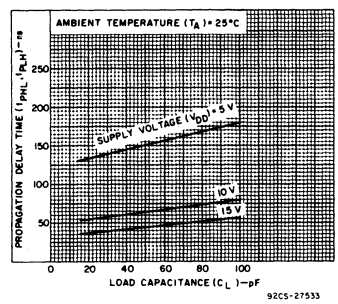


Fig. 5 — Typical propagation delay time vs. load capacitance (CLOCK or SET to Q,CLOCK or RESET to $\overline{Q}$).

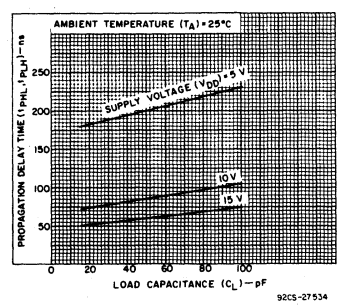


Fig. 6 — Typical propagation delay time vs. load capacitance (SET to $\overline{Q}$ or RESET to Q.

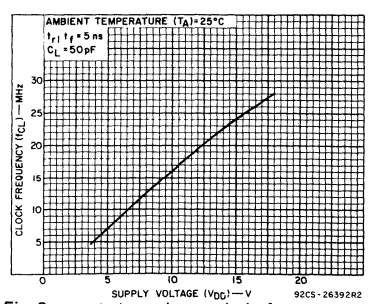


Fig. 8 — Typical maximum clock frequency vs. supply voltage.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . –0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = –40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
PACKAGE TYPE E . . . . . –40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

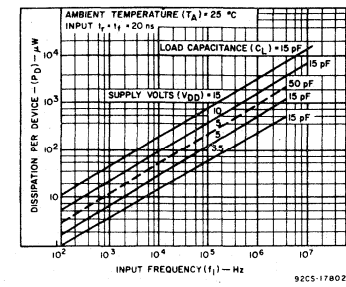


Fig. 9 — Typical power dissipation vs. frequency.

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Propagation Delay Time: Clock to Q or $\overline{Q}$ Outputs t_{PHL}, t_{PLH}	5	–	150	300	ns
	10	–	65	130	
	15	–	45	90	
Set to Q or Reset to $\overline{Q}$ t_{PLH}	5	–	150	300	ns
	10	–	65	130	
	15	–	45	90	
Set to $\overline{Q}$ or Reset to Q t_{PHL}	5	–	200	400	ns
	10	–	85	170	
	15	–	60	120	
Transition Time t_{THL}, t_{TLH}	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Maximum Clock Input Frequency Frequency # f_{CL}	5	3.5	7	–	MHz
	10	8	16	–	
	15	12	24	–	
Minimum Clock Pulse Width t_W	5	–	70	140	ns
	10	–	30	60	
	15	–	20	40	
Minimum Set or Reset Pulse Width t_W	5	–	90	180	ns
	10	–	40	80	
	15	–	25	50	
Minimum Data Setup Time t_S	5	–	20	40	ns
	10	–	10	20	
	15	–	7	15	
Clock Input Rise or Fall Time t_{rCL}, t_{fCL}	5	–	–	15	μs
	10	–	–	4	
	15	–	–	1	
Input Capacitance C_{IN}	Any Input	–	5	7.5	pF

#Input t_r, t_f = 5 ns.

TEST CIRCUITS

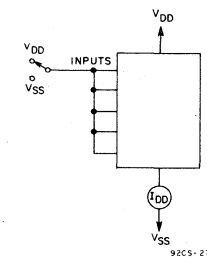


Fig. 9 — Quiescent device current.

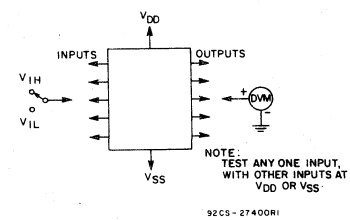


Fig. 10 — Input voltage.

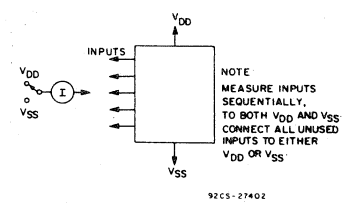
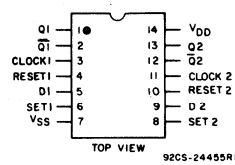
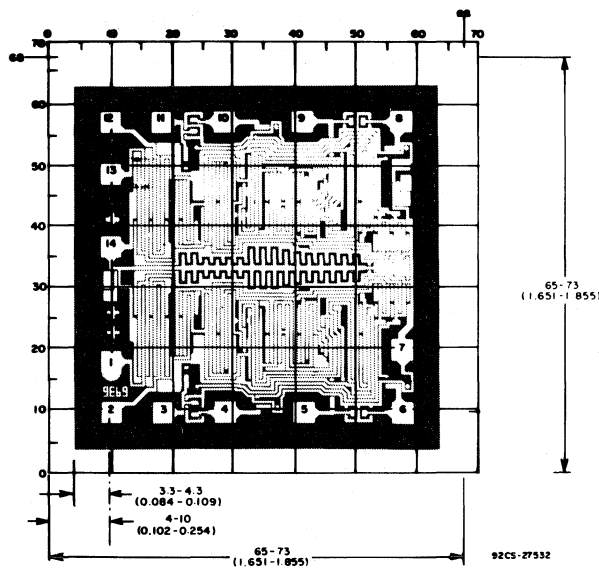


Fig. 11 — Input current.



TERMINAL ASSIGNMENT

DIMENSIONS AND PAD LAYOUT FOR CD4013BH



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Preliminary Data

COS/MOS 8-Stage Static Shift Registers

High-Voltage Types (20-Volt Rating)

CD4014B:
Synchronous Parallel or
Serial Input/Serial Output

CD4021B:
Asynchronous Parallel or Synchronous
Serial Input/Serial Output

The RCA-CD4014B and CD4021B series types are 8-stage parallel- or serial-input/serial output registers having common CLOCK and PARALLEL/SERIAL CONTROL inputs, a single SERIAL data input, and individual parallel "JAM" inputs to each register stage. Each register stage is a D-type, master-slave flip-flop. In addition to an output from stage 8, "Q" outputs are also available from stages 6 and 7. Parallel as well as serial entry is made into the register synchronous with the positive clock line transition in the CD4014B. In the CD4021B serial entry is synchronous with the clock but parallel entry is asynchronous. In both types, entry is controlled by the PARALLEL/SERIAL CONTROL input. When the PARALLEL/SERIAL CONTROL input is low, data is serially shifted into the 8-stage register synchronously with the positive transition of the clock line. When the PARALLEL/SERIAL CONTROL input is high, data is jammed into the 8-stage register via the parallel input lines and synchronous with the positive transition of the clock line. In the CD4021B, the CLOCK input of the internal stage is "forced" when asynchronous parallel entry is made. Register expansion using multiple packages is permitted.

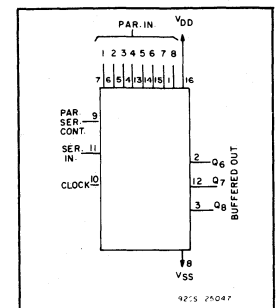
The CD4014B and CD4021B series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Recommended Operating Conditions
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

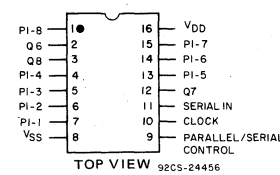
Characteristic	V_{DD} (V)	Min.	Max.	Units
Supply-Voltage Range (T_A=Full Package Temperature Range)	–	3	18	V

Features:
- Medium-speed operation . . . 12 MHz (typ.) clock rate at $V_{DD}-V_{SS}$ = 10 V
- Fully static operation
- 8 master-slave flip-flops plus output buffering and control gating
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:
- Parallel input/serial output data queueing
- Parallel to serial data conversion
- General-purpose register



CD4014B, CD4021B
FUNCTIONAL DIAGRAM



TERMINAL DIAGRAM
CD4014B, CD4021B

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D,K,F,H Packages Values at –40, +25, +85 Apply to E Package							UNITS
									+25		
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	–40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	15, 13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5, 3.5	–	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

Preliminary Data

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C, Input t_r,t_f=20 ns, C_L=50 pF, R_L=200 KΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS TYPICAL VALUES	UNITS
Propagation Delay Time; t_{PLH}, t_{PHL}	5	200	ns
	10	100	
	15	80	
Transition Time; t_{THL}, t_{TLH}	5	100	ns
	10	50	
	15	40	
Maximum Clock Input Frequency, f_{CL}	5	5	MHz
	10	12	
	15	16	
Minimum Clock Pulse Width, t_W	5	100	ns
	10	45	
	15	30	
Clock Rise & Fall Time; t_rCL, t_fCL*	5	15	μs
	10	15	
	15	15	
Minimum Data Set-up Time, t_S	5	50	ns
	10	25	
	15	20	
Average Input Capacitance, C_I	Any Input	5	pF

*If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

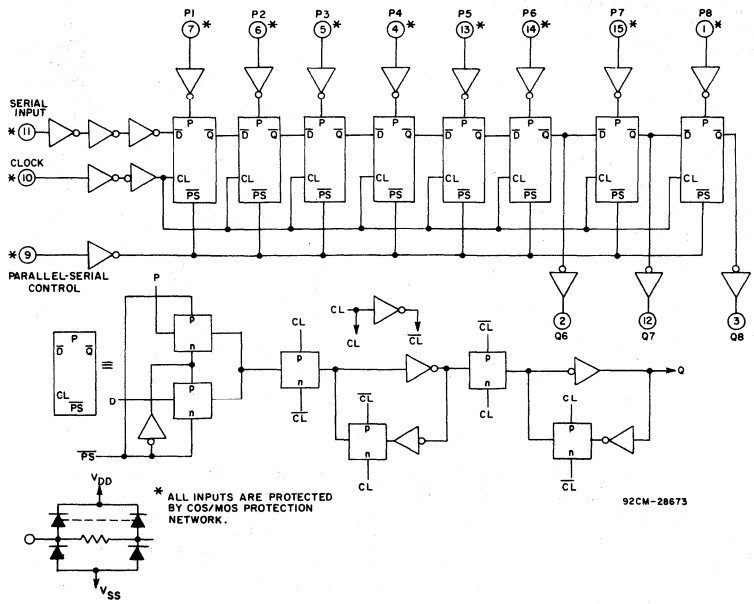


Fig. 1 — Logic diagram for CD4014B.

TRUTH TABLE

CL▲	SER IN	PAR SER CONTROL	PI-1	PI-n	Q_1 (INTERNAL)	Q_n	
	X	1	0	0	0	0	
	X	1	1	0	1	0	
	X	1	0	1	0	1	
	X	1	1	1	1	1	
	0	0	X	X	0	Q_n-1	
	1	0	X	X	1	Q_n-1	
	X	X	X	X	Q_1	Q_n	NC

X = DON'T CARE CASE ▲ = LEVEL CHANGE
NC = NO CHANGE

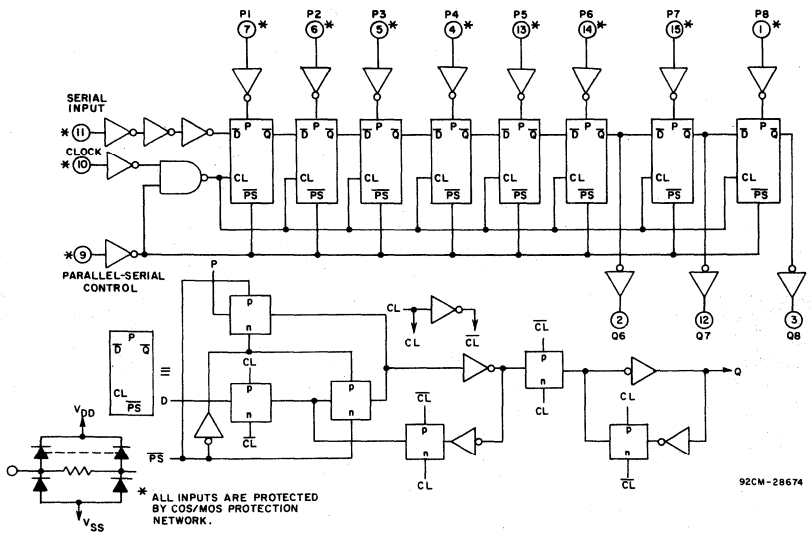


Fig. 2 — Logic diagram for CD4021B.

TRUTH TABLE

CL▲	Serial Input	Parallel/ Serial Control	PI-1	PI-n	Q_1 (Internal)	Q_n	
X	X	1	0	0	0	0	
X	X	1	0	1	0	1	
X	X	1	1	0	1	0	
X	X	1	1	1	1	1	
	0	0	X	X	0	Q_n-1	
	1	0	X	X	1	Q_n-1	
	X	0	X	X	Q_1	Q_n	NC

▲ = LEVEL CHANGE X = DON'T CARE CASE

COS/MOS Dual 4-Stage Static Shift Register

With Serial Input/Parallel Output

High-Voltage Types (20-Volt Rating)

Preliminary Data

The RCA-CD4015B consists of two identical, independent, 4-stage serial-input/parallel-output registers. Each register has independent CLOCK and RESET inputs as well as a single serial DATA input. "Q" outputs are available from each of the four stages on both registers. All register stages are D-type, master-slave flip-flops. The logic level present at the DATA input is transferred into the first register stage and shifted over one stage at each positive-going clock transition. Resetting of all stages is accomplished by a high level on the reset line. Register expansion to 8 stages using one CD4015B package, or to more than 8 stages using additional CD4015B's is possible.

The CD4015B-series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

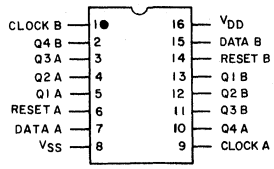
Features:

- **Medium speed operation . . . . . 12 MHz (typ.) clock rate at $V_{DD} - V_{SS}$ = 10 V**
- **Fully static operation**
- **8 master-slave flip-flops plus input and output buffering**
- **Standardized, symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

- **Serial-input/parallel-output data queueing**
- **Serial to parallel data conversion**
- **General-purpose register**

TERMINAL DIAGRAM
Top View



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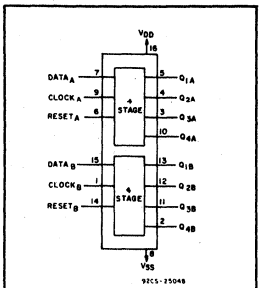


CD4015B
FUNCTIONAL DIAGRAM

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
									+25		
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . 0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . 0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS
at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS	UNITS
	V_{DD} (V)	TYPICAL VALUES	
CLOCKED OPERATION			
Propagation Delay Time; T_{PLH}, T_{PHL}	5	200	ns
	10	100	
	15	80	
Transition Time; t_{THL}, t_{TLH}	5	100	ns
	10	50	
	15	40	
Minimum Clock Pulse Width, t_W	5	100	ns
	10	45	
	15	30	
Clock Rise & Fall Time; t_rCL, t_fCL*	5	15	μs
	10	15	
	15	15	
Minimum Data Setup Time, t_S	5	50	ns
	10	25	
	15	20	
Maximum Clock Input Frequency, f_{CL}	5	5	MHz
	10	12	
	15	16	
Average Input Capacitance, C_I	Any Input	5	pF
RESET OPERATION			
Propagation Delay Time, T_{PLH}, T_{PHL}	5	200	ns
	10	100	
	15	80	
Minimum Reset Pulse Width t_W	5	100	ns
	10	45	
	15	30	

* If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

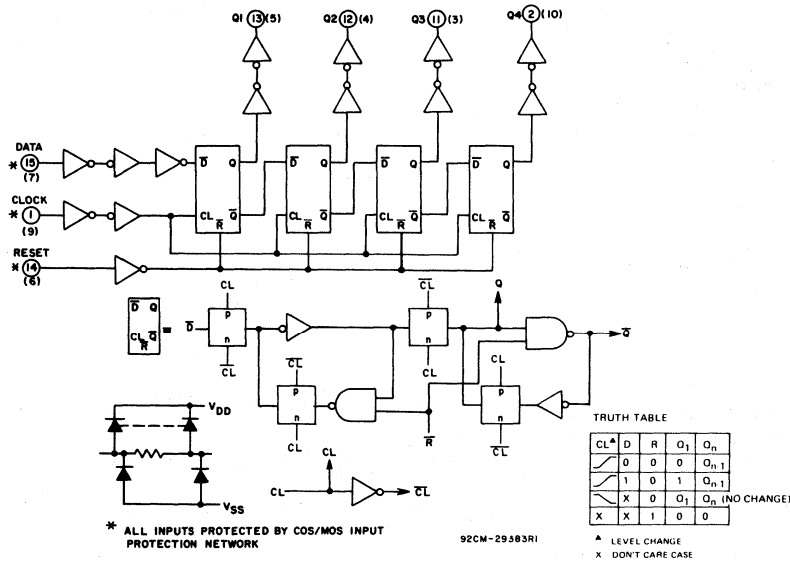


Fig. 1 – Logic diagram.

COS/MOS Quad Bilateral Switch

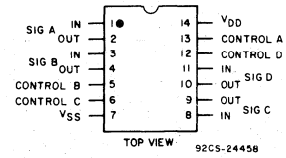
For Transmission or Multiplexing of Analog or Digital Signals

High-Voltage Types (20-Volt Rating)

The RCA-CD4016B Series types are quad bilateral switches intended for the transmission or multiplexing of analog or digital signals. Each of the four independent bilateral switches has a single control signal input which simultaneously biases both the p and n device in a given switch ON or OFF.

The CD4016 "B" Series types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

Terminal Assignment



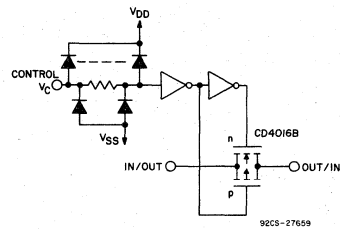
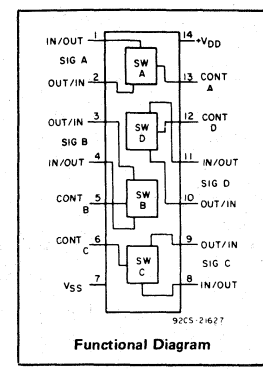


Fig.1 – Schematic diagram – 1 of 4 identical sections.



Functional Diagram

Features:

- 20-V digital or ± 10-V peak-to-peak switching
- 280-Ω typical ON resistance for 15-V operation
- Switch ON resistance matched to within 10 Ω typ. over 15-V signal-input range
- High ON/OFF output-voltage ratio: 65 dB typ. @ f_{is} = 10 kHz, R_L = 10 kΩ
- High degree of linearity: <0.5% distortion typ. @ f_{is} = 1 kHz, V_{is} = 5 V_{p-p}, $V_{DD}-V_{SS} \geq 10$ V, R_L = 10 kΩ
- Extremely low OFF switch leakage resulting in very low offset current and high effective OFF resistance: 100 pA typ. @ $V_{DD}-V_{SS}$=18 V, T_A=25°C
- Extremely high control input impedance (control circuit isolated from signal circuit: 10^{12} Ω typ.
- Low crosstalk between switches: –50 dB typ. @ f_{is} = 0.9 MHz, R_L = 1 kΩ
- Matched control-input to signal-output capacitance: Reduces output signal transients
- Frequency response, switch ON = 40 MHz (typ.)
- 100% tested for quiescent current at 20 V
- Maximum control input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V at 25°C
- 5-V, 10-V, and 15-V parametric ratings

Applications:

- Analog signal switching/multiplexing
  - Signal gating
  - Squelch control
  - Chopper
  - Modulator
  - Demodulator
  - Commutating switch
- Digital signal switching/multiplexing
- COS/MOS logic implementation
- Analog-to-digital & digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

TYPICAL "ON" RESISTANCE CHARACTERISTICS, T_A = 25°C

CHARACTERISTIC*	SUPPLY CONDITIONS		LOAD CONDITIONS					
			R_L = 1kΩ		R_L = 10kΩ		R_L = 100kΩ	
	V_{DD} (V)	V_{SS} (V)	VALUE (Ω)	V_{is} (V)	VALUE (Ω)	V_{is} (V)	VALUE (Ω)	V_{is} (V)
R_{ON}	+15	0	200	+15	200	+15	180	+15
			200	0	200	0	200	0
R_{ON}(max.)	+15	0	300	+11	300	+9.3	320	+9.2
R_{ON}	+10	0	290	+10	250	+10	240	+10
			290	0	250	0	300	0
R_{ON}(max.)	+10	0	500	+7.4	560	+5.6	610	+5.5
R_{ON}	+ 5	0	860	+ 5	470	+ 5	450	+ 5
			600	0	580	0	800	0
R_{ON}(max.)	+ 5	0	1.7k	+4.2	7k	+2.9	33k	+2.7
R_{ON}	+7.5	–7.5	200	+7.5	200	+7.5	180	+7.5
			200	–7.5	200	–7.5	180	–7.5
R_{ON}(max.)	+7.5	–7.5	290	±0.25	280	±25	400	±0.25
R_{ON}	+ 5	– 5	260	+ 5	250	+ 5	240	+ 5
			310	– 5	250	– 5	240	– 5
R_{ON}(max.)	+ 5	– 5	600	±0.25	580	±0.25	760	±0.25
R_{ON}	+2.5	–2.5	590	+2.5	450	+2.5	490	+2.5
			720	–2.5	520	–2.5	520	–2.5
R_{ON}(max.)	+2.5	–2.5	232k	±0.25	300k	±0.25	870k	±0.25

* Variation from a perfect switch, R_{ON} = 0Ω.

ELECTRICAL CHARACTERISTICS

Characteristic	Test Conditions: All Voltage Values are in Volts			Limits: Values at −55°C,+25°C,+125°C Apply to D,F,K,H Packages; Values at −40°C,+25°C,+85°C Apply to E Package						Unit
			V_{DD} (V)	−55°	−40°	+85°	+125°	+25°C Typ.	+25°C Max.	
Quiescent Device Current, I_{DD} max (All switches ON or all Switches OFF)			5	0.25	0.25	7.5	7.5	0.01	0.25	μA
			10	0.5	0.5	15	15	0.01	0.5	
			15	1	1	30	30	0.01	1	
			20	5	5	150	150	0.02	5	
Signal Inputs (V_{is}) and Outputs (V_{os})										
ON Resistance, R_{ON}	V_C=V_{DD}	V_{SS}	V_{is}	Typ/Max	Typ/Max	Typ/Max	Typ/Max			Ω
	R_L = 10 kΩ●									
	+7.5	-7.5	+7.5	120/360	130/370	260/520	300/600	200	400	
			−7.5	120/360	130/370	260/520	300/600	200	400	
			±0.25	130/775	160/790	400/1080	470/1230	280	850	
	+5	−5	+5	130/600	150/610	340/840	400/960	250	660	
			−5	130/600	150/610	340/840	400/960	250	660	
			±0.25	325/1870	370/1900	770/2380	900/2600	580	2000	
	+15	0	+15	120/360	130/370	260/520	300/600	200	400	
			+0.25	120/360	130/370	260/520	300/600	200	400	
			+9.3	150/775	180/790	400/1080	490/1230	300	850	
	+10	0	+10	130/600	150/610	340/840	400/960	250	660	
			+0.25	130/600	150/610	340/840	400/960	250	660	
			+5.6	300/187Ω	350/1900	750/2380	880/2600	560	2000	
ΔON Resistance Between Any 2 of 4 Switches ΔR_{ON}	R_L = 10 kΩ●									
	+7.5	-7.5	±7.5	–	–	–	–	10	–	Ω
	+5	−5	±5	–	–	–	–	15	–	
Sine Wave Response (Distortion)	+5	−5	5V p-p▲							
	R_L = 10 kΩ, f_{is} = 1 kHz			–	–	–	–	0.4	–	%
Frequency Response Switch ON (Sine-Wave Input)	+5	−5	5 p-p							
	R_L = 1 kΩ, $20 \log_{10} \frac{V_{os}}{V_{is}}$ = −3 dB			–	–	–	–	40	–	MHz
Feedthrough Switch OFF	V_{DD} = +5, V_C=V_{SS}=−5		−5 p-p							
	R_L = 1 kΩ, $20 \log_{10} \frac{V_{os}}{V_{is}}$ = −50 dB			–	–	–	–	1.25	–	MHz
Input or Output Leakage Current Switch OFF (Effective OFF Resistance)	V_{DD}	V_C=V_{SS}								
	+18	0	–					10^{-3}	±100	nA

▲ Symmetrical about 0 volts.
● For all test conditions.

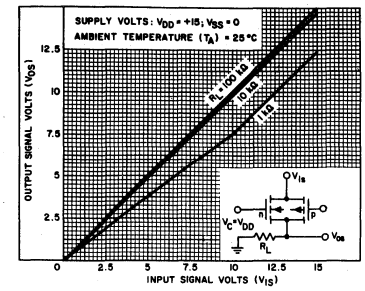


Fig.2 – Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +15 V, V_{SS} = 0 V.

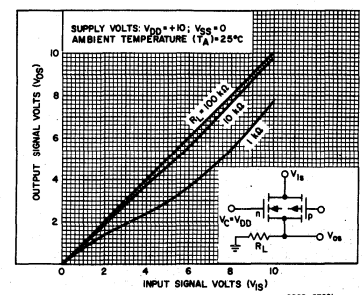


Fig.3 – Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +10 V, V_{SS} = 0 V.

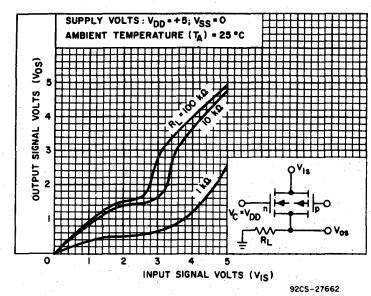


Fig.4 – Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +5 V, V_{SS} = 0 V.

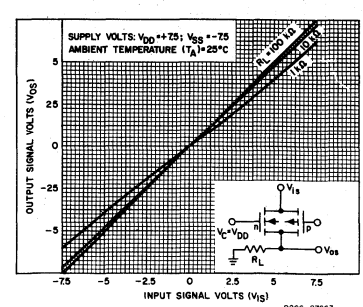


Fig.5 – Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +7.5 V, V_{SS} = -7.5 V.

ELECTRICAL CHARACTERISTICS (Cont'd)

Characteristic	Test Conditions All Voltage Values are in Volts	V_{DD} (V)	Limits Values at −55°C,+25°C,+125°C Apply to D,F,K,H Packages Values at −40°C,+25°C,+85°C Apply to E Package −55°	−40°	+85°	+125°	+25°C Typ.	+25°C Max.	Unit
Crosstalk Between Any 2 of 4 Switches (f = −50 dB)	$V_C(A)=V_{DD}=+5$ $V_C(B)=V_{SS}=-5$ $V_{is}(A)$ = 5 p-p R_L=1 kΩ $20\log_{10}\frac{V_{os}(B)}{V_{is}(A)}$ = −50 dB		–	–	–	–	0.9	–	MHz
Propagation Delay (Signal Input to Signal Output) t_{pd}	$V_C = V_{DD}$ V_{SS} = GND C_L = 50 pF V_{is} = 10 Sq. Wave t_r, t_f = 20 ns	V_{DD} 5					40	100	ns
		10	–	–	–	–	20	50	
		15					15	40	
Capacitance: Input, C_{is}	V_{DD}=+5		–	–	–	–	4	–	pF
Output, C_{os}	$V_{CC}=V_{SS}=-5$		–	–	–	–	4	–	
Feedthrough, C_{ios}			–	–	–	–	0.2	–	
Control (V_C)									
Switch Threshold Voltage, V_{TH}	I_{is} = 10μA	V_{DD} 5	1 min; 2.25 typ.						V
		10	2 min; 4.5 typ.						
		15	2 min; 6.75 typ.						
Input Current, I_{IN} Max.	$V_{is} \leq V_{DD}$	V_{DD} =18	±0.1		±1		±10−5	±0.1	μA
Crosstalk (Control Input to Signal Output)	V_C=10 (Sq.Wave) t_r, t_f=20 ns R_L=10 kΩ	V_{DD} =10	–	–	–	–	50	–	mV
Turn-On Propagation Delay, t_{pd}	$V_{DD}-V_{SS}$=10 V_{DD} 10, (See Fig.25) t_r, t_f=20 ns C_L=50 pF R_L= 1 kΩ	V_{DD} 5	–	–	–	–	35	70	ns
		10	–	–	–	–	20	40	
		15	–	–	–	–	15	30	
Maximum Allowable Control Input Repetition Rate	V_{DD}=10, V_{SS}=GND R_L=1 kΩ, C_L=50pF V_{CC}=10(Sq.Wave) t_r, t_f = 20 ns		–	–	–	–	10		MHz
Input Capacitance, C_{IN}				–	–	–	5	7.5	pF

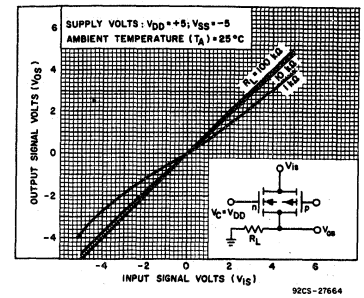


Fig.6 – Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +5 V, V_{SS} = -5 V.

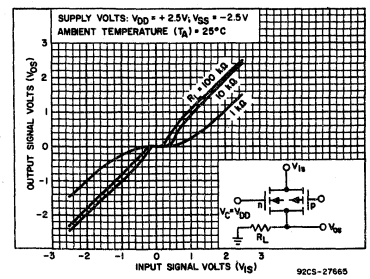


Fig.7 – Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +2.5 V, V_{SS} = -2.5 V.

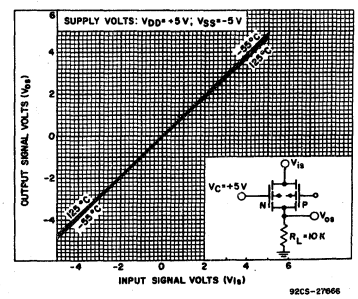


Fig.8 – Typ. "ON" characteristics as a function of temp. for 1 of 4 switches with V_{DD} = +5 V, V_{SS} = -5 V.

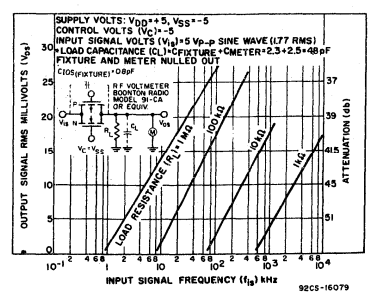


Fig.9 – Typ. feedthru vs. frequency – switch "OFF".

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

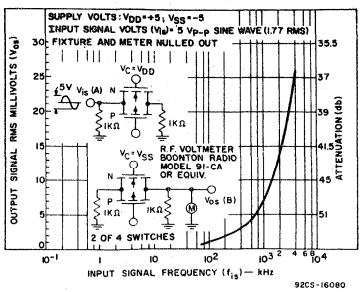


Fig.10 – Typical crosstalk between switch circuits in the same package.

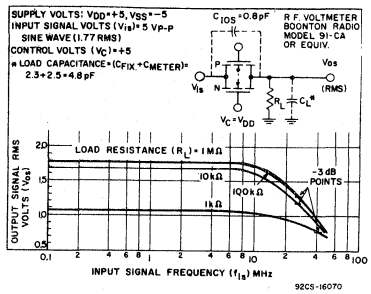


Fig.11 – Typical switch frequency response – switch "ON".

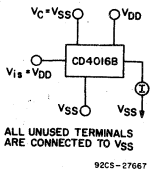


Fig.12 – "OFF" switch input or output leakage current test circuit.

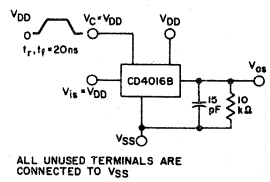


Fig.13 – Test circuit for square-wave response.

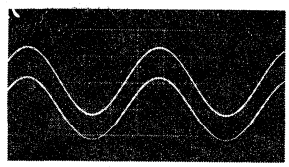


Fig.14 – Typical sine wave response of V_{DD} = +7.5 V, V_{SS} = –7.5 V.

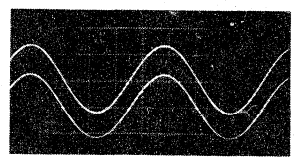


Fig.15 – Typical sine wave response of V_{DD} = +5 V, V_{SS} = –5 V.

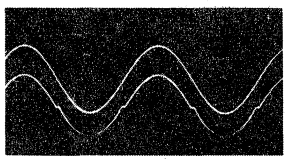


Fig.16 – Typical sine wave response of V_{DD} = +2.5 V, V_{SS} = –2.5 V.

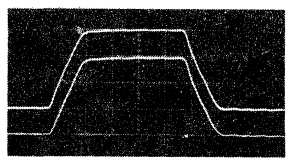


Fig.17 – Typical square wave response at V_{DD} = V_C = +15 V, V_{SS} = Gnd.

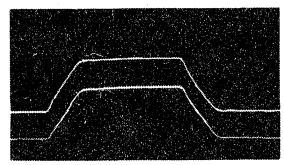


Fig.18 – Typical square wave response at V_{DD} = V_C = +10 V, V_{SS} = Gnd.

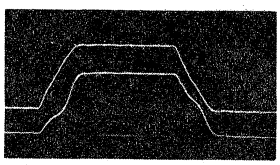
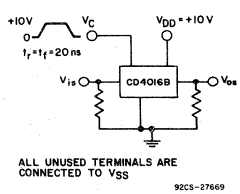
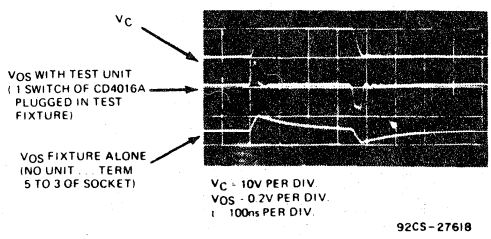


Fig.19 – Typical square wave response at V_{DD} = V_C = +5 V, V_{SS} = Gnd.



(a)



(b)

Fig.20 – Crosstalk-control input to signal output.

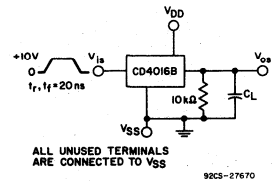


Fig.21 – Propagation delay time signal input (V_{IS}) to signal output (V_{OS}).

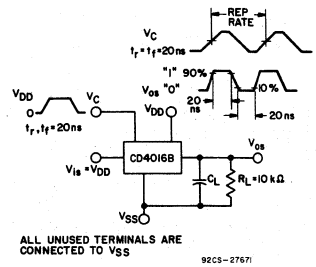


Fig.22 – Max. allowable control-input repetition rate.

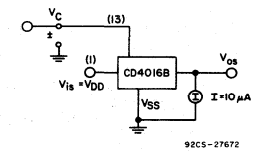


Fig.23 – Switch threshold voltage.

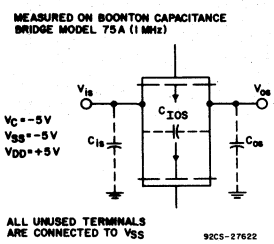
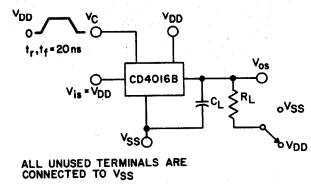


Fig.24 – Capacitance C_{IOS} and C_{OS}.



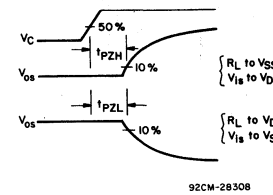
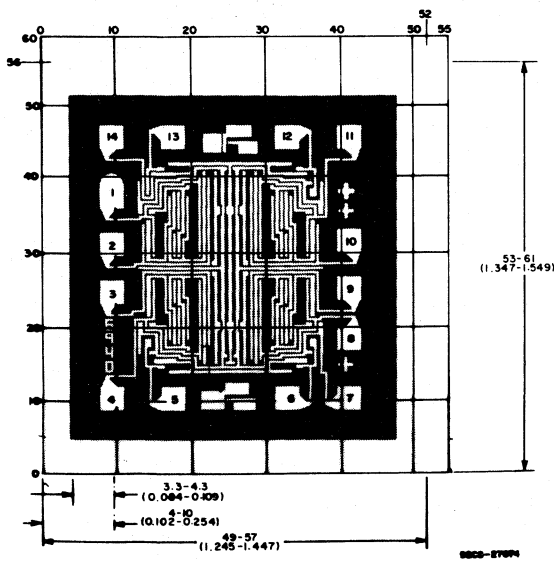


Fig.25 – Turn-On propagation delay-control input.

Dimensions and pad layout for CD4016BH



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CD4017B, CD4022B Types

COS/MOS Counter/Dividers

Preliminary Data

High-Voltage Types (20-Volt Rating)

CD4017B—Decade Counter with 10 Decoded Outputs
CD4022B—Octal Counter with 8 Decoded Outputs

The RCA-CD4017B and CD4022B are 5-stage and 4-stage Johnson counters having 10 and 8 decoded outputs, respectively. Inputs include a CLOCK, a RESET, and a CLOCK INHIBIT signal. Schmitt trigger action in the CLOCK input circuit provides pulse shaping that allows unlimited clock input pulse rise and fall times.

These counters are advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. A high RESET signal clears the counter to its zero count. Use of the Johnson decade-counter configuration permits high-speed operation, 2-input decimal-decode gating, and spike-free decoded outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The decoded outputs are normally low and go high only at their respective decoded time slot. Each decoded output remains high for one full clock cycle. A CARRY-OUT signal completes one cycle every 10 clock input cycles in the CD4017B or every 8 clock input cycles in the CD4022B and is used to ripple-clock the succeeding device in a multi-device counting chain.

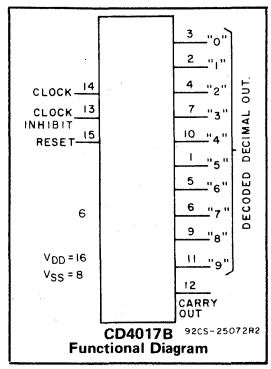
The CD4017B and CD4022B-series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

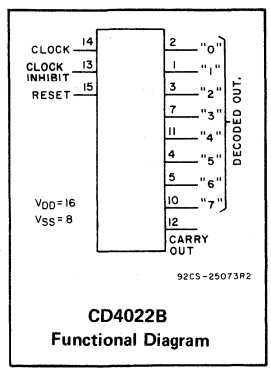
- **Fully static operation**
- **Medium-speed operation . . . 12 MHz (typ.) at V_{DD} = 10 V**
- **Standardized, symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

- **Decade counter/decimal decode display**
- **Binary counter/decoder**
- **Frequency division**
- **Counter control/timers**
- **Divide-by-N counting**
- **For further application information, see ICAN-6166 "COS/MOS MSI Counter and Register Design and Applications"**



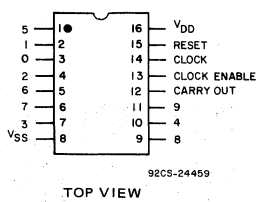
CD4017B
Functional Diagram



CD4022B
Functional Diagram

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C



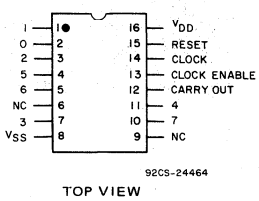
TOP VIEW

CD4017B
TERMINAL DIAGRAM

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS ALL TYPES		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V



TOP VIEW
NC = no connection

CD4022B
TERMINAL DIAGRAM

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
									+25		
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1, 9	–	10	7				7	–	–	
	1.5,13.5	-	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

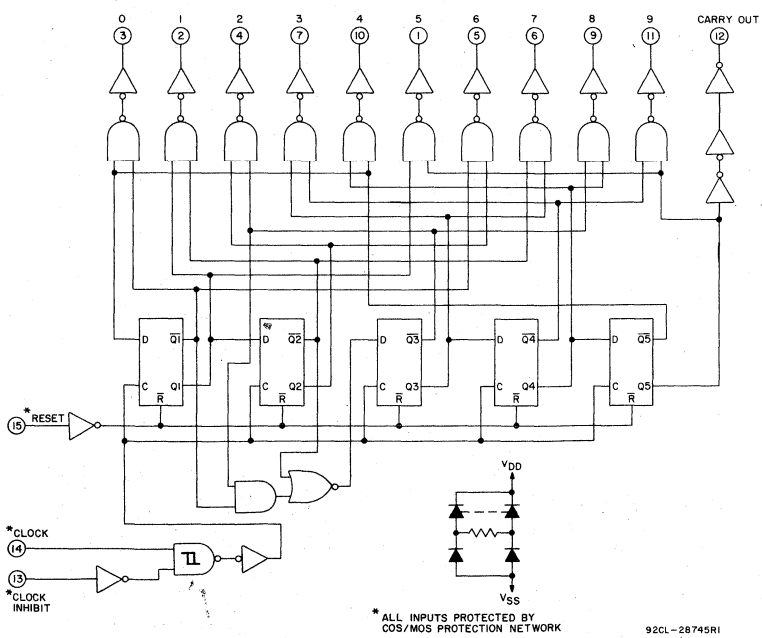


Fig. 1 – Logic diagram for CD4017B.

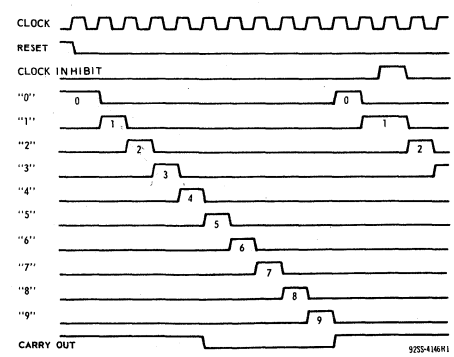


Fig. 2 – Timing diagram for CD4017B.

DYNAMIC ELECTRICAL CHARACTERISTICS
At T_A = 25°C, Input t_r,t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	CONDITIONS V_{DD} (V)	TYPICAL VALUES	UNITS
CLOCKED OPERATION			
Propagation Delay Time, t_{PHL}, t_{PLH} Carry Out or Decode Out Lines	5 10 15	250 100 80	ns
Transition Time, t_{THL}, t_{TLH} Carry Out or Decode Out Lines	5 10 15	100 50 40	ns
Maximum Clock Input Frequency, f_{CL}*	5 10 15	5 12 16	MHz
Minimum Clock Pulse Width, t_W	5 10 15	100 45 30	ns
Clock Rise or Fall Time, t_rCL, t_fCL	5, 10, 15	Unlimited	μs
Minimum Clock Inhibit Setup Time, t_s	5 10 15	175 75 50	ns
Input Capacitance, C_{IN}	Any Input	5	pF
RESET OPERATION			
Propagation Delay Time, t_{PHL}, t_{PLH} Carry Out or Decode Out Lines	5 10 15	250 100 80	ns
Minimum Reset Pulse Width, t_W	5 10 15	200 100 75	ns
Minimum Reset Removal Time	5 10 15	100 50 40	ns

*Measured with respect to carry output line.

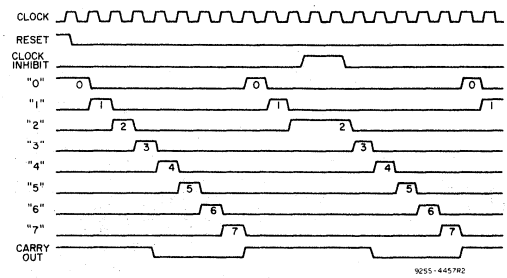


Fig. 3 – Timing diagram for CD4022B.

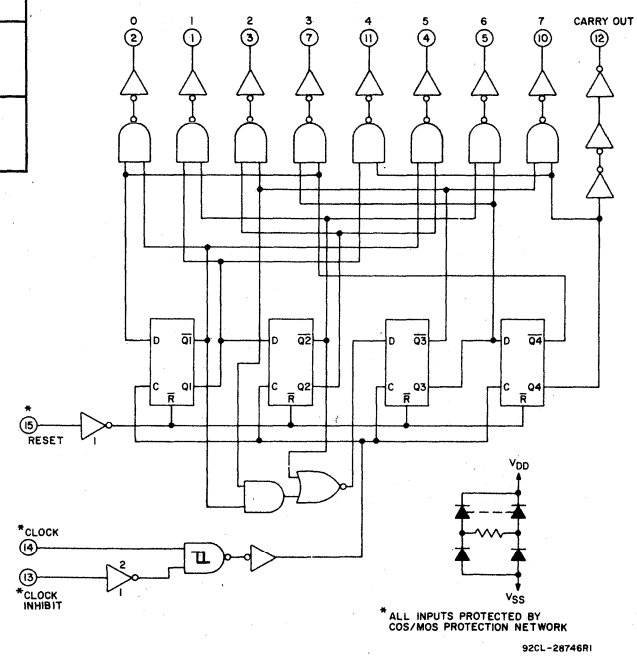


Fig. 4 – Logic diagram for CD4022B.

Preliminary Data

COS/MOS Presettable Divide-By-'N' Counter

High-Voltage Types (20-Volt Rating)

The RCA-CD4018B types consist of 5 Johnson-Counter stages, buffered $\overline{Q}$ outputs from each stage, and counter preset control gating. CLOCK, RESET, DATA, PRESET ENABLE, and 5 individual JAM inputs are provided. Divide by 10, 8, 6, 4, or 2 counter configurations can be implemented by feeding the $\overline{Q}5$, $\overline{Q}4$, $\overline{Q}3$, $\overline{Q}2$, $\overline{Q}1$ signals, respectively, back to the DATA input. Divide-by-9, 7, 5, or 3 counter configurations can be implemented by the use of a CD4011B gate package to properly gate the feedback connection to the DATA input. Divide-by functions greater than 10 can be achieved by use of multiple CD4018B units. The counter is advanced one count at the positive clock-signal transition. Schmitt Trigger action on the clock line permits unlimited clock rise and fall times. A high RESET signal clears the counter to an all-zero condition. A high PRESET-ENABLE signal allows information on the JAM inputs to preset the counter. Anti-lock gating is provided to assure the proper counting sequence.

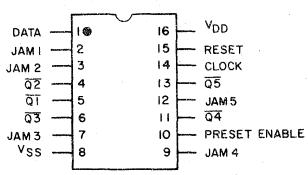
The CD4018B-series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Applications:

- Fixed and programmable divide-by-10, 9, 8, 7, 6, 5, 4, 3, 2 counters
- Fixed and programmable counters greater than 10
- Programmable decade counters
- Divide-by-"N" counters/frequency synthesizers
- Frequency division
- Counter control/timers

TERMINAL DIAGRAM

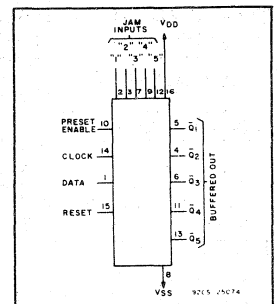
Top View



92CS-24460

Features:

- Medium speed operation . . . . . 10 MHz (typ.) at $V_{DD} - V_{SS} = 10$ V
- Fully static operation
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"



FUNCTIONAL DIAGRAM

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
									+25		
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	15, 13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5, 3.5	–	15	11				11	—	—	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

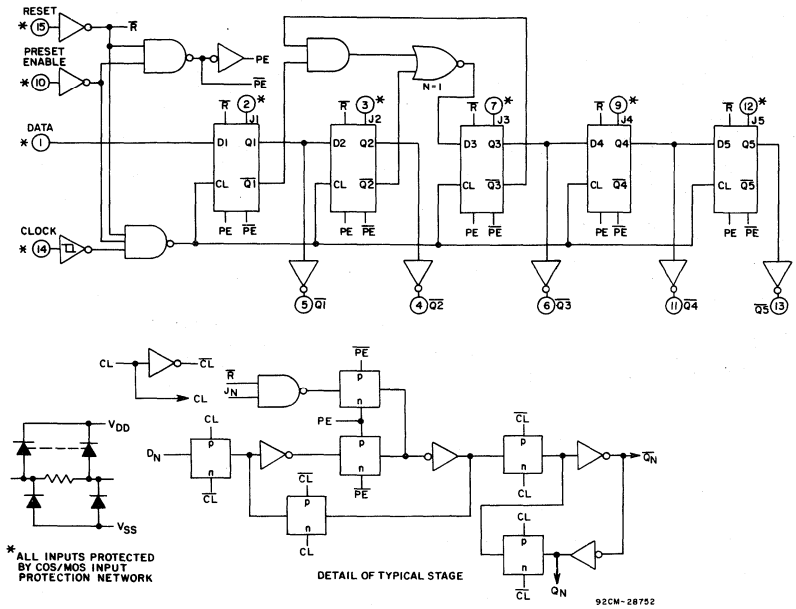
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	TYPICAL VALUES	UNITS
CLOCKED OPERATION			
Propagation Delay Time; t_{PLH}, t_{PHL}	5	180	ns
	10	90	
	15	60	
Transition Time; t_{THL}, t_{TLH}	5	100	ns
	10	50	
	15	40	
Maximum Clock Input Frequency, f_{CL}	5	5	MHz
	10	10	
	15	15	
Min. Clock Pulse Width, t_W	5	80	ns
	10	35	
	15	25	
Clock Rise & Fall Time; t_rCL, t_fCL	5	Unlimited	μs
	10		
	15		
Min. Data Input Set-Up Time, t_S	5	0	ns
	10	0	
	15	0	
Min. Data Input Hold Time, t_H	5	70	ns
	10	40	
	15	30	
Average Input Capacitance, C_I	Any Input	5	pF
PRESET* OR RESET OPERATION			
Propagation Delay Time; Reset or Reset to $\overline{Q}$ t_{PLH}, t_{PHL}	5	280	ns
	10	120	
	15	80	
Min. Preset or Reset Pulse Width t_W	5	130	ns
	10	60	
	15	40	
Min. Preset or Reset Removal Time	5	70	ns
	10	30	
	15	20	

* At PRESET ENABLE OR JAM Inputs.



*ALL INPUTS PROTECTED BY COS/MOS INPUT PROTECTION NETWORK

Fig. 1 – logic diagram.

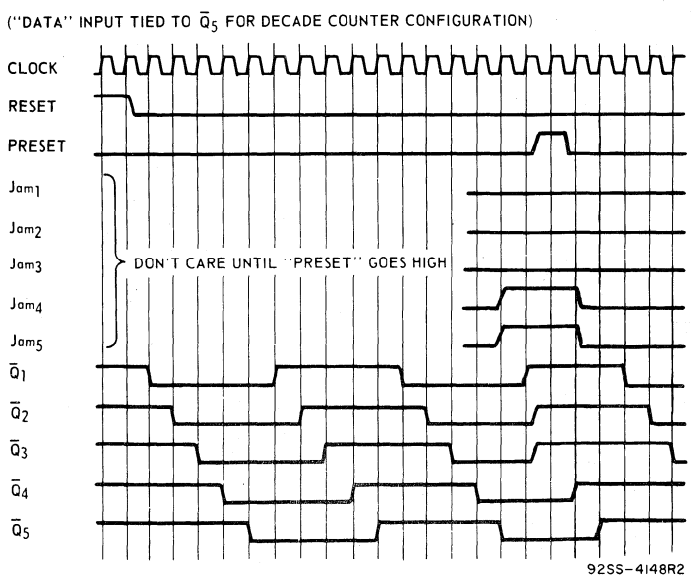


Fig. 2 – Timing diagram.

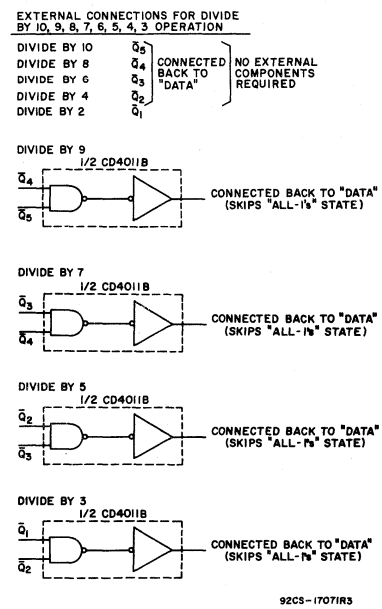


Fig. 3 – External connections for divide by 10, 9, 8, 7, 6, 5, 4, 3, 2 operation.

CD4019B Types

COS/MOS Quad AND/OR Select Gate

High-Voltage Types (20-Volt Rating)

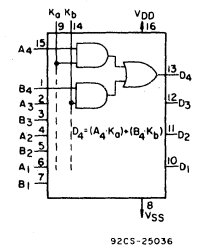
Preliminary Data

Features:

- Medium-speed operation . . . . . $t_{PHL} = t_{PLH} = 60$ ns (typ.) at $C_L = 50$ pF, $V_{DD} = 10$ V
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- AND-OR select gating
- Shift-right/shift-left registers
- True/complement selection
- AND/OR/Exclusive-OR selection



92CS-25036

CD4019B
FUNCTIONAL DIAGRAM

The RCA-CD4019B types are comprised of four AND/OR select gate configurations, each consisting of two 2-input AND gates driving a single 2-input OR gate. Selection is accomplished by control bits K_a and K_b. In addition to selection of either channel A or channel B information, the control bits can be applied simultaneously to accomplish the logical A + B function.

The CD4019B-Series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

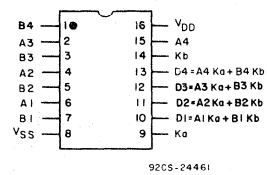
CHARACTERISTIC	V_{DD} (V)	Min.	Max.	Units
Supply-Voltage Range (For T_A = Full Package Temperature Range)	–	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . –0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = –40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
PACKAGE TYPE E . . . . . –40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

TERMINAL DIAGRAM

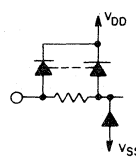
Top View



92CS-24461

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS	UNITS
		V_{DD} (V)	TYPICAL VALUES	
Propagation Delay Time; t_{PLH}, t_{PHL}		5	150	ns
		10	60	
		15	50	
Transition Time; t_{THL}, t_{TLH}		5	100	ns
		10	50	
		15	40	
Average Input Capacitance, C_I	All A and B Inputs		5	pF
	K_a and K_b Inputs		12	pF



ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55,+25,+125 Apply to D,K,F,H Pkgs. Values at −40,+25,+85 Apply to E Pkgs.							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

CD4020B, CD4024B, CD4040B Types

COS/MOS Ripple-Carry Binary Counter/Dividers

High-Voltage Types (20-Volt Rating)

CD4020B – 14 Stage
CD4024B – 7 Stage
CD4040B – 12 Stage

Preliminary Data

Features:

- Medium-speed operation
- Fully static operation
- Common reset
- Buffered inputs and outputs
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

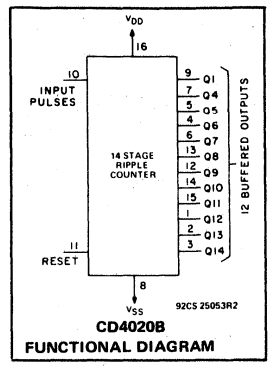
Applications:

- Control counters
- Timers
- Frequency dividers
- Time-delay circuits

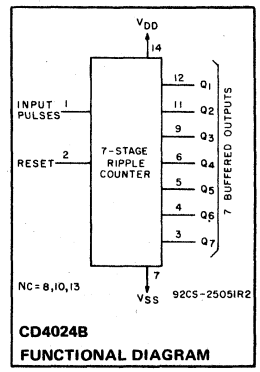
RCA-CD4020B, CD4024B, and CD4040B are ripple-carry binary counters. All counter stages are master-slave flip-flops. The state of a counter advances one count on the negative transition of each input pulse; a high level on the RESET line resets the counter to its all zeros state. Schmitt trigger action on the input-pulse line permits unlimited clock rise and fall times. All inputs and outputs are buffered.

The CD4020B, CD4024B and CD4040B-series types are supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead dual-in-line plastic packages (K suffix), and in chip form (H suffix).

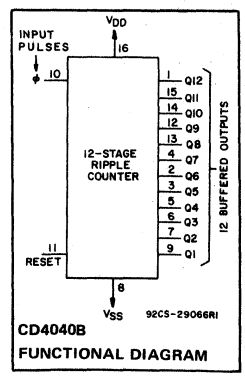
The CD4024B-series types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).



CD4020B
FUNCTIONAL DIAGRAM



CD4024B
FUNCTIONAL DIAGRAM



CD4040B
FUNCTIONAL DIAGRAM

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D,K,F,H Packages Values at –40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	–40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5, 13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1, 9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

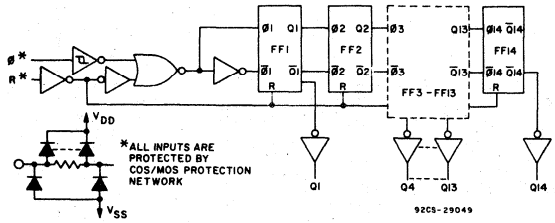


Fig. 1 – Logic diagram for CD4020B.

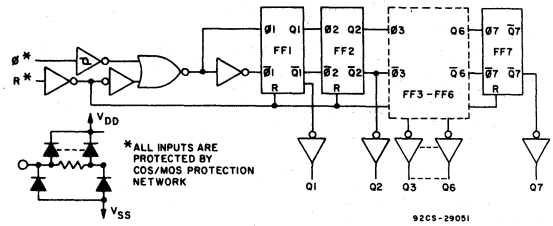


Fig. 2 – Logic diagram for CD4024B.

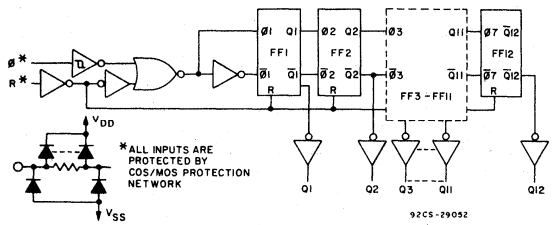


Fig. 3 – Logic diagram for CD4040B.

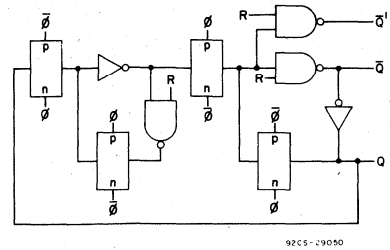
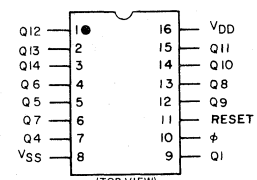


Fig. 4 – Detail of typical flip-flop stage.

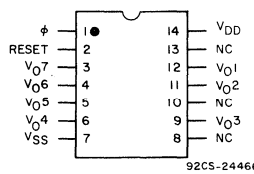
TERMINAL ASSIGNMENT

Top View

CD4020B

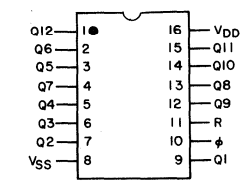


CD4024B



NC = No Connection

CD4040B



RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, V_{DD} (Voltages referenced to V_{SS} terminal) . . . −0.5 to +20 V

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V

POWER DISSIPATION PER PACKAGE (P_D):

For T_A = −40 to +60°C (Package Type E) . . . . . 500 mW

For T_A = +60 to +85°C (Package Type E) . . . . . Derate Linearly to 200 mW

For T_A = −55 to +100°C (Package Types D,K,H) . . . . . 500 mW

For T_A = +100 to +125°C (Package Types D,K,H) Derate Linearly to 100 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR:

For T_A = Full package-temperature range (All package types) . . . . . 100 mW

OPERATING-TEMPERATURE RANGE (T_A):

Package Types D,K,H . . . . . −55 to +125°C

Package Type E . . . . . −40 to +85°C

STORAGE-TEMPERATURE RANGE (T_{STG}) . . . . . −65 to 150°C

LEAD TEMPERATURE (During Soldering):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	LIMITS TYPICAL VALUES	UNITS
Input-Pulse Operation				
Propagation Delay Time, ϕ_1 to Q_1 Out; t_{PHL}, t_{PLH}		5	400	ns
		10	170	
		15	120	
Propagation Delay Time, Q_n to $Q_n + 1$; t_{PHL}, t_{PLH}		5	200	ns
		10	85	
		15	60	
Transition Time, t_{THL}, t_{TLH}		5	100	ns
		10	50	
		15	40	
Minimum Input-Pulse Width, t_W	f = 100 kHz	5	70	ns
		10	30	
		15	20	
Input-Pulse Rise or Fall Time, $t_{r\phi}$, $t_{f\phi}$		5	Unlimited	μs
		10		
		15		
Maximum Input-Pulse Frequency, f_ϕ		5	7	MHz
		10	16	
		15	24	
Input Capacitance, C_I	Any Input		5	pF
Reset Operation				
Propagation Delay Time, t_{PHL}		5	300	ns
		10	140	
		15	100	
Minimum Reset Pulse Width, t_W		5	375	ns
		10	200	
		15	150	

Preliminary Data

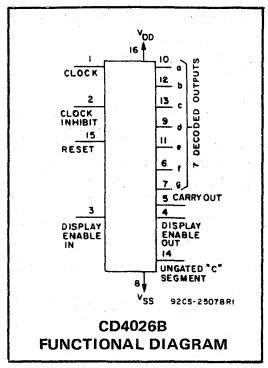
COS/MOS Decade Counters/Dividers

High-Voltage Types (20-Volt Rating)

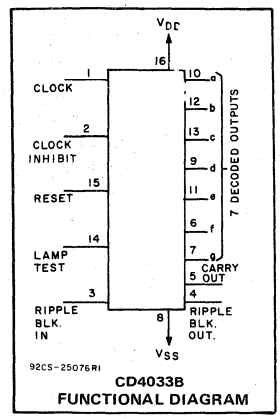
With Decoded 7-Segment Display Outputs and:
Display Enable – CD4026B
Ripple Blanking – CD4033B

Features:

- **Counter and 7-segment decoding in one package**
- **Easily interfaced with 7-segment display types**
- **Fully static counter operation: DC to 6 MHz (typ.) at V_{DD}=10 V**
- **Ideal for low-power displays**
- **Display enable output (CD4026B)**
- **"Ripple blanking" and lamp test (CD4033B)**
- **100% tested for quiescent current at 20 V**
- **Standardized, symmetrical output characteristics**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No.13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**



CD4026B
FUNCTIONAL DIAGRAM



CD4033B
FUNCTIONAL DIAGRAM

Applications

- **Decade counting 7-segment decimal display**
- **Frequency division 7-segment decimal displays**
- **Clocks, watches, timers (e.g. ÷60, ÷ 60, ÷ 12 counter/display)**
- **Counter/display driver for meter applications**

The RCA-CD4026B and CD4033B each consist of a 5-stage Johnson decade counter and an output decoder which converts the Johnson code to a 7-segment decoded output for driving one stage in a numerical display.

These devices are particularly advantageous in display applications where low power dissipation and/or low package count are important.

Inputs common to both types are CLOCK, RESET, & CLOCK INHIBIT; common outputs are CARRY OUT and the seven decoded outputs (a, b, c, d, e, f, g). Additional inputs and outputs for the CD4026B include DISPLAY ENABLE input and DISPLAY ENABLE and UNGATED "C-SEGMENT" outputs. Signals peculiar to the CD4033B are RIPPLE-BLANKING INPUT AND LAMP TEST INPUT and a RIPPLE-BLANKING OUTPUT.

A high RESET signal clears the decade counter to its zero count. The counter is advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. Antilock gating is provided on the JOHNSON counter, thus assuring proper counting sequence. The CARRY-OUT (C_{out}) signal completes one cycle every ten CLOCK INPUT cycles and is used to clock the succeeding decade directly in a multi-decade counting chain.

The seven decoded outputs (a, b, c, d, e, f, g) illuminate the proper segments in a seven segment display device used for representing the decimal numbers 0 to 9. The 7-segment outputs go high on selection in the CD4033B; in the CD4026B these outputs go high only when the DISPLAY ENABLE IN is high.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D,K,F,H Packages Values at –40, +25, +85 Apply to E Package							UNITS
									+25		
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	–40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	-	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

CD4026B

When the DISPLAY ENABLE IN is low the seven decoded outputs are forced low regardless of the state of the counter. Activation of the display only when required results in significant power savings. This system also facilitates implementation of display-character multiplexing.

The CARRY OUT and UNGATED "C-SEGMENT" signals are not gated by the DISPLAY ENABLE and therefore are available continuously. This feature is a requirement in implementation of certain divider functions such as divide-by-60 and divide-by-12.

CD4033B

The CD4033B has provisions for automatic blanking of the non-significant zeros in a multi-digit decimal number which results in an easily readable display consistent with normal writing practice. For example, the number 0050.07000 in an eight digit display would be displayed as 50.07. Zero suppression on the integer side is obtained by connecting the RBI terminal of the CD4033B associated with the most significant digit in the display to a low-level voltage and connecting the RBO terminal of that stage to the RBI terminal of the CD4033B in the next-lower significant position in the display. This procedure is continued for each succeeding CD4033B on the integer side of the display.

On the fraction side of the display the RBI of the CD4033B associated with the least significant bit is connected to a low-level voltage and the RBO of that CD4033B is connected to the RBI terminal of the CD4033B in the next more-significant-bit position. Again, this procedure is continued for all CD4033B's on the fraction side of the display.

In a purely fractional number the zero immediately preceding the decimal point can be displayed by connecting the RBI of that stage to a high level voltage (instead of to the RBO of the next more-significant-stage). For example: optional zero → 0.7346. Likewise, the zero in a number such as 763.0 can be displayed by connecting the RBI of the CD4033B associated with it to a high-level voltage.

Ripple blanking of non-significant zeros provides an appreciable savings in display power.

The CD4033B has a LAMP TEST input which, when connected to a high-level voltage, overrides normal decoder operation and enables a check to be made on possible display malfunctions by putting the seven outputs in the high state.

The CD4026B- and CD4033B-series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

DYNAMIC ELECTRICAL CHARACTERISTICS *at $T_A = 25^oC$, Input t_r, $t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200$ kΩ*

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	LIMITS TYPICAL VALUES	UNITS
CLOCKED OPERATION				
Propagation Delay Time; t_{PLH}, t_{PHL} Carry Out Line		5	280	ns
		10	125	
		15	90	
Decode Out lines		5	475	ns
		10	220	
		15	160	
Transition Time; t_{THL}, t_{TLH} Carry Out Line		5	100	ns
		10	50	
		15	40	
Maximum Clock Input Frequency, f_{CL}▲		5	3	MHz
		10	6	
		15	7.5	
Min. Clock Pulse Width, t_W		5	150	ns
		10	70	
		15	50	
Clock Rise or Fall Time; t_{rCL}, t_{fCL}		5	Unlimited	μs
		10		
		15		
Min. Clock Inhibit Set Up Time, t_S		5	60	ns
		10	30	
		15	20	
Average Input Capacitance, C_{IN}	Any Input		5	pF
RESET OPERATION				
Propagation Delay Time; t_{PLH}, t_{PHL} To Carry Out Line		5	250	ns
		10	120	
		15	85	
To Decode Out Lines		5	450	ns
		10	210	
		15	150	
Min. Reset Pulse Width, t_W		5	200	ns
		10	100	
		15	80	
Min. Reset Removal Time		5	150	ns
		10	70	
		15	50	

▲ Measured with respect to carry out line.

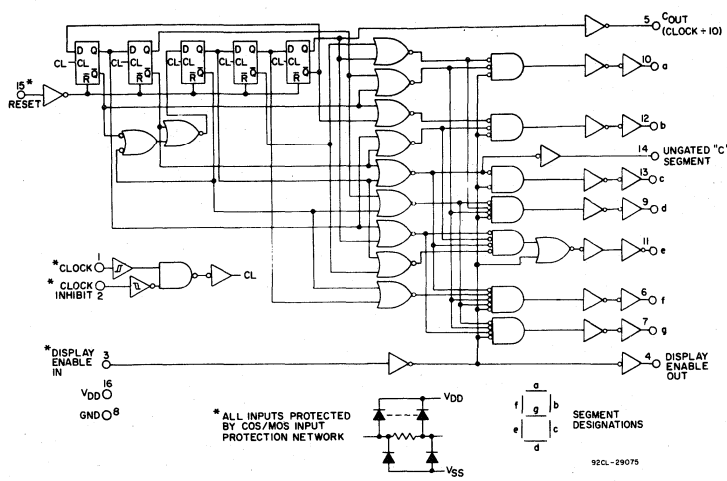


Fig.1 – CD4026B logic diagram.

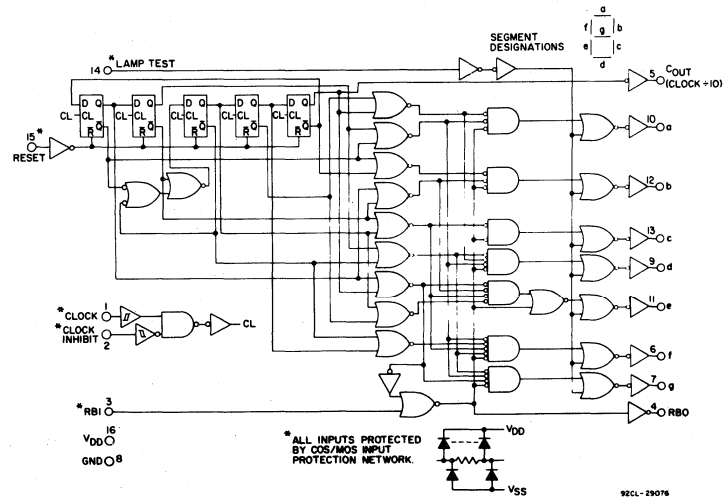


Fig.2 – CD4033B logic diagram.

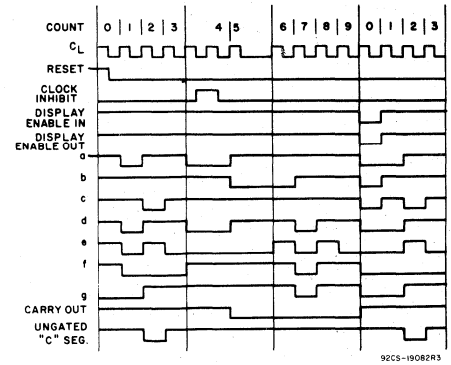


Fig.3 – CD4026B timing diagram.

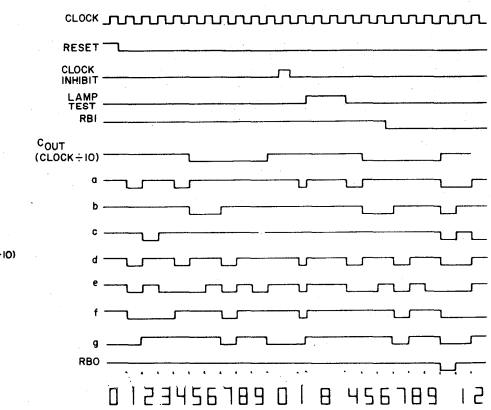


Fig.4 – CD4033B timing diagram.

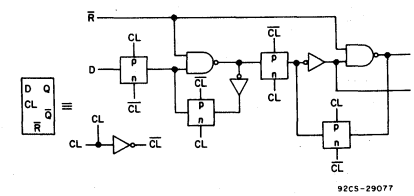
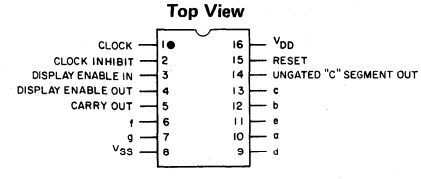


Fig.5 – Detail of typical flip-flop stage for both types.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

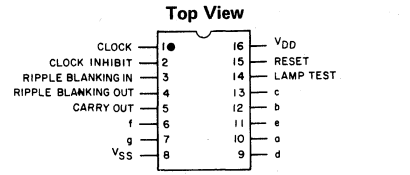
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

Top View



CD4026B

Top View



CD4033B

COS/MOS Dual J-K Master-Slave Flip-Flop

High-Voltage Types (20-Volt Rating)

The RCA-CD4027B is a single monolithic chip integrated circuit containing two identical complementary-symmetry J-K master-slave flip-flops. Each flip-flop has provisions for individual J, K, Set, Reset, and Clock input signals. Buffered Q and $\overline{Q}$ signals are provided as outputs. This input-output arrangement provides for compatible operation with the RCA-CD4013B dual D-type flip-flop.

The CD4027B is useful in performing control, register, and toggle functions. Logic levels present at the J and K inputs along with internal self-steering control the state of each flip-flop; changes in the flip-flop state are synchronous with the positive-going transition of the clock pulse. Set and reset functions are independent of the clock and are initiated when a high level signal is present at either the Set or Reset input.

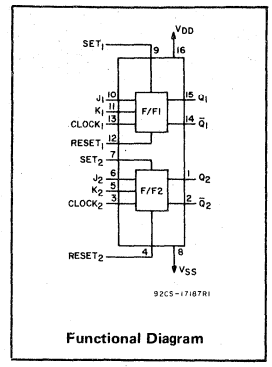
Features:

- **Set-Reset capability**
- **Static flip-flop operation — retains state indefinitely with clock level either "high" or "low"**
- **Medium speed operation — 16 MHz (typ.) clock toggle rate at 10 V**
- **Standardized symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (over full package-temperature range):**
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

- **Registers, counters, control circuits**

The CD4027B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K) suffix), and in chip form (H suffix).



Functional Diagram

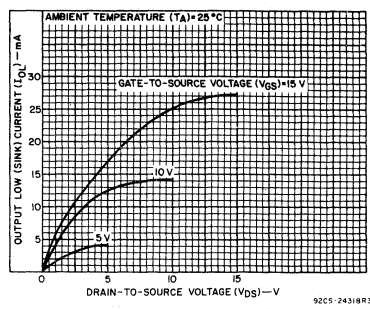


Fig.1 — Typical output low (sink) current characteristics.

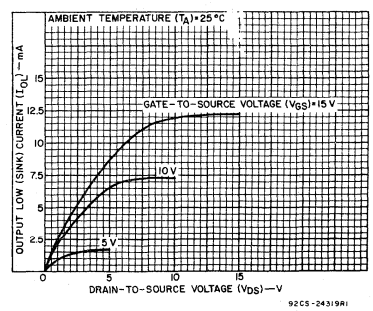


Fig.2 — Minimum output low (sink) current characteristics.

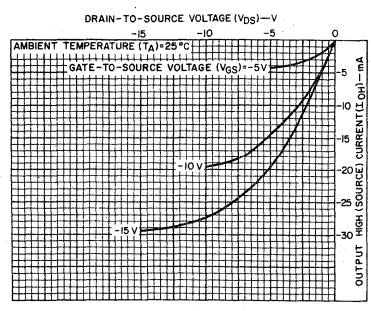


Fig.3 — Typical output high (source) current characteristics.

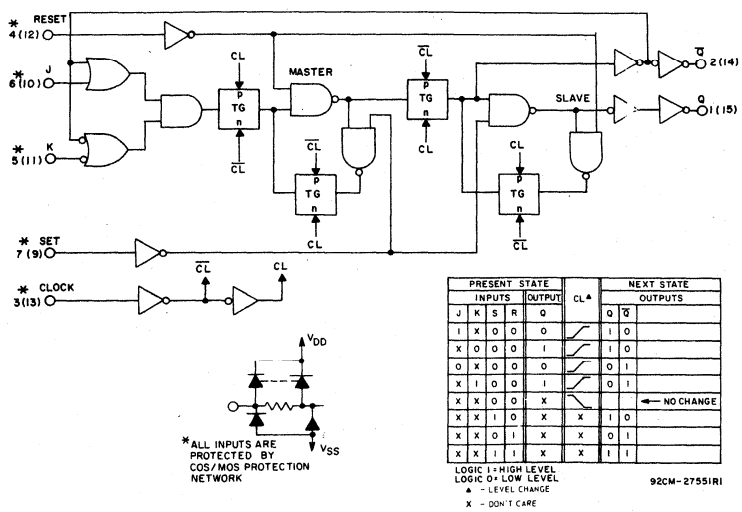
STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55,+25,+125 Apply to D,K,F,H Pkgs. Values at −40,+25,+85 Apply to E Pkgs.							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		V_{DD} (V)	LIMITS All Packages Min.	LIMITS All Packages Max.	UNITS
Supply-Voltage Range (For T_A = Full Package Temperature Range)		–	3	18	V
Data Setup Time	t_S	5	200	–	ns
		10	75	–	
		15	50	–	
Clock Pulse Width	t_W	5	140	–	ns
		10	60	–	
		15	40	–	
Clock Input Frequency (Toggle Mode)	f_{CL}	5		3.5	MHz
		10	dc	8	
		15		12	
Clock Rise or Fall Time	t_rCL*, t_fCL	5	–	15	μs
		10	–	4	
		15	–	1	
Set or Reset Pulse Width	t_W	5	180	–	ns
		10	80	–	
		15	50	–	

* If more than one unit is cascaded in a parallel clocked operation, t_rCL should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.



PRESENT STATE INPUTS J	K	S	R	PRESENT STATE OUTPUT Q	CL▲	NEXT STATE OUTPUTS Q	Q̄	
1	X	0	0	0		1	0	
X	0	0	0	1		1	0	
0	X	0	0	0		0	1	
X	1	0	0	1		0	1	
X	X	0	0	X				← NO CHANGE
X	X	1	0	X		1	0	
X	X	0	1	X		0	1	
X	X	1	1	X		1	1	

LOGIC 1 = HIGH LEVEL
LOGIC 0 = LOW LEVEL
▲ – LEVEL CHANGE
X – DON'T CARE

92CM-27551RI

Fig.7 – Logic diagram and truth table for CD4027B (one of two identical J-K flip flops).

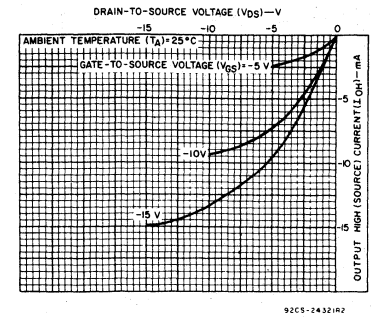


Fig.4 – Minimum output high (source) current characteristics.

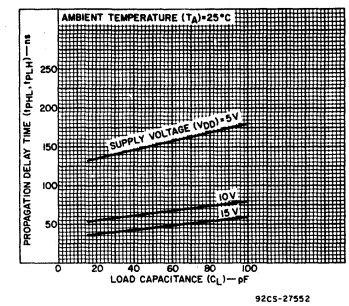


Fig.5 – Typical propagation delay time vs. load capacitance (CLOCK or SET to Q, CLOCK or RESET to Q̄.

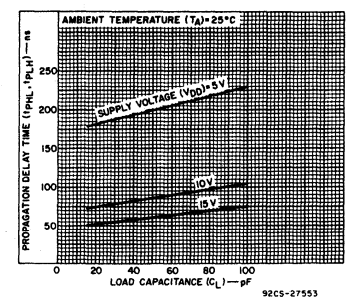


Fig.6 – Typical propagation delay time vs. load capacitance (SET to Q̄ or RESET to Q).

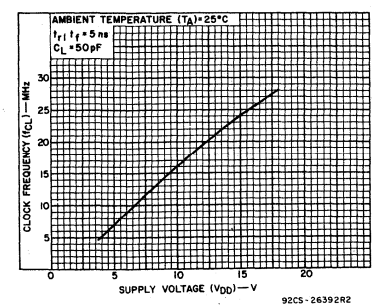


Fig.8 – Typical maximum clock frequency vs. supply voltage (toggle mode).

CD4027B Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

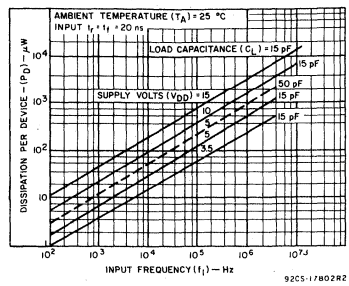


Fig.9 – Typical power dissipation vs. frequency.

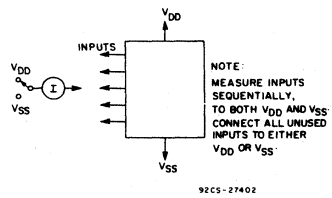


Fig.10 – Input current test circuit.

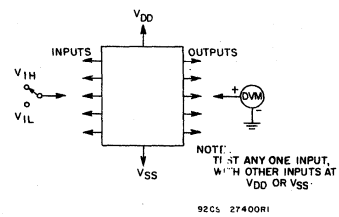


Fig.11 – Input-voltage test circuit.

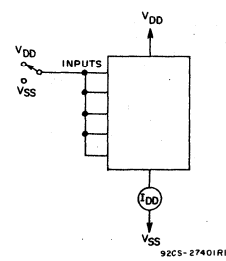
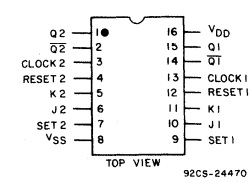


Fig.12 – Quiescent device current test circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

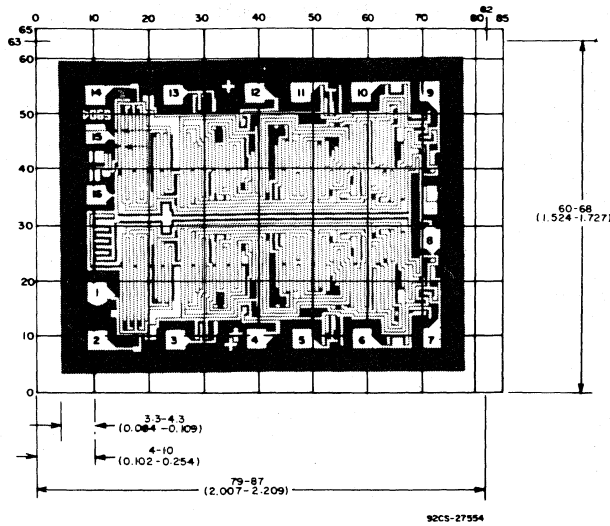
CHARACTERISTIC	V_{DD} (V)	LIMITS All Packages Min.	Typ.	Max.	UNITS
Propagation Delay Time: Clock to Q or $\overline{Q}$ Outputs t_{PHL}, t_{PLH}	5	–	150	300	ns
	10	–	65	130	
	15	–	45	90	
Set to Q or Reset to $\overline{Q}$ t_{PLH}	5	–	150	300	ns
	10	–	65	130	
	15	–	45	90	
Set to $\overline{Q}$ or Reset to Q t_{PHL}	5	–	200	400	ns
	10	–	85	170	
	15	–	60	120	
Transition Time t_{THL}, t_{TLH}	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Maximum Clock Input Frequency# (Toggle Mode) f_{CL}	5	3.5	7	–	MHz
	10	8	16	–	
	15	12	24	–	
Minimum Clock Pulse Width t_W	5	–	70	140	ns
	10	–	30	60	
	15	–	20	40	
Minimum Set or Reset Pulse Width t_W	5	–	90	180	ns
	10	–	40	80	
	15	–	25	50	
Minimum Data Setup Time t_S	5	–	100	200	ns
	10	–	35	75	
	15	–	25	50	
Clock Input Rise or Fall Time t_{rCL}, t_{fCL}	5	–	–	15	μs
	10	–	–	4	
	15	–	–	1	
Input Capacitance C_I		–	5	7.5	pF

Input t_r, t_f = 5 ns.



TERMINAL ASSIGNMENT

Dimensions and Pad Layout for CD4027BH



Dimensions in millimeters are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3}).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS BCD-to-Decimal Decoder

High-Voltage Types (20-Volt Rating)

The RCA-CD4028B types are BCD-to-decimal or binary-to-octal decoders consisting of buffering on all 4 inputs, decoding-logic gates, and 10 output buffers. A BCD code applied to the four inputs, A to D, results in a high level at the selected one of 10 decimal decoded outputs. Similarly, a 3-bit binary code applied to inputs A through C is decoded in octal code at output 0 to 7 if D = "0". High drive capability is provided at all outputs to enhance dc and dynamic performance in high fan-out applications.

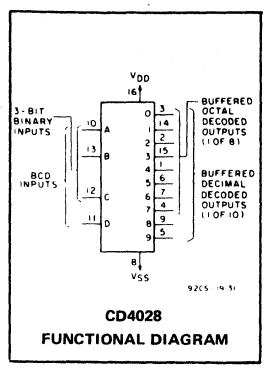
The CD4028B-Series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

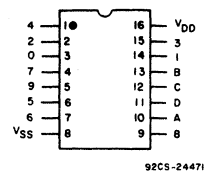
- BCD-to-decimal decoding or binary-to-octal decoding
- High decoded output drive capability
- "Positive logic" inputs and outputs. . . .
  . . . . . decoded outputs go high on selection
- Medium-speed operation. . . .
  t_{PHL}, t_{PLH} = 80 ns (typ.) @ V_{DD} = 10 V
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range):
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Code conversion
- Indicator-tube decoder
- Address decoding—memory selection control



CD4028
FUNCTIONAL DIAGRAM



Top View
TERMINAL DIAGRAM

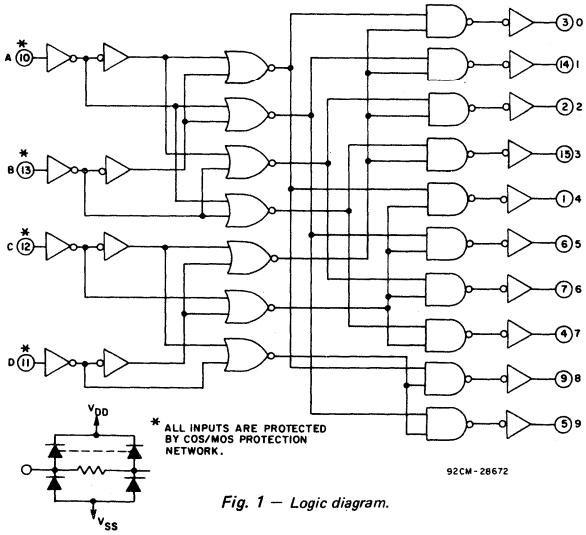


Fig. 1 — Logic diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

TABLE I – TRUTH TABLE

D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1
1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

1 = HIGH LEVEL 0 = LOW LEVEL

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1, 9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $C_L = 50$ pF, Input $t_r, t_f = 20$ ns, $R_L = 200$ kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS
	V_{DD} (V)	Typ.	Max.	
Propagation Delay Time: t_{PHL}, t_{PLH}	5	175	350	ns
	10	80	160	
	15	60	120	
Transition Time t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Input Capacitance, C_{IN}	–	5	7.5	pF

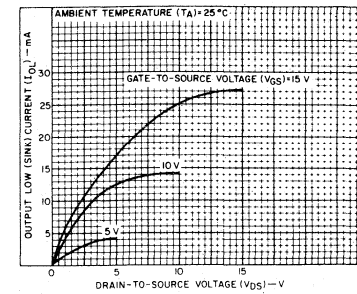


Fig. 2 — Typical output low (sink) current characteristics.

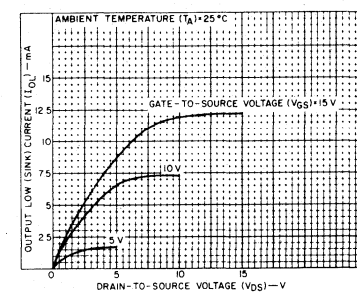


Fig. 3 — Minimum output low (sink) current characteristics.

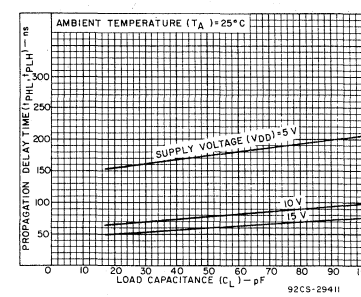


Fig. 4 — Typical propagation delay time as a function of load capacitance.

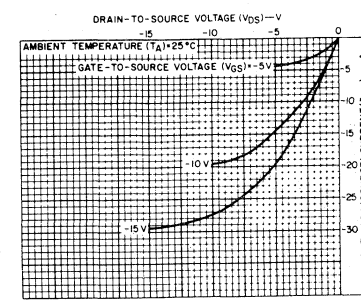


Fig. 5 — Typical output high (source) current characteristics.

TABLE II – CODE CONVERSION CHART

INPUTS				INPUT CODES						OUTPUT NUMBER																
				Hexa-Decimal		Decimal																				
D	C	B	A	4-BIT BINARY	4-BIT GRAY	EXCESS-3	EXCESS-3 GRAY	AIKEN	4-2-2-1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0			0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	1			1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	2	3		0	2	2	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	3	2	0	3	3		0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	4	7	1	4	4		0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	5	6	2			3	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	1	1	0	6	4	3	1		4	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	1	1	1	7	5	4	2			0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	0	8	15	5				0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	9	14	6			5	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
1	0	1	0	10	12	7	9		6	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
1	0	1	1	11	13	8		5		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1	1	0	0	12	8	9	5	6		0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
1	1	0	1	13	9		6	7	7	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
1	1	1	0	14	11		8	8	8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	1	1	1	15	10		7	9	9	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

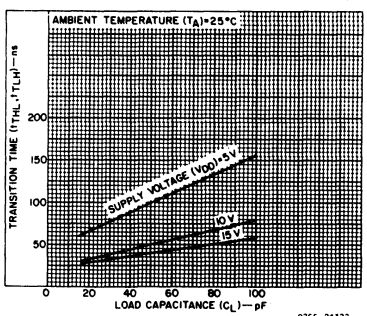


Fig. 8 – Typical transition time as a function of load capacitance.

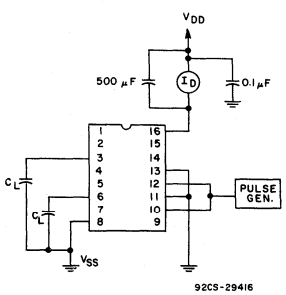


Fig. 10 – Dynamic power dissipation test circuit.

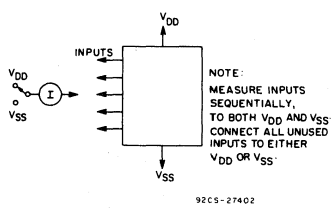


Fig. 9 – Input current test circuit.

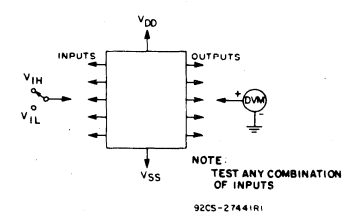


Fig. 11 – Input voltage test circuit.

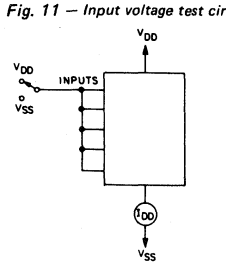


Fig. 12 – Quiescent device current test circuit.

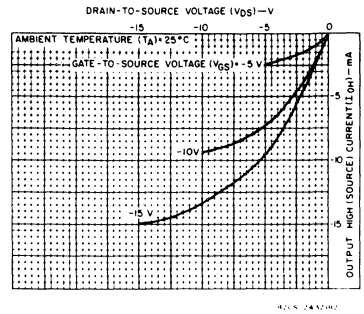


Fig. 6 – Minimum output high (source) current characteristics.

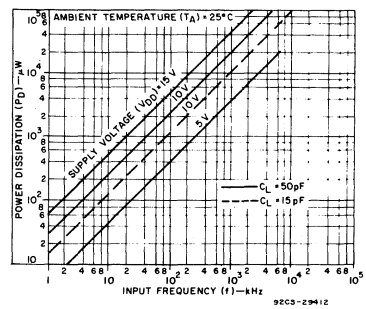


Fig. 7 – Typical dynamic power dissipation as a function of input frequency.

TYPICAL APPLICATIONS

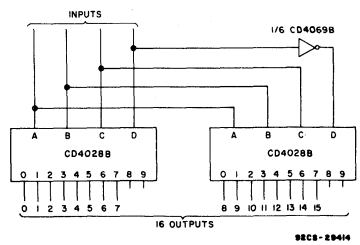
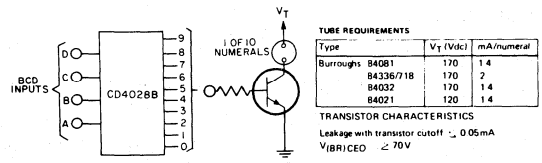


Fig. 13 – Code conversion circuit.

The circuit shown in Fig.13 converts any 4-bit code to a decimal or hexadecimal code. Table 2 shows a number of codes and the decimal or hexadecimal number in these codes which must be applied to the input terminals of the CD4028B to select a particular output. For example: in order to get a high on output No. 8 the input must be either an 8 expressed in 4-Bit Binary code, a 15 expressed in 4-Bit Gray code, or a 5 expressed in Excess-3 code.



▲(Trademark) Burroughs Corp.

Fig. 14 — Neon readout (Nixie Tube▲) display application.

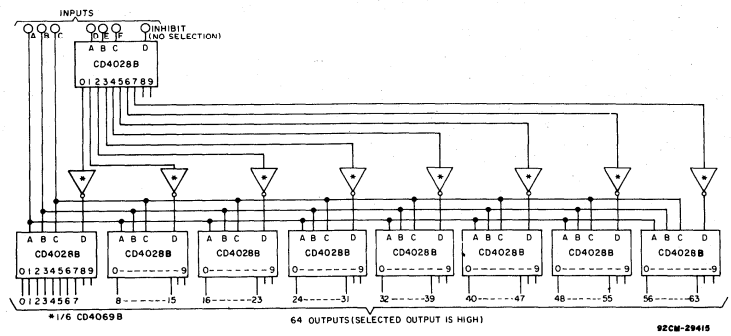
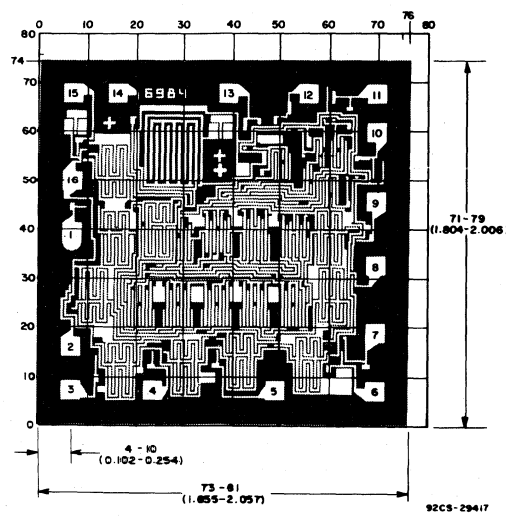


Fig. 15 — 6-bit binary to 1-of-64 address decoder.



CD4028BH
DIMENSIONS AND PAD LAYOUT

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CD4029B Types

COS/MOS Presettable Up/Down Counter

Binary or BCD-Decade

High-Voltage Types (20-Volt Rating)

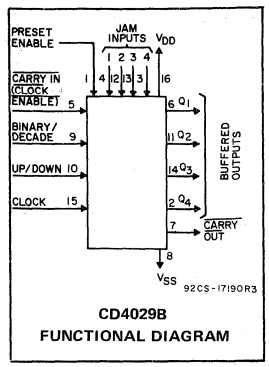
Preliminary Data

Features:

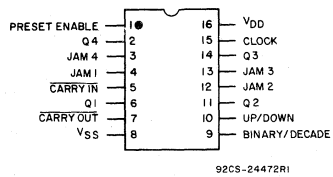
- Medium-speed operation . . . 10 MHz (typ.) @ C_L = 50 pF and $V_{DD}-V_{SS}$ = 10 V
- Multi-package parallel clocking for synchronous high speed output response or ripple clocking for slow clock input rise and fall times
- "Preset Enable" and individual "Jam" inputs provided
- Binary or decade up/down counting
- BCD outputs in decade mode
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Programmable binary and decade counting/frequency synthesizers-BCD output
- Analog to digital and digital to analog conversion
- Up/Down binary counting
- Magnitude and sign generation
- Up/Down decade counting
- Difference counting



CD4029B
FUNCTIONAL DIAGRAM



CD4029B Terminal Diagram

The RCA-CD4029B consists of a four-stage binary or BCD-decade up/down counter with provisions for look-ahead carry in both counting modes. The inputs consist of a single CLOCK, CARRY-IN (CLOCK ENABLE), BINARY/DECADE, UP/DOWN, PRESET ENABLE, and four individual JAM signals. Q1, Q2, Q3, Q4 and a CARRY OUT signal are provided as outputs.

A high PRESET ENABLE signal allows information on the JAM INPUTS to preset the counter to any state asynchronously with the clock. A low on each JAM line, when the PRESET-ENABLE signal is high, resets the counter to its zero count. The counter is advanced one count at the positive transition of the clock when the CARRY-IN and PRESET ENABLE signals are low. Advancement is inhibited when the CARRY-IN or PRESET ENABLE signals are high. The CARRY-OUT signal is normally high and goes low when the counter reaches its maximum count in the UP mode or the minimum count in the DOWN mode provided the CARRY-IN signal is low. The CARRY-IN signal in the low state can thus be considered a CLOCK ENABLE. The CARRY-IN terminal must be connected to V_{SS} when not in use.

Binary counting is accomplished when the BINARY/DECADE input is high; the counter counts in the decade mode when the BINARY/DECADE input is low. The counter counts Up when the UP/DOWN INPUT is high, and Down when the UP/DOWN INPUT is low. Multiple packages can be connected in either a parallel-clocking or a ripple-clocking arrangement as shown in Fig. 6.

Parallel clocking provides synchronous control and hence faster response from all counting outputs. Ripple-clocking allows for longer clock input rise and fall times.

The CD4029B-series types are supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Recommended Operating Conditions
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V_{DD} (V)	Min.	Max.	Units
Supply-Voltage Range (T_A=Full Package Temperature Range)	–	3	18	V

STATIC ELECTRICAL CHARACTERISTICS

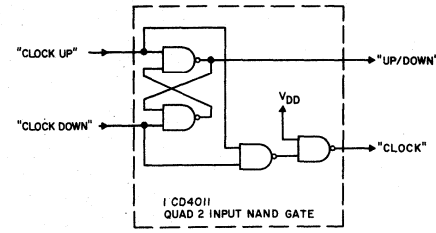
CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
									+25		
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS TYPICAL VALUES	UNITS
Clocked Operation			
Propagation Delay Time: t_{PHL}, t_{PLH} Q Outputs	5	165	ns
	10	75	
	15	55	
Carry Output	5	280	
	10	130	
	15	95	
Transition Time: t_{THL}, t_{TLH} Q Outputs, Carry Output	5	100	ns
	10	50	
	15	40	
Minimum Clock Pulse Width, t_W	5	60	ns
	10	30	
	15	24	
Clock Rise & Fall Time, t_rCL, t_fCL**	5	>200	μs
	10		
	15		
Minimum Setup Times, t_S* Carry In	5	30	ns
	10	10	
	15	6	
B/D or U/D	5	150	
	10	70	
	15	50	
Maximum Clock Input Frequency, f_{CL}	5	4.6	MHz
	10	10	
	15	14	
Input Capacitance, C_I	Any Input	5	pF
Preset Enable			
Propagation Delay Time: t_{PHL}, t_{PLH} Q Outputs	5	200	ns
	10	90	
	15	65	
Carry Output	5	320	
	10	145	
	15	105	
Minimum Preset Enable Pulse Width, t_W	5	50	ns
	10	35	
	15	25	
Minimum Preset Enable Removal Time, t_{rem}*	5	120	ns
	10	55	
	15	40	
Carry Input			
Propagation Delay Time: t_{PHL}, t_{PLH} Carry Output	5	140	ns
	10	70	
	15	50	

* From Up/Down, Binary/Decode, Carry In, or Preset Enable Control Inputs to Clock Edge.

** If more than one unit is cascaded in the parallel clocked application, t_rCL should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transition time of the carry output driving stage for the estimated capacitive load.



92CS-17195R2

The CD4029B CLOCK and UP/DOWN inputs are used directly in most applications. In applications where CLOCK UP and CLOCK DOWN inputs are provided, conversion to the CD4029B CLOCK and UP/DOWN inputs can easily be realized by use of the circuit in Fig. 1.

CD4029B changes count on positive transitions of CLOCK UP or CLOCK DOWN inputs. For the gate configuration shown below, when counting up the CLOCK DOWN input must be maintained high and conversely when counting down the CLOCK UP input must be maintained high.

Fig. 1 – Conversion of clock up, clock down input signals to clock and up/down input signals.

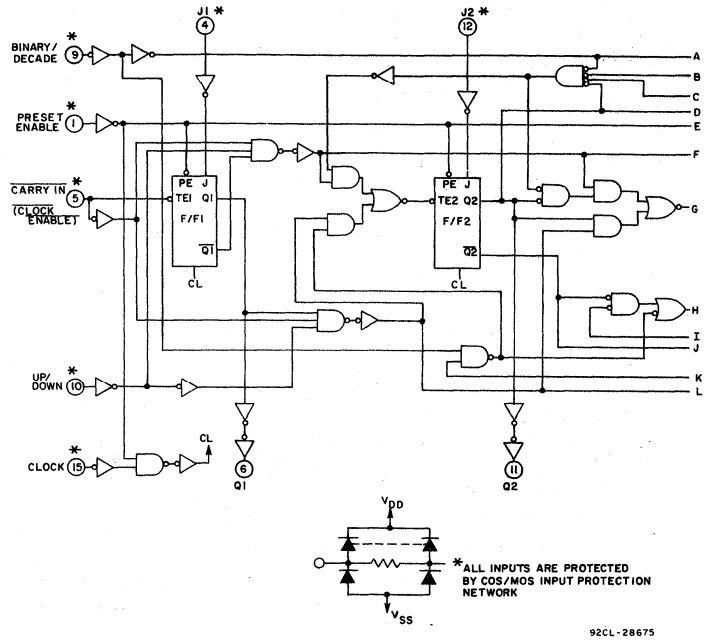


Fig. 2 – Logic diagram.

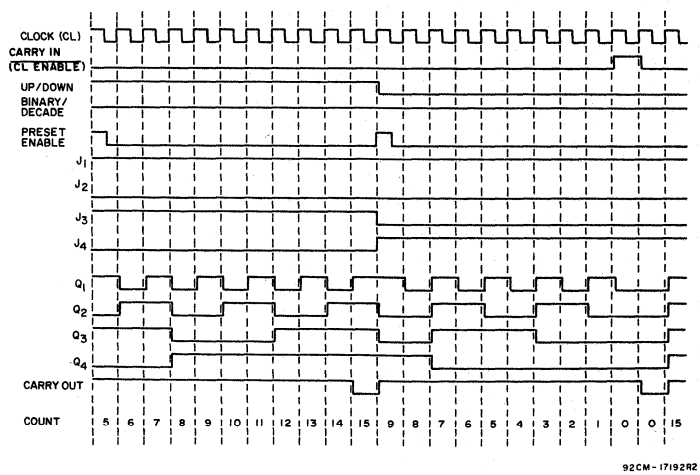
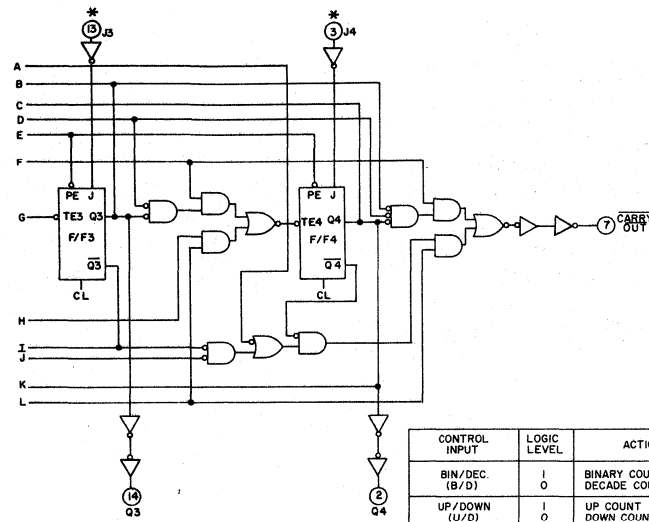
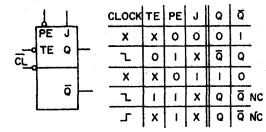


Fig. 3 – Timing diagram-binary mode.



TRUTH TABLE



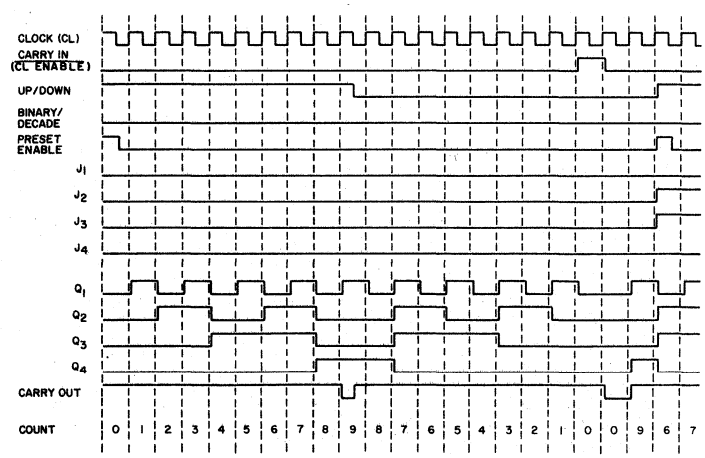
CLOCK	TE	PE	J	Q	$\overline{Q}$
X	X	0	0	0	1
↓	0	1	X	$\overline{Q}$	Q
X	X	0	1	1	0
↓	1	1	X	Q	$\overline{Q}$ NC
↑	X	1	X	Q	$\overline{Q}$ NC

X-DON'T CARE

CONTROL INPUT	LOGIC LEVEL	ACTION
BIN/DEC. (B/D)	1	BINARY COUNT
	0	DECADE COUNT
UP/DOWN (U/D)	1	UP COUNT
	0	DOWN COUNT
PRESET ENABLE (PE)	1	JAM IN
	0	NO JAM
$\overline{\text{CARRY IN (CI)}}$ (CLOCK ENABLE)	1	NO COUNTER ADVANCE AT POS. CLOCK TRANSITION
	0	ADVANCE COUNTER AT POS. CLOCK TRANSITION

92CL-28675

Fig. 2 – Logic diagram (cont'd).

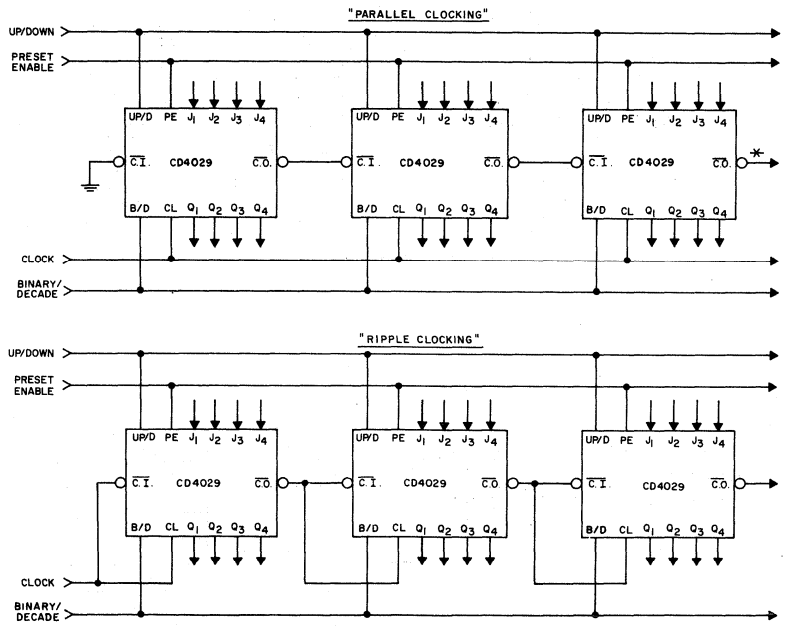


92CM-17193R3

Fig. 4 – Timing diagram-decade mode.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C



Ripple Clocking Mode:
The Up/Down control can be changed at any count. The only restriction on changing the Up/Down control is that the clock input to the first counting stage must be high.

*$\overline{\text{CARRY OUT}}$ lines at the 2nd, 3rd, etc., stages may have a negative-going glitch pulse resulting from differential delays of different CD4029B IC's. These negative-going glitches do not affect proper CD4029B operation. However, if the $\overline{\text{CARRY OUT}}$ signals are used to trigger other edge-sensitive logic devices, such as FF's or counters, the $\overline{\text{CARRY OUT}}$ signals should be gated with the clock signal using a 2-input OR gate such as CD4071B.

Fig. 5 – Cascading counter packages.

Preliminary Data

COS/MOS Quad Exclusive-OR Gate

High-Voltage Types (20-Volt Rating)

The RCA-CD4030B types consist of four independent Exclusive-OR gates integrated on a single monolithic silicon chip. Each Exclusive-OR gate consists of four n-channel and four p-channel enhancement-type transistors. All inputs and outputs are protected against electrostatic effects.

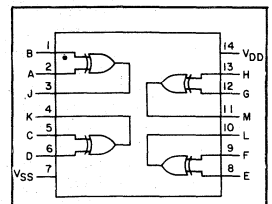
The CD4030B-series types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- Medium-speed operation. . . . . $t_{PHL} = t_{PLH} = 60$ ns (typ) @ $C_L = 50$ pF and $V_{DD}-V_{SS} = 10$ V
- Low output impedance . . . . . 500 Ω (typ.) @ $V_{DD}-V_{SS} = 10$ V
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of "B" Series CMOS Devices"

Applications:

- Even and odd-parity generators and checkers
- Logical comparators
- Adders/subtractors
- General logic functions

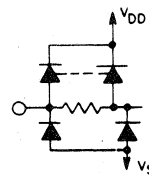


FUNCTIONAL DIAGRAM

TRUTH TABLE FOR ONE OF FOUR IDENTICAL GATES

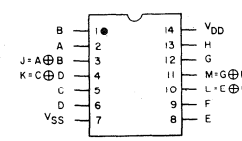
A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

WHERE "1" = HIGH LEVEL
"0" = LOW LEVEL



All inputs (Terminals 1, 2, 5, 6, 8, 9, 12, and 13) protected by COS/MOS input protection network.

TERMINAL DIAGRAM
Top View



STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55,+25,+125 Apply to D,K,F,H Pkgs. Values at −40,+25,+85 Apply to E Pkgs.							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		TYPICAL VALUES	UNITS
		V_{DD} (V)		
Propagation Delay Time: t_{PLH}, t_{PHL}		5	150	ns
		10	60	
		15	45	
Transition Time: t_{TLH}, t_{THL}		5	100	ns
		10	50	
		15	40	
Average Input Capacitance, C_I	Any Input		5	pF

COS/MOS 64-Stage Static Shift Register

High-Voltage Types (20-Volt Rating)

Preliminary Data

The RCA-CD4031B is a static shift register that contains 64 D-type, master-slave flip-flop stages and one stage which is a D-type master flip-flop only (referred to as a 1/2 stage).

The logic level present at the DATA input is transferred into the first stage and shifted one stage at each positive-going clock transition. Maximum clock frequencies up to 16 Megahertz (typical) can be obtained. Because fully static operation is allowed, information can be permanently stored with the clock line in either the low or high state. The CD4031B has a MODE CONTROL input that, when in the high state, allows operation in the recirculating mode. The MODE CONTROL input can also be used to select between two separate data sources. Register packages can be cascaded and the clock lines driven directly for high-speed operation. Alternatively, a delayed clock output (CL_D) is provided that enables cascading register packages while allowing reduced clock drive fan-out and transition-time requirements. A third cascading option makes use of the Q' output from the 1/2 stage, which is available on the next negative-going transition of the clock after the Q output occurs. This delayed output, like the delayed clock CL_D, is used with clocks having slow rise and fall times.

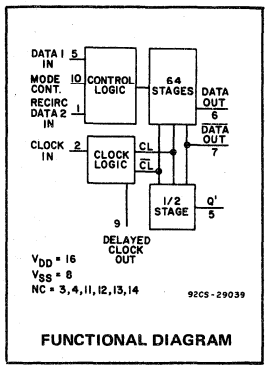
The CD4031B types are supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead plastic dual-in-line packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Fully static operation: DC to 16 MHz typ. @ $V_{DD} - V_{SS}$ = 15 V**
- **Standard TTL drive capability on Q output**
- **Recirculation capability**
- **Three cascading modes:**
  - **Direct clocking for high-speed operation**
  - **Delayed clocking for reduced clock drive requirements**
  - **Additional 1/2 stage for slow clocks**
- **100% tested for quiescent current at 20 V**
- **Standardized, symmetrical output characteristics**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

- **Serial shift registers**
- **Time delay circuits**



FUNCTIONAL DIAGRAM

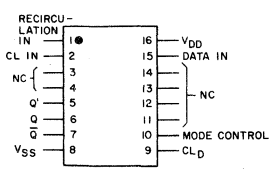
RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)	3	18	V

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85, Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min. Q	0.4	0,5	5	2.56	2.44	1.68	1.44	2.04	4	–	mA
	0.5	0,10	10	6.4	6	4.4	3.6	5.2	10.4	–	
	1.5	0,15	15	16.8	16	11.2	9.6	13.6	27.2	–	
$\overline{Q}$, Q'	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
CL_D	0.4	0,5	5	–	–	–	–	–	1	–	
	0.5	0,10	10	–	–	–	–	–	2.6	–	
	1.5	0,15	15	–	–	–	–	–	6.8	–	
Output High (Source) Current, I_{OH} Min. Q, $\overline{Q}$, Q', CL_D	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5, 13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5, 13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA



TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

DYNAMIC ELECTRICAL CHARACTERISTIC *at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ*

CHARACTERISTIC	TEST CONDITIONS V_{DD}(V)	TYPICAL VALUES	UNITS
Propagation Delay Time: t_{PHL}, t_{PLH} Positive Clock to Q, $\overline{Q}$; Negative Clock to Q'	5	200	ns
	10	100	
	15	80	
Positive Clock to CL_D	5	100	ns
	10	50	
	15	35	
Transition Time, t_{THL}, t_{TLH} (Any Output)	5	100	ns
	10	50	
	15	40	
Minimum Data Setup Time, t_S	5	50	ns
	10	25	
	15	20	
Minimum Data Hold Time, t_H	5	0	ns
	10	0	
	15	0	
Minimum Clock Pulse Width, t_W	5	100	ns
	10	45	
	15	30	
Maximum Clock Input Frequency, f_{CL}**	5	5	MHz
	10	12	
	15	16	
Maximum Clock Input Rise or Fall Time, t_{rCL}, t_{fCL}*	5	15	μs
	10	15	
	15	15	
Input Capacitance, C_{IN} (Any Input)	—	5	pF

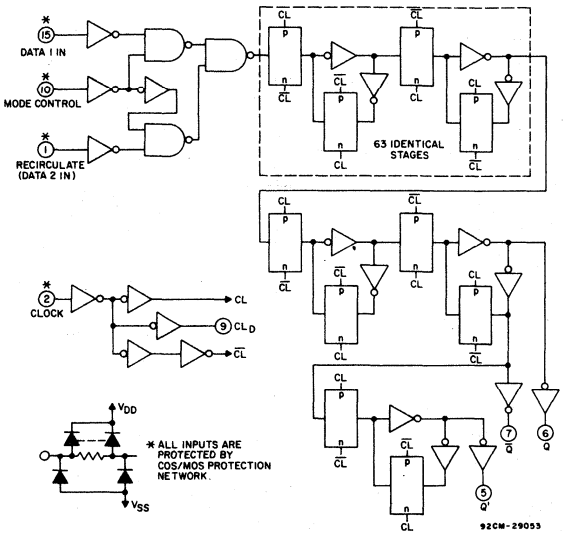
** If more than one unit is cascaded in the parallel clocked application, t_rCL should be made less than or equal to the sum of the propagation delay at 50 pF and the transition time of the output driving stage.

*** Maximum Clock Frequency for Cascaded Units;

a) Using Delayed Clock Feature —

$$f_{max} = \frac{1}{(n\text{-}1)\ CL_D \text{ prop. delay} + Q \text{ prop. delay} + \text{set-up time}}$$ where n = number of packages

b) Not Using Delayed Clock — $$f_{max} = \frac{1}{\text{propagation delay} + \text{set-up time}}$$



INPUT CONTROL CIRCUIT TRUTH TABLE

DATA	RECIRC.	MODE	BIT INTO STAGE I
1	X	0	1
0	X	0	0
X	1	1	1
X	0	1	0

TYPICAL STAGE TRUTH TABLE

Data	CL▲	Data + 1
0	⌐	0
1	⌐	1
X	⌐	NC

TRUTH TABLE FOR OUTPUT FROM Q' (TERMINAL 5)

Data + 63	CL▲	Data + 64.5
0	⌐	0
1	⌐	1
X	⌐	NC

1 = HIGH LEVEL 0 = LOW LEVEL NC = NO CHANGE
X = DON'T CARE ▲ = LEVEL CHANGE

Fig. 1 – Logic diagram and truth tables for CD4031B.

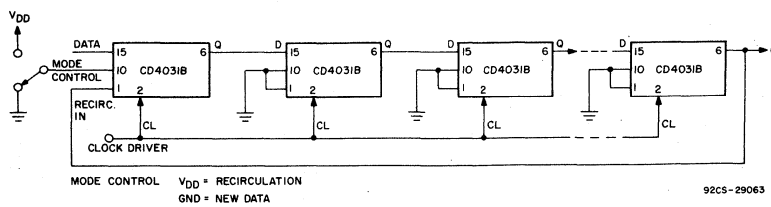


Fig. 2 – Cascading using direct clocking for high speed operation (see clock rise & fall time requirement).

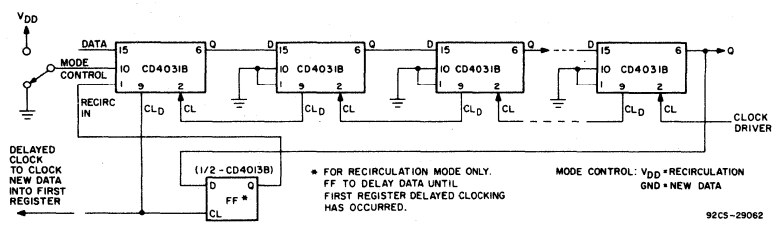


Fig. 3 – Cascading using delayed clocking for reduced clock drive requirements.

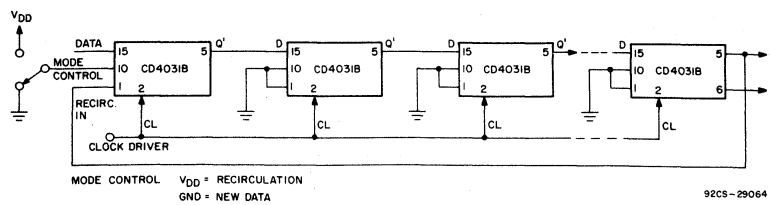


Fig. 4 – Cascading using half-clock-pulse delayed data output (Q') to permit use of slow rise and fall time clock inputs.

COS/MOS Triple Serial Adders

Preliminary Data

High-Voltage Types (20-Volt Rating)
Positive Logic Adder – CD4032B
Negative Logic Adder – CD4038B

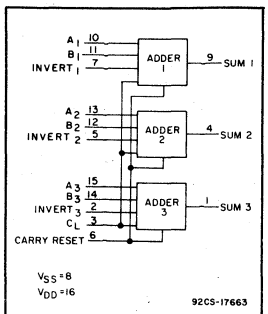
The RCA-CD4032B and CD4038B types consist of three serial adder circuits with common CLOCK and CARRY-RESET inputs. Each adder has two provisions for two serial DATA INPUT signals and an INVERT command signal. When the command signal is a logical "1", the sum is complemented. Data words enter the adder with the least significant bit first; the sign bit trails. The output is the MOD 2 sum of the input bits plus the carry from the previous bit position. The carry is only added at the positive-going clock transition for the CD4032B or at the negative-going clock for the CD4038B, thus, for spike-free operation the input data transitions should occur as soon as possible after the triggering edge.

The CARRY is reset to a logical "0" at the end of each word by applying a logical "1" signal to a CARRY-RESET input one-bit-position before the application of the first bit of the next word.

The CD4032B and CD4038B types are supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Invert inputs on all adders for sum complementing applications**
- **Fully static operation. . . . . dc to 10 MHz (typ.) @ V_{DD} = 10 V**
- **Buffered inputs and outputs**
- **Single-phase clocking**
- **Standardized, symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of "B" Series CMOS Devices"**

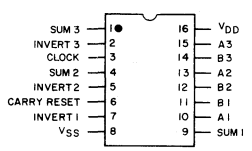


FUNCTIONAL DIAGRAM

Applications

- **Serial arithmetic units**
- **Digital correlators**
- **Digital datalink computers**
- **Flight control computers**
- **Digital servo control systems**

CD4032B, CD4038B
TERMINAL DIAGRAM
Top View



RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D,K,F,H Packages Values at –40, +25, +85 Apply to E Package							UNITS
									+25		
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	–40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

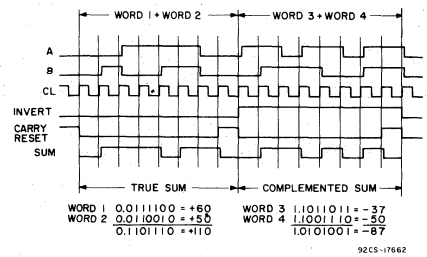


Fig.1 — CD4032B timing diagram.

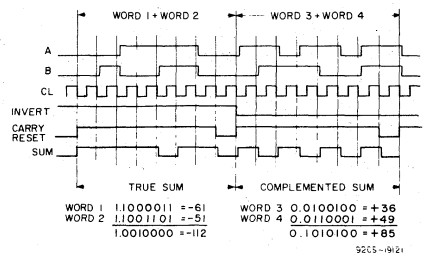


Fig.2 — CD4038B timing diagram.

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ*

CHARACTERISTIC	TEST CONDITIONS V_{DD}(V)	TYPICAL VALUES	UNITS
Propagation Delay Time: t_{PHL}, t_{PLH} A, B, or Invert Inputs to Sum Outputs	5 10 15	280 120 90	ns
Clock Input to Sum Outputs	5 10 15	500 180 135	ns
Transition Time: t_{THL}, t_{TLH}	5 10 15	100 50 40	ns
Data Input Hold Time, t_H Clock Edge to A, B, or Reset Inputs	5 10 15	0 0 0	ns
Maximum Clock Input Frequency, f_{CL}	5 10 15	4 10 12	MHz
Maximum Clock Input Rise or Fall Time, t_{rCL}, t_{fCL}*	5 10 15	15 15 15	μs
Input Capacitance, C_{IN}	(Any Input)	5	pF

* If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

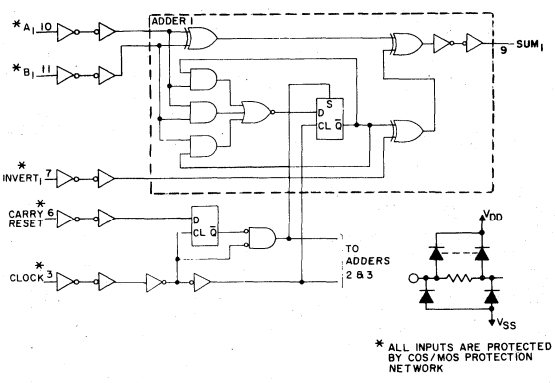


Fig.3 — CD4032B logic diagram of one of three serial adders.

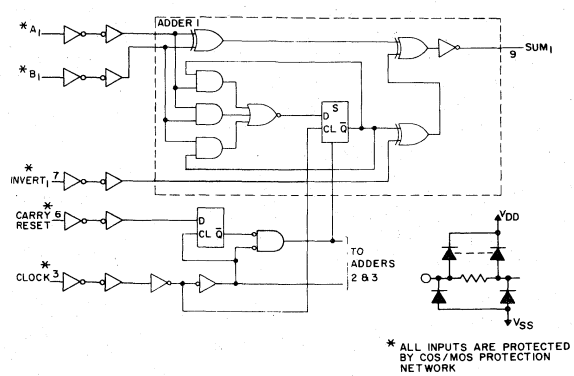


Fig.4 — CD4038B logic diagram of one of three serial adders.

CD4034B Types

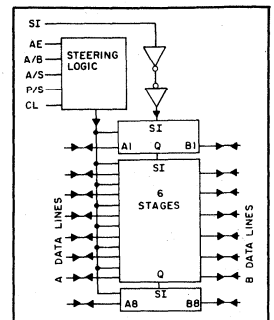
COS/MOS 8-Stage Static Bidirectional Parallel/Serial Input/Output Bus Register

High-Voltage Types (20-Volt Rating)

Preliminary Data

Features:

- Bidirectional parallel data input
- Parallel or serial inputs/parallel outputs
- Asynchronous or synchronous parallel data loading
- Parallel data-input enable on "A" data lines (3-state output)
- Data recirculation for register expansion
- Multipackage register expansion
- Fully static operation dc-to-5 MHz (typ.) at V_{DD} = 10 V
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"



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Functional Diagram

The RCA-CD4034B is a static eight-stage parallel-or serial-input parallel-output register. It can be used to:

1) bidirectionally transfer parallel information between two buses, 2) convert serial data to parallel form and direct the parallel data to either of two buses, 3) store (recirculate) parallel data, or 4) accept parallel data from either of two buses and convert that data to serial form. Inputs that control the operations include a single-phase CLOCK (CL), A DATA ENABLE (AE), ASYNCHRONOUS/SYNCHRONOUS (A/S), A-BUS-TO-B-BUS/B-BUS-TO-A-BUS (A/B), and PARALLEL/SERIAL (P/S).

Data inputs include 16 bidirectional parallel data lines of which the eight A data lines are inputs (3-state outputs) and the B data lines are outputs (inputs) depending on the signal level on the A/B input. In addition, an input for SERIAL DATA is also provided.

All register stages are D-type master-slave flip-flops with separate master and slave clock inputs generated internally to allow synchronous or asynchronous data transfer from master to slave. Isolation from external noise and the effects of loading is provided by output buffering.

PARALLEL OPERATION

A high P/S input signal allows data transfer into the register via the parallel data lines synchronously with the positive transition of the clock provided the A/S input is low. If the A/S input is high the transfer is independent of the clock. The direction of data flow is controlled by the A/B input. When this signal is high the A data lines are inputs (and B data lines are outputs); a low A/B signal reverses the direction of data flow.

The AE input is an additional feature which allows many registers to feed data to a common bus. The A DATA lines are enabled only when this signal is high.

Data storage through recirculation of data in each register stage is accomplished by making the A/B signal high and the AE signal low.

SERIAL OPERATION

A low P/S signal allows serial data to transfer into the register synchronously with the positive transition of the clock. The A/S input is internally disabled when the register is in the serial mode (asynchronous serial operation is not allowed).

The serial data appears as output data on either the B lines (when A/B is high) or the A lines (when A/B is low and the AE signal is high).

Register expansion can be accomplished by simply cascading CD4034B packages.

The CD4034B types are supplied in 24-lead dual-in-line ceramic packages (D and F suffixes), 24-lead dual-in-line plastic packages (E suffix), 24-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Applications:

- Parallel Input/Parallel Output, Parallel Input/Serial Output, Serial Input/Parallel Output, Serial Input/Serial Output Register
- Shift right/shift left register
- Shift right/shift left with parallel loading
- Address register
- Buffer register
- Bus system register with enable parallel lines at bus side
- Double bus register system
- Up-Down Johnson or ring counter
- Pseudo-random code generators
- Sample and hold register (storage, counting, display)
- Frequency and phase comparator

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

RECOMMENDED OPERATING CONDITIONS

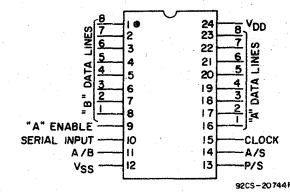
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1, 9	–	10	7				7	–	–	
	1.5, 3.5	–	15	11				11	–	–	
Input Current* I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA
Output Leakage Current#		0,18	18	±0.4	±0.4	±12	±12	–	$\pm 10^{-4}$	±0.4	μA

* All inputs except A and B Lines.
\# A or B Lines when they are Inputs.



Top View
TERMINAL DIAGRAM

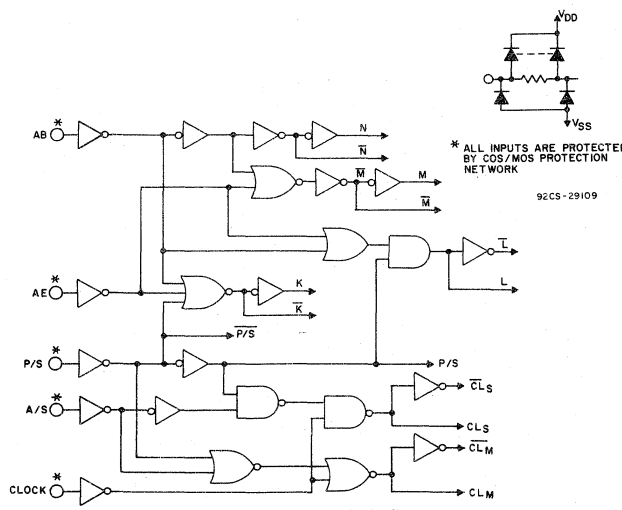


Fig. 1 – Steering logic diagram.

FLIP-FLOP TRUTH TABLE

INPUTS			OUTPUT
$\overline{CL}_M$▲	$\overline{CL}_S$▲	D	Q
↓	↓	0	0
↑	↓	0	0
↓	↑	0	#
↑	↑	X	0
↓	↓	1	1
↑	↓	1	1
↓	↑	1	#

▲= LEVEL CHANGE

#= INVALID CONDITION

DYNAMIC ELECTRICAL CHARACTERISTICS *at $T_A = 25^oC$; Input t_r, $t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200$ kΩ*

CHARACTERISTIC		V_{DD} (V)	TYPICAL VALUES	UNITS
Propagation Delay Time,	t_{PHL}, t_{PLH}	5 10 15	750 300 140	ns
Transition Time,	t_{THL}, t_{TLH}	5 10 15	100 50 40	ns
Minimum Data Setup Time,	t_S	5 10 15	250 100 70	ns
Minimum High-Level Pulse Width, AE, P/S, A/S	t_W	5 10 15	240 85 40	ns
Maximum Clock Frequency,	f_{CL}	5 10 15	2.5 5 6	MHz
Minimum Clock Pulse Width,	t_W	5 10 15	200 100 80	ns
Maximum Clock Rise or Fall Time,	t_{rCL}, t_{fCL}*	5 10 15	15 15 15	μs
Input Capacitance, (Any Input)	C_{IN}	–	5	pF

* If more than one unit is cascaded, t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

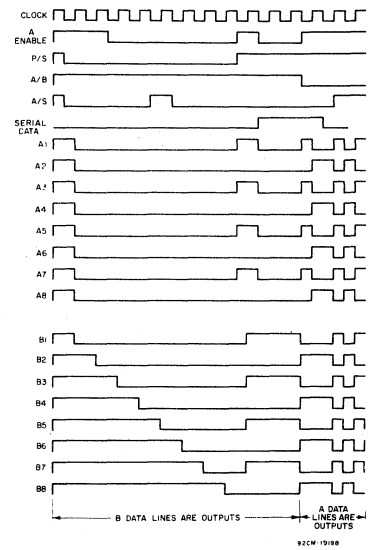


Fig.2 – Timing diagram.

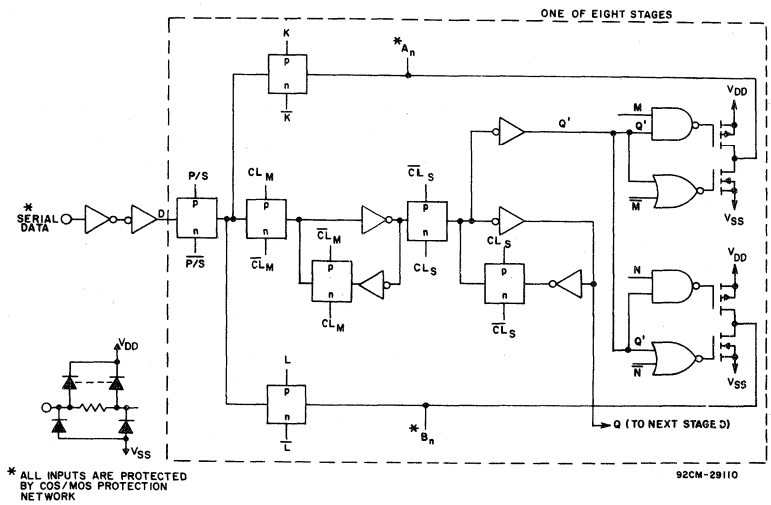


Fig.3 – Register stage logic diagram (1 of 8 stages).

TRUTH TABLE FOR REGISTER INPUT-LEVELS AND RESULTING REGISTER OPERATION

"A" Enable	P/S	A/B	A/S	Operation*
0	0	0	X	Serial Mode; Synch. Serial Data Input, "A" Parallel Data Outputs Disabled
0	0	1	X	Serial Mode; Synch. Serial Data Input, "B" Parallel Data Output
0	1	0	0	Parallel Mode; "B" Synch. Parallel Data Inputs, "A" Parallel Data Outputs Disabled
0	1	0	1	Parallel Mode; "B" Asynch. Parallel Data Inputs, "A" Parallel Data Outputs Disabled
0	1	1	0	Parallel Mode; "A" Parallel Data Inputs Disabled, "B" Parallel Data Outputs, Synch. Data Recirculation
0	1	1	1	Parallel Mode; "A" Parallel Data Inputs Disabled, "B" Parallel Data Outputs, Asynch. Data Recirculation
1	0	0	X	Serial Mode; Synch. Serial Data Input, "A" Parallel Data Output
1	0	1	X	Serial Mode; Synch. Serial Data Input, "B" Parallel Data Output
1	1	0	0	Parallel Mode; "B" Synch. Parallel Data Input, "A" Parallel Data Output
1	1	0	1	Parallel Mode; "B" Asynch. Parallel Data Input, "A" Parallel Data Output
1	1	1	0	Parallel Mode; "A" Synch. Parallel Data Input, "B" Parallel Data Output
1	1	1	1	Parallel Mode; "A" Asynch. Parallel Data Input, "B" Parallel Data Output

*Outputs change at positive transition of clock in the serial mode and when the A/S control input is "low" in the parallel mode.

1 = HIGH LEVEL 0 = LOW LEVEL X = DON'T CARE

CD4035B Types

COS/MOS 4-Stage Parallel In/Parallel Out Shift Register

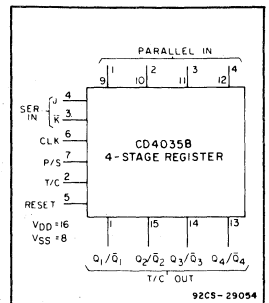
with J-$\overline{K}$ Serial Inputs and True/Complement Outputs

High-Voltage Types (20-Volt Rating)

Preliminary Data

Features:

- 4-Stage clocked shift operation
- Synchronous parallel entry on all 4 stages
- J$\overline{K}$ inputs on first stage
- Asynchronous True/Complement control on all outputs
- Static flip-flop operation; Master-slave configuration
- Buffered inputs and outputs
- High speed — 12 MHz (typ.) at V_{DD} = 10 V
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of "B" Series CMOS Devices"



FUNCTIONAL DIAGRAM

The RCA-CD4035B is a four-stage clocked signal serial register with provision for synchronous PARALLEL inputs to each stage and SERIAL inputs to the first stage via J$\overline{K}$ logic. Register stages 2, 3, and 4 are coupled in a serial D flip-flop configuration when the register is in the serial mode (PARALLEL/SERIAL control low).

Parallel entry into each register stage is permitted when the PARALLEL/SERIAL control is high.

In the parallel or serial mode information is transferred on positive clock transitions.

When the TRUE/COMPLEMENT control is high, the true contents of the register are available at the output terminals. When the TRUE/COMPLEMENT control is low, the outputs are the complements of the data in the register. The TRUE/COMPLEMENT control functions asynchronously with respect to the CLOCK signal.

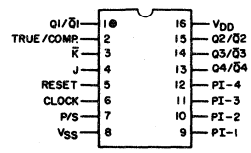
J$\overline{K}$ input logic is provided on the first stage SERIAL input to minimize logic requirements particularly in counting and sequence-generation applications. With J$\overline{K}$ inputs connected together, the first stage becomes a D flip-flop. An asynchronous common RESET is also provided.

The CD4035B-Series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Applications:

- Counters, Registers
  Arithmetic-unit registers
  Shift-left — shift right registers
  Serial-to-parallel/parallel-to-serial conversions
- Sequence generation
- Control circuits
- Code conversion

TERMINAL DIAGRAM
Top View



RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

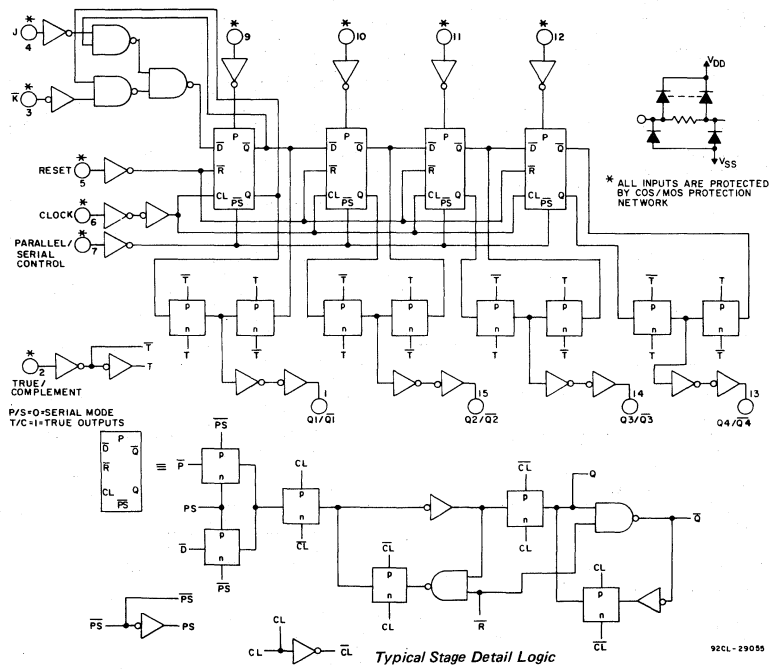
CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
									+25		
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C



Typical Stage Detail Logic

FIRST STAGE TRUTH TABLE

CL	t_{n-1} (INPUTS)				t_n (OUTPUTS)
	J	$\overline{K}$	R	Q_{n-1}	Q_n
↑	0	X	0	0	0
↑	1	X	0	0	1
↑	X	0	0	1	0
↑	1	0	0	Q_{n-1}	$\overline{Q_{n-1}}$ TOGGLE MODE
↑	X	1	0	1	1
↓	X	X	0	Q_{n-1}	Q_{n-1}
X	X	X	1	X	0

Fig. 1 – Logic diagram.

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25^oC$, Input t_r, $t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200\,k\Omega$

CHARACTERISTICS	TEST CONDITIONS V_{DD} (V)	TYPICAL VALUES	UNITS
CLOCKED OPERATION			
Propagation Delay Time: t_{PLH}, t_{PHL}	5	200	ns
	10	100	
	15	80	
Transition Time: t_{THL}, t_{TLH}	5	100	ns
	10	50	
	15	40	
Minimum Clock Pulse Width, t_W	5	100	ns
	10	45	
	15	30	
Maximum Clock Rise & Fall Time t_{rCL}, t_{fCL}*	5,10, 15	15	μs
Minimum Setup Time: J/$\overline{K}$ Lines	5	50	ns
	10	25	
	15	20	
Parallel-In-Lines	5	25	ns
	10	15	
	15	10	
Maximum Clock Frequency, f_{CL}	5	5	MHz
	10	12	
	15	16	
Input Capacitance, C_{IN}	Any Input	5	pF
RESET OPERATION			
Propagation Delay Time: t_{PHL}, t_{PLH}	5	200	ns
	10	100	
	15	80	
Minimum Reset Pulse Width, t_W	5	100	ns
	10	45	
	15	30	

* If more than one unit is cascaded $t_{r}CL$ should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

COS/MOS Quad True/Complement Buffer

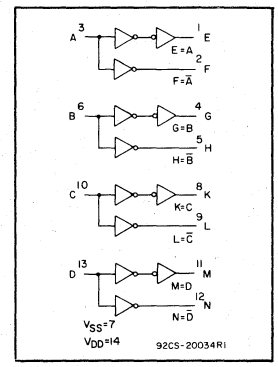
High Voltage Types (20-Volt Rating)

The RCA-CD4041UB types are quad true/complement buffers consisting of n- and p-channel units having low channel resistance and high current (sourcing and sinking) capability. The CD4041UB is intended for use as a buffer, line driver, or COS/MOS-to-TTL driver. It can be used as an ultra-low power resistor-network driver for A/D and D/A conversion, as a transmission-line driver, and in other applications where high noise immunity and low-power dissipation are primary design requirements.

The CD4041UB types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

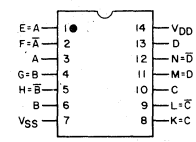
Features:

- Balanced sink and source current; approximately 4 times standard "B" drive
- Equalized delay to true and complement outputs
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"



Applications:

- High current source/sink driver
- COS/MOS-to-DTL/TTL Converter Buffer
- Display driver
- MOS clock driver
- Resistor network driver (Ladder or weighted R)
- Buffer
- Transmission line driver



92CS-20755R1

TOP VIEW
TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)	3	18	V

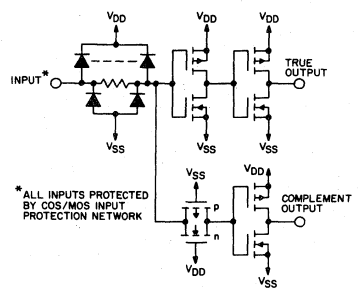


Fig.1 – Schematic diagram 1 of 4 buffers.

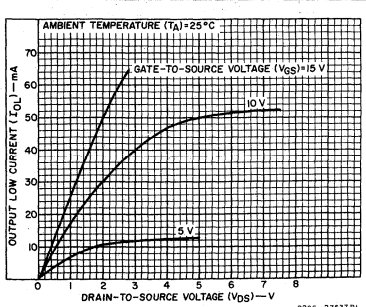


Fig.2 – Typical output low (sink) current characteristics.

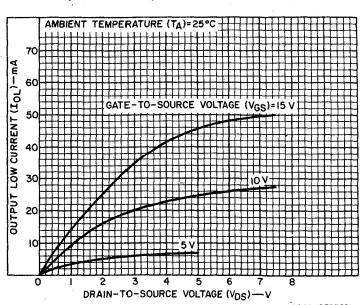


Fig.3 – Minimum low (sink) current characteristics.

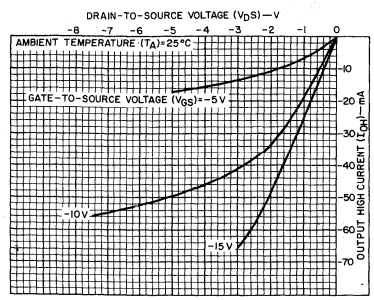


Fig.4 – Typical output high (source) current characteristics.

CD4041UB Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55,+25,+125 Apply to D,K,F,H Pkgs. Values at −40,+25,+85 Apply to E Pkgs.							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

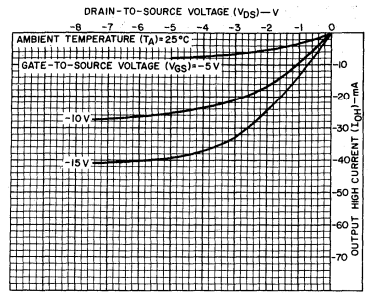


Fig.5 – Minimum output high (source) current characteristics.

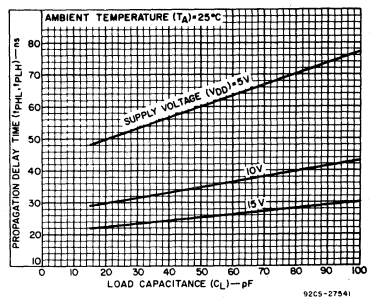


Fig.6 – Typical propagation delay time vs. load capacitance.

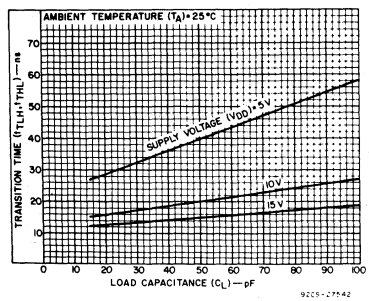


Fig.7 – Typical transition time vs. load capacitance.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r,t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC		CONDITIONS	ALL TYPES LIMITS		UNITS
		V_{DD} Volts	Typ.	Max.	
Propagation Delay Time:	t_{PHL}, t_{PLH}	5	60	120	ns
		10	35	70	
		15	25	50	
Transition Time	t_{THL}, t_{TLH}	5	40	80	ns
		10	20	40	
		15	15	30	
Input Capacitance	C_{IN}	Any Input	15	22.5	pF

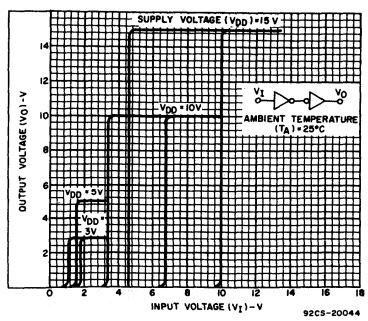


Fig.8 – Minimum and maximum transfer characteristics – true output.

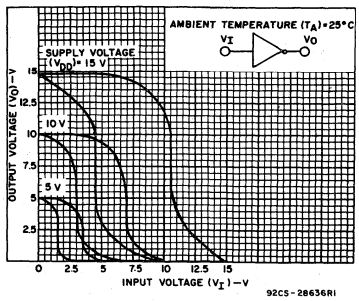


Fig.9 – Minimum and maximum transfer characteristics – complement output.

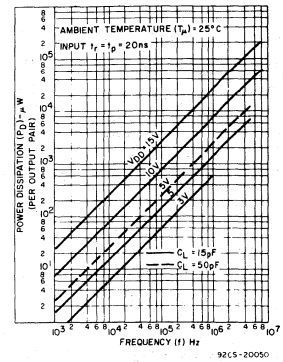


Fig.11 – Typical power dissipation vs frequency per output pair.

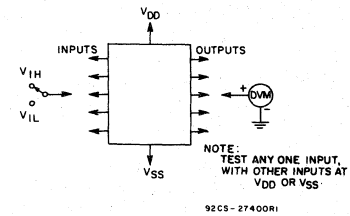


Fig.13 – Input voltage test circuit.

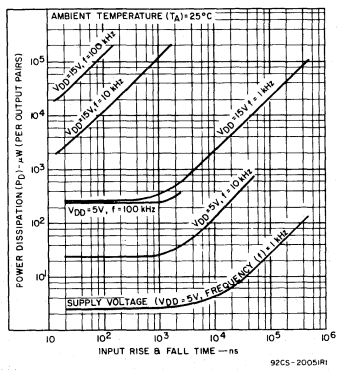


Fig.10 – Typical power dissipation vs. input rise & fall time per output pair.

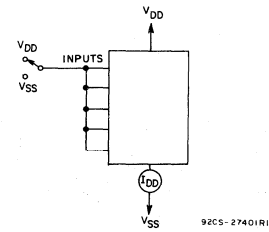


Fig.12 – Quiescent device current test circuit.

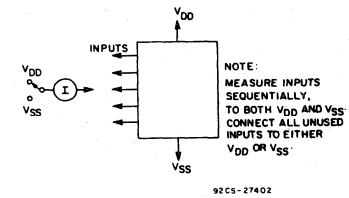
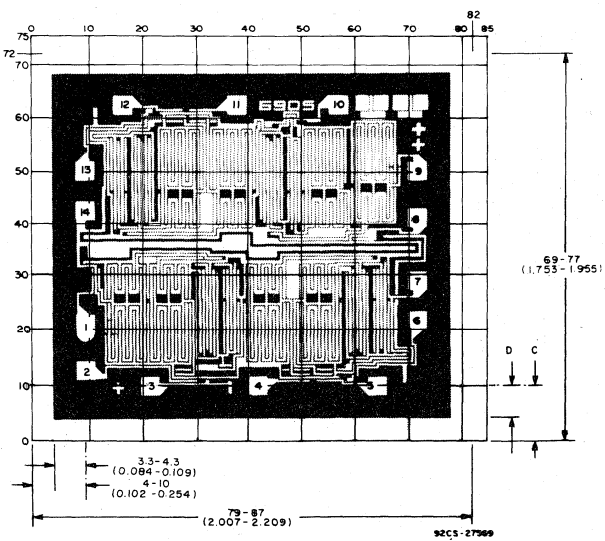


Fig.14 – Input-leakage-current test circuit.

Dimensions and pad layout for the CD4041BH



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS
Quad Clocked "D" Latch
High-Voltage Types (20-Volt Rating)

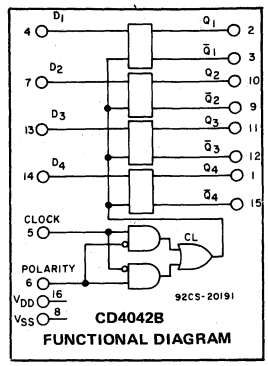
The RCA-CD4042B types contain four latch circuits, each strobed by a common clock. Complementary buffered outputs are available from each circuit. The impedance of the n- and p-channel output devices is balanced and all outputs are electrically identical.

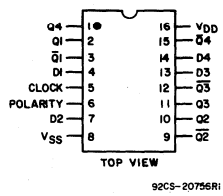
Information present at the data input is transferred to outputs Q and $\overline{Q}$ during the CLOCK level which is programmed by the POLARITY input. For POLARITY = 0 the transfer occurs during the 0 CLOCK level and for POLARITY = 1 the transfer occurs during the 1 CLOCK level. The outputs follow the data input providing the CLOCK and POLARITY levels defined above are present. When a CLOCK transition occurs (positive for POLARITY = 0 and negative for POLARITY = 1) the information present at the input during the CLOCK transition is retained at the outputs until an opposite CLOCK transition occurs.

The CD4042B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

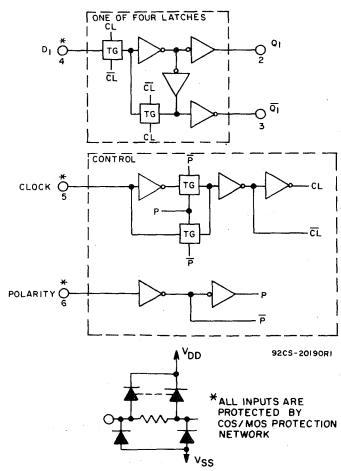
Features:
- Clock polarity control
- Q and $\overline{Q}$ outputs
- Common clock
- Low power TTL compatible
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings
- Noise margin (over full package temperature range):
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:
- Buffer storage
- Holding register
- General digital logic





TERMINAL ASSIGNMENT



CLOCK	POLARITY	Q
0	0	D
⌐	0	LATCH
1	1	D
¬	1	LATCH

Fig. 1 – Logic block diagram and truth table.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55,+25,+125 Apply to D,K,F,H Pkgs. Values at −40,+25,+85 Apply to E Pkgs.							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS ALL TYPES		UNITS
		Min.	Max.	
Supply-Voltage Range (For T_A=Full Package Temperature Range)	–	3	18	V
Clock Pulse Width, t_W	5	200	–	ns
	10	100	–	
	15	60	–	
Setup Time, t_S	5	50	–	ns
	10	30	–	
	15	25	–	
Hold Time, t_H	5	120	–	ns
	10	60	–	
	15	50	–	
Clock Rise or Fall Time: t_r , t_f	5,10 15	Not rise or fall time sensitive.		μS

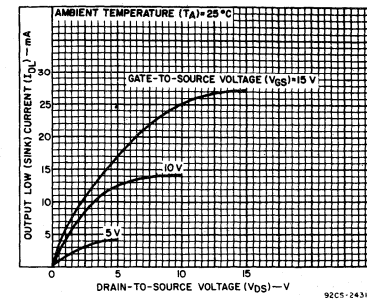


Fig. 2 – Typical output low (sink) current characteristics.

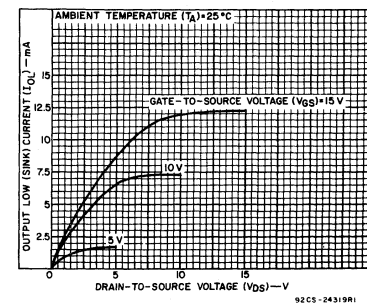


Fig. 3 – Minimum output low (sink) current characteristics.

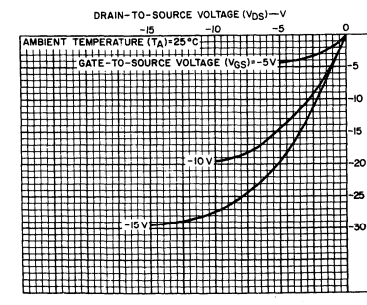


Fig. 4 – Typical output high (source) current characteristics.

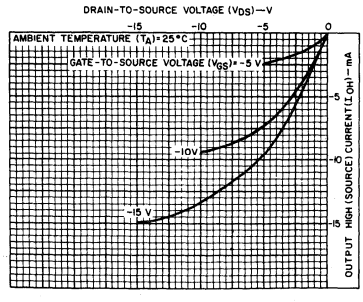


Fig. 5 – Minimum output high (source) current characteristics.

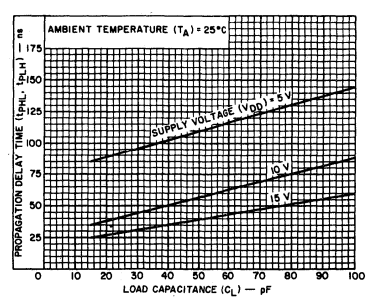


Fig. 6 – Typical propagation delay time vs. load capacitance–data to Q.

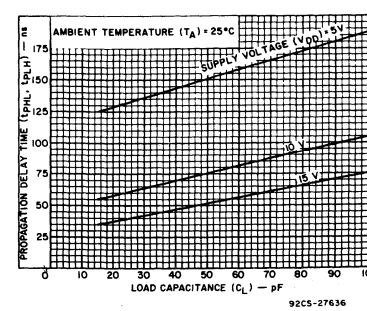


Fig. 7 – Typical propagation delay time vs. load capacitance–data to $\overline{Q}$.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS ALL TYPES Typ.	Max.	UNITS
Propagation Delay Time: t_{PHL}, t_{PLH} Data In to Q	5	110	220	ns
	10	55	110	
	15	40	80	
Data In to $\overline{Q}$	5	150	300	ns
	10	75	150	
	15	50	100	
Clock to Q	5	225	450	ns
	10	100	200	
	15	80	160	
Clock to $\overline{Q}$	5	250	500	ns
	10	115	230	
	15	90	180	
Transition Time : t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Minimum Clock Pulse Width, t_W	5	100	200	ns
	10	50	100	
	15	30	60	
Minimum Hold Time, t_H	5	60	120	ns
	10	30	60	
	15	25	50	
Minimum Setup Time, t_S	5	0	50	ns
	10	0	30	
	15	0	25	
Clock Input Rise or Fall Time: t_r, t_f	5,10 15	Not rise or fall time sensitive.		μS
Input Capacitance, C_{IN} (Any Input)	–	5	7.5	pF

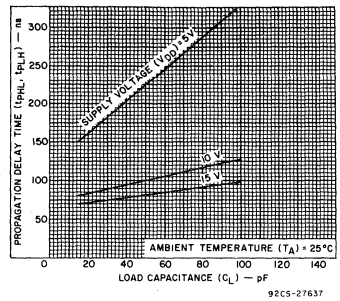


Fig. 8 – Typical propagation delay time vs. load capacitance–clock to Q

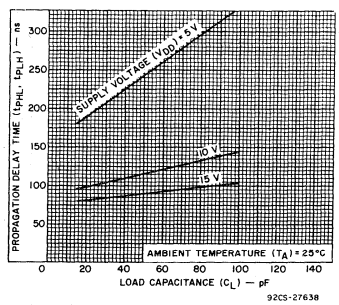


Fig. 9 – Typical propagation delay time vs. load capacitance–clock to $\overline{Q}$.

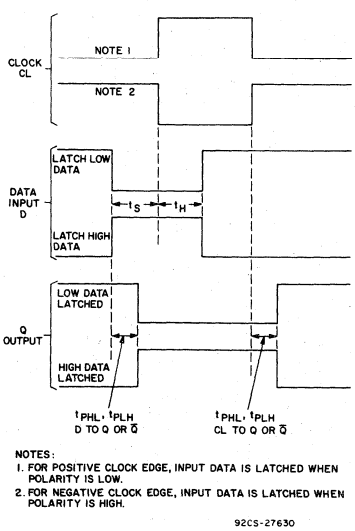


Fig. 11 – Dynamic test parameters.

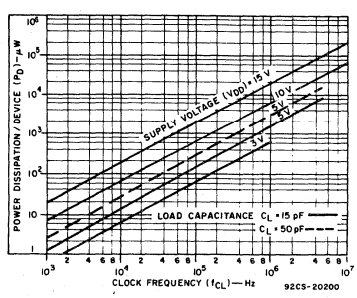


Fig. 12 – Typical power dissipation vs. frequency.

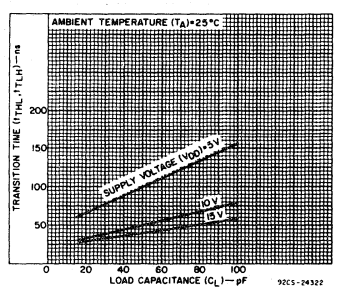


Fig. 10 – Typical transition time vs. load capacitance.

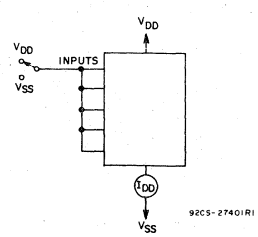


Fig. 13 – Quiescent device current test circuit.

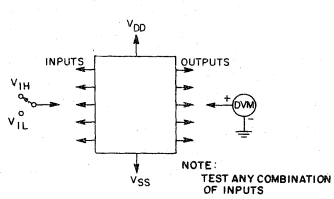


Fig. 14 – Input voltage test circuit.

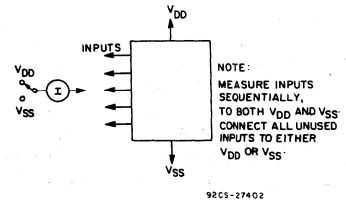
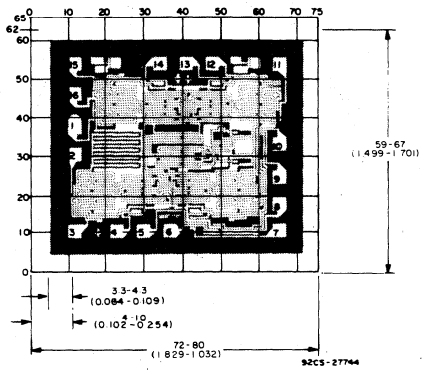


Fig. 15 — Input current test circuit.

Chip Photograph, Dimensions, and Pad Layout



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS Quad 3-State R/S Latches

High-Voltage Types (20-Volt Rating)
Quad NOR R/S Latch – CD4043B
Quad NAND R/S Latch – CD4044B

The RCA-CD4043B types are quad cross-coupled 3-state COS/MOS NOR latches and the CD4044B types are quad cross-coupled 3-state COS/MOS NAND latches. Each latch has a separate Q output and individual SET and RESET inputs. The Q outputs are controlled by a common ENABLE input. A logic "1" or high on the ENABLE input connects the latch states to the Q outputs. A logic "0" or low on the ENABLE input disconnects the latch states from the Q outputs, resulting in an open circuit condition on the Q outputs. The open circuit feature allows common busing of the outputs.

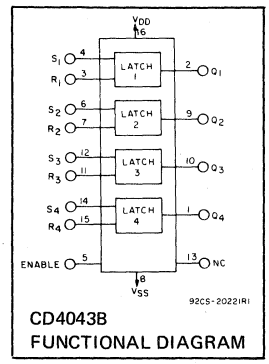
The CD4043B and CD4044B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

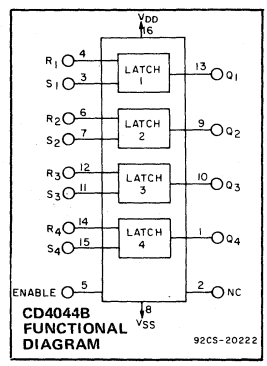
- 3-state outputs with common output ENABLE
- Separate SET and RESET inputs for each latch
- NOR and NAND configurations
- 5-V, 10-V, and 15-V parametric ratings
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range): 1 V at V_{DD} = 5 V; 2 V at V_{DD} = 10 V; 2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Holding register in multi-register system
- Four bits of independent storage with output ENABLE
- Strobed register
- General digital logic

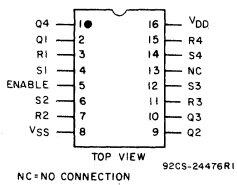


CD4043B
FUNCTIONAL DIAGRAM

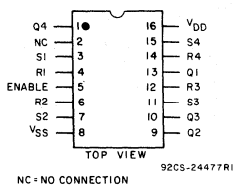


CD4044B FUNCTIONAL DIAGRAM

TERMINAL ASSIGNMENTS



CD4043B



CD4044B

Recommended Operating Conditions T_A=25°C
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V_{DD} (V)	Min.	Max.	Units
Supply-Voltage Range (T_A = Full Package Temperature Range)	–	3	12	V
SET or RESET Pulse Width, t_W	5	160	–	ns
	10	80	–	
	15	40	–	

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . –0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = –40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
PACKAGE TYPE E . . . . . –40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

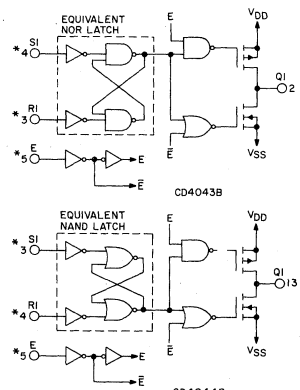


Fig. 1 – Logic diagrams.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1, 9	–	10	7				7	–	–	
	1.5, 3.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA
3-State Output Leakage Current I_{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	–	$±10^{-4}$	±0.4	μA

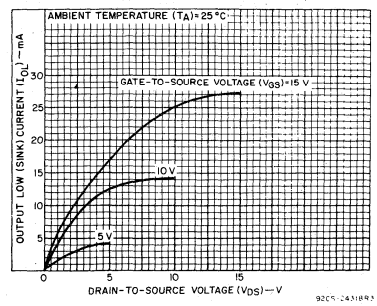


Fig. 2 – Typical output low (sink) current characteristics.

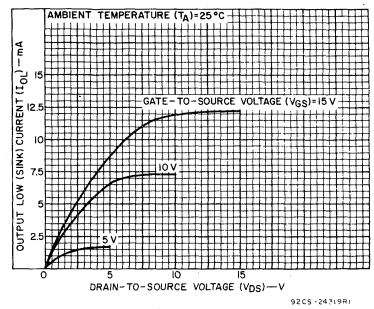


Fig. 3 – Minimum output low (sink) current characteristics.

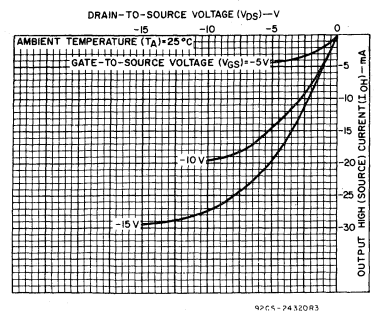


Fig. 4 – Typical output high (source) current characteristics.

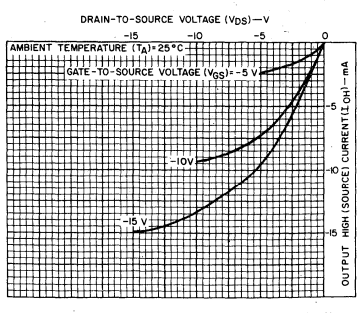


Fig. 5 – Minimum output high (source) current characteristics.

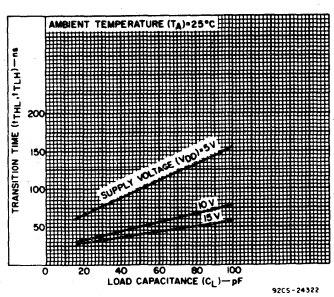


Fig. 6 – Typical transition time vs. load capacitance.

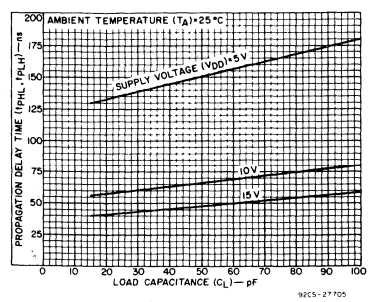


Fig. 7 – Typical propagation delay time vs. load capacitance—SET, RESET to Q, Q̄.

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A = 25° C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ*

CHARACTERISTIC	V_{DD} (V)	LIMITS ALL TYPES TYP.	LIMITS ALL TYPES MAX.	UNITS
Propagation Delay Time: t_{PHL}, t_{PLH} SET or RESET to Q	5	150	300	ns
	10	70	140	
	15	50	100	
3-State Propagation Delay Time: ENABLE to Q t_{PHZ}, t_{PZH}	5	115	230	ns
	10	55	110	
	15	40	80	
t_{PLZ}, t_{PZL}	5	90	180	ns
	10	50	100	
	15	35	70	
Transition Time: t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Minimum SET or RESET Pulse Width, t_W	5	80	160	ns
	10	40	80	
	15	20	40	
Input Capacitance, (Any Input) C_{IN}	–	5	7.5	pF

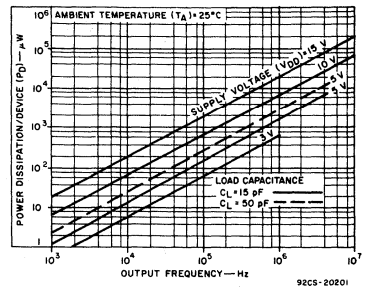


Fig. 8 – Typical power dissipation vs. frequency.

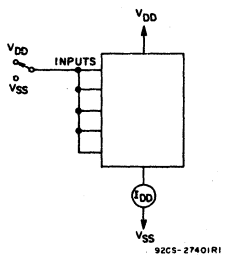


Fig. 9 – Quiescent device current.

TEST CIRCUITS

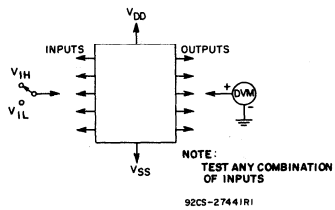


Fig. 10 – Input voltage.

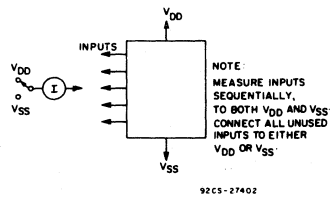


Fig. 11 – Input current.

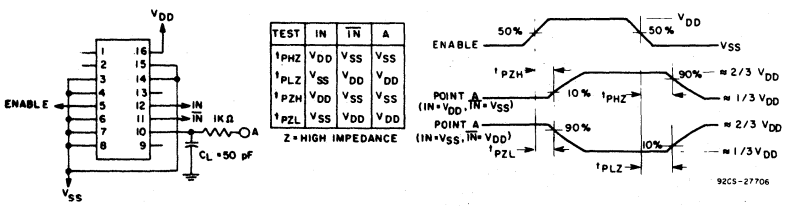


Fig. 12 – ENABLE propagation delay time test circuit and waveforms.

APPLICATIONS

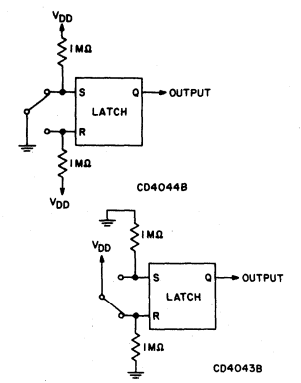


Fig. 13 – Switch bounce eliminator.

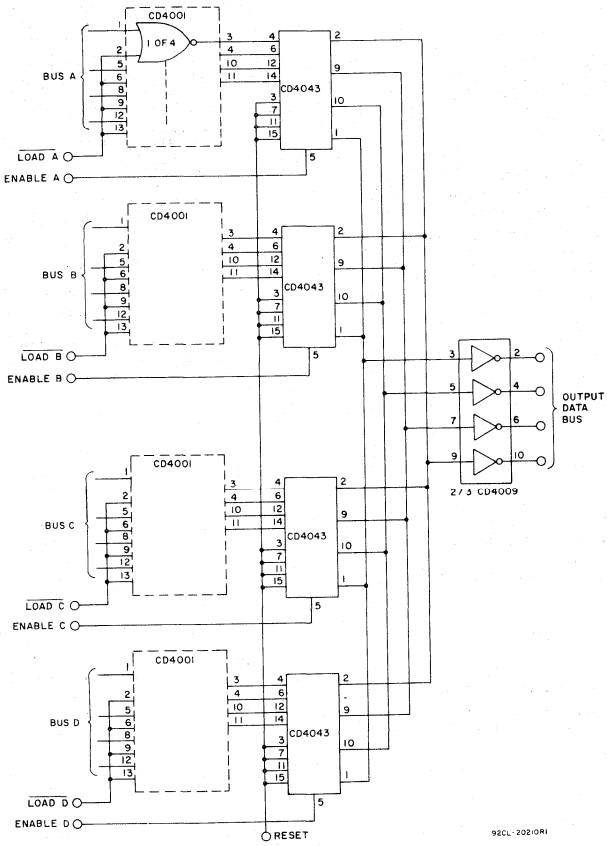
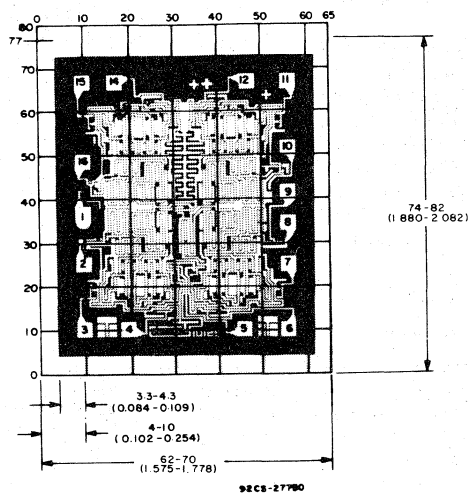
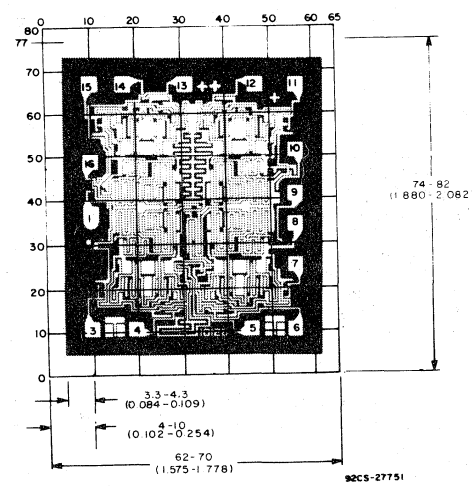


Fig. 14 — Multiple bus storage.

CHIP PHOTOGRAPHS DIMENSIONS AND PAD LAYOUTS



CD4043BH



CD4044BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CD4045B Types

COS/MOS 21-Stage Counter

Preliminary Data

High-Voltage Types (20-Volt Rating)

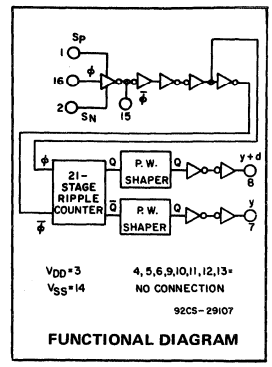
The RCA-CD4045B is a timing circuit consisting of 21 counter stages, two output-shaping flip-flops, two inverter output drivers, and input inverters for use in a crystal oscillator. The CD4045B configuration provides 21 flip-flop counting stages, and two flip-flops for shaping the output waveform for a 3.125% duty cycle. Push-pull operation is provided by the inverter output drivers.

The first inverter is intended for use as a crystal oscillator/amplifier. However, it may be used as a normal logic inverter if desired. A crystal oscillator circuit can be made less sensitive to voltage-supply variations by the use of source resistors. In this device, the sources of the p and n transistors have been brought out to package terminals. If external resistors are not required, the sources must be shorted to their respective substrates (S_p to V_{DD}, S_n to V_{SS}). See Fig. 1.

The CD4045B types are supplied in 16-lead dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Very low operating dissipation . . . . . 1 mW (typ.); @ V_{DD} = 5 V, fϕ = 1 MHz**
- **Output drivers with sink or source capability . . . . . 7 mA (typ.) @ V_{DD} = 5 V**
- **Medium speed (typ.) . . . . . fϕ = 16 MHz @ V_{DD} = 10 V**
- **100% tested for quiescent current at 20 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, Standard Specifications for Descripiton of 'B' Series CMOS Devices"**



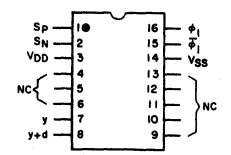
FUNCTIONAL DIAGRAM

Applications:

- **Digital equipment in which ultra-low dissipation and/or operation using a battery source and primary design requirements**
- **Accurate timing from a crystal oscillator for timing applications such as wall clocks, table clocks, automobile clocks, and digital timing references in any circuit requiring accurately timed outputs at various intervals in the counting sequence.**
- **Driving miniature synchronous motors, stepping motors, or external bipolar transistors in push-pull fashion.**

TERMINAL DIAGRAM

Top View



NC=NO CONNECTION

NOTE Observe power-supply terminal connections, V_{DD} is terminal No. 3 and V_{SS} is terminal No. 14 (not 16 and 8 respectively, as in other CD4000B Series 16-lead devices).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85, Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	–	–	–	–	–	7	–	mA
	0.5	0,10	10	–	–	–	–	–	18	–	
	1.5	0,15	15	–	–	–	–	–	47	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–	–	–	–	–	−7	–	
	9.5	0,10	10	–	–	–	–	–	−18	–	
	13.5	0,15	15	–	–	–	–	–	−47	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5, 13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5, 13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	V_{DD} V	TYPICAL VALUES	UNITS
Propagation Delay Time: ϕ to y or y+d out t_{PHL}, t_{PLH}		5 10 15	2.2 1.2 1	μs
Transition Time: t_{THL}, t_{TLH}		5 10 15	100 50 40	ns
Maximum Input-Pulse Frequency, $f_{m\phi}$		5 10 15	7 16 24	MHz
Minimum Input-Pulse Width, t_W		5 10 15	100 50 40	ns
Maximum Input-Pulse Rise or Fall Time; $t_r\phi$, $t_f\phi$		5 10 15	15 10 10	μs
Input Capacitance, C_{IN}	Any Input	–	5	pF

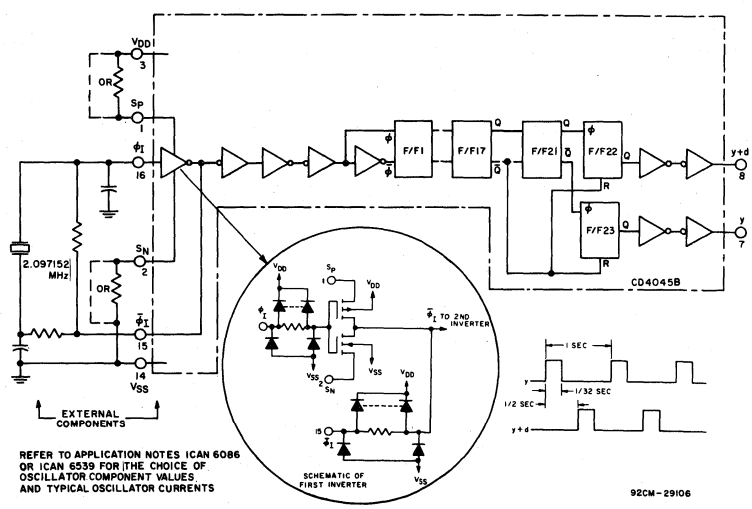


Fig. 1 – CD4045B and outboard components in a typical 21-stage counter application.

Preliminary Data

COS/MOS Micropower Phase-Locked Loop

The RCA-CD4046B COS/MOS Micropower Phase-Locked Loop (PLL) consists of a low-power, linear voltage-controlled oscillator (VCO) and two different phase comparators having a common signal-input amplifier and a common comparator input. A 5.2-V zener diode is provided for supply regulation if necessary.

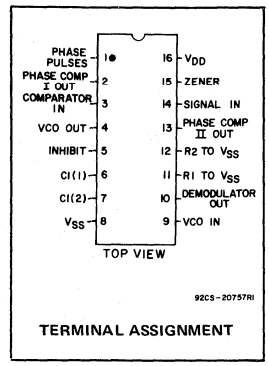
The CD4046B types are supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

VCO Section

The VCO requires one external capacitor C1 and one or two external resistors (R1 or R1 and R2). Resistor R1 and capacitor C1 determine the frequency range of the VCO and resistor R2 enables the VCO to have a frequency offset if required. The high input impedance ($10^{12}\Omega$) of the VCO simplifies the design of low-pass filters by permitting the designer a wide choice of resistor-to-capacitor ratios. In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided at terminal 10 (DEMODULATED OUTPUT). If this terminal is used, a load resistor (R_S) of 10 kΩ or more should be connected from this terminal to V_{SS}. If unused this terminal should be left open. The VCO can be connected either directly or through frequency dividers to the comparator input of the phase comparators. A full COS/MOS logic swing is available at the output of the VCO and allows direct coupling to COS/MOS frequency dividers such as the RCA-CD4024, CD4018, CD4020, CD4022, CD4029, and CD4059. One or more CD4018 (Preset-table Divide-by-N Counter) or CD4029 (Presettable Up/Down Counter), or CD4059A (Programmable Divide-by-"N" Counter), together with the CD4046B (Phase-Locked Loop) can be used to build a micropower low-frequency synthesizer. A logic 0 on the INHIBIT input "enables" the VCO and the source follower, while a logic 1 "turns off" both to minimize stand-by power consumption.

Features:

- **Very low power consumption: 100 μW (typ.) at VCO f_o = 10 kHz, V_{DD} = 5 V**
- **Operating frequency range up to 1.4 MHz (typ.) at V_{DD} = 10 V**
- **Low frequency drift: 0.06%/°C (typ.) at V_{DD} = 10 V**
- **Choice of two phase comparators:**
  1. **Exclusive-OR network**
  2. **Edge-controlled memory network with phase-pulse output for lock indication**
- **High VCO linearity: 1% (typ.)**
- **VCO inhibit control for ON-OFF keying and ultra-low standby power consumption**
- **Source-follower output of VCO control input (Demod. output)**
- **Zener diode to assist supply regulation**
- **Standardized, symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**



TERMINAL ASSIGNMENT

Applications:

- **FM demodulator and modulator**
- **Frequency synthesis and multiplication**
- **Frequency discriminator**
- **Data synchronization**
- **Voltage-to-frequency conversion**
- **Tone decoding**
- **FSK – Modems**
- **Signal conditioning**
- **(See ICAN-6101) "RCA COS/MOS Phase-Locked Loop – A Versatile Building Block for Micropower Digital and Analog Applications"**

Phase Comparators

The phase-comparator signal input (terminal 14) can be direct-coupled provided the signal swing is within COS/MOS logic levels [logic "0" ≤30% (V_{DD}–V_{SS}), logic "1" ≥ 70% (V_{DD}–V_{SS})]. For smaller swings the signal must be capacitively coupled to the self-biasing amplifier at the signal input.

Phase comparator I is an exclusive-OR network; it operates analagously to an overdriven balanced mixer. To maximize the lock range, the signal- and comparator-input frequencies must have a 50% duty cycle. With no signal or noise on the signal input, this phase comparator has an average output voltage equal to $V_{DD}/2$. The low-pass filter connected to the output of phase comparator I supplies the averaged voltage to the VCO input, and causes the VCO to oscillate at the center frequency (f_o).

The frequency range of input signals on which the PLL will lock if it was initially out of lock is defined as the frequency capture range ($2f_c$).

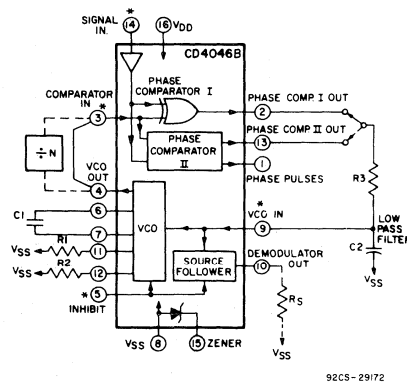
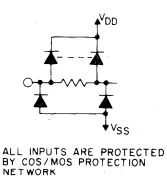


Fig. 1 – COS/MOS phase-locked loop block diagram.



MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . –0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = –40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
PACKAGE TYPE E . . . . . –40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

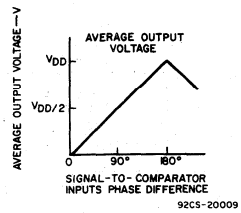


Fig.2 – Phase-comparator I characteristics at low-pass filter output.

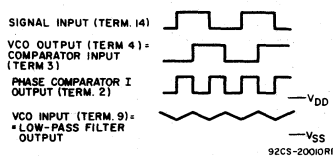


Fig.3 – Typical waveforms for COS/MOS phase-locked loop employing phase comparator I in locked condition of f_o.

The frequency range of input signals on which the loop will stay locked if it was initially in lock is defined as the frequency lock range ($2f_L$). The capture range is ⩽ the lock range.

With phase comparator I the range of frequencies over which the PLL can acquire lock (capture range) is dependent on the low-pass-filter characteristics, and can be made as large as the lock range. Phase-comparator I enables a PLL system to remain in lock in spite of high amounts of noise in the input signal.

One characteristic of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the VCO center-frequency. A second characteristic is that the phase angle between the signal and the comparator input varies between 0° and 180°, and is 90° at the center frequency. Fig. 2 shows the typical, triangular, phase-to-output response characteristic of phase-comparator I. Typical waveforms for a COS/MOS phase-locked-loop employing phase comparator I in locked condition of f_o is shown in Fig. 3.

Phase-comparator II is an edge-controlled digital memory network. It consists of four flip-flop stages, control gating, and a three-state output circuit comprising p- and n-type drivers having a common output node. When the p-MOS or n-MOS drivers are ON they pull the output up to V_{DD} or down to V_{SS}, respectively. This type of phase comparator acts only on the positive edges of the signal and comparator inputs. The duty cycles of the signal and comparator inputs are not important since positive transitions control the PLL system utilizing this type of comparator. If the signal-input frequency is higher than the comparator-input

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

CHARACTERISTIC	TEST CONDITIONS			LIMITS			UNITS
		V_O (V)	V_{DD} (V)	ALL PACKAGE TYPES Min.	Typ.	Max.	
VCO Section							
Operating Power Dissipation, P_D	f_o = 10 kHz, R_1 = 1 MΩ, R_2 = ∞, $VCO_{IN} = \frac{V_{DD}}{2}$		5	–	100	–	μW
			10	–	700	–	
			15	–	3000	–	
Maximum Operating Frequency, f_{max}	R1 = 5 kΩ, R_2 = ∞, $VCO_{IN} = V_{DD}$, C1 = 50 pF		5	–	0.7	–	MHz
			10	–	1.4	–	
			15	–	1.9	–	
Center Frequency (f_0) and Frequency Range, $f_{max}-f_{min}$	Programmable with external components R1, R2, and C1 *See Design Information*						
Linearity	VCO_{IN} = 2.5 V ± 0.3 V, R1 > 10 kΩ		5	–	1	–	%
	= 5 V ± 2.5 V, R1 > 400 kΩ		10	–	1	–	
	= 7.5 V ± 5 V, R1 = 1 MΩ		15	–	1	–	
Temperature-Frequency Stability•: No Frequency Offset $f_{MIN} = 0$	$\%/°C \propto \frac{1}{f \cdot V_{DD}}$, R2 = ∞		5	–	0.12–0.24	–	%/°C
			10	–	0.04–0.08	–	
			15	–	0.015–0.03	–	
Frequency Offset $f_{MIN} \neq 0$	$\%/°C \propto \frac{1}{f \cdot V_{DD}}$		5	–	0.06–0.12	–	
			10	–	0.05–0.1	–	
			15	–	0.03–0.06	–	
Input Resistance of VCO_{IN} (Term 9), R_I			5,10,15	–	10^{12}	–	Ω
VCO Output Voltage (Term 4) Low Level, V_{OL}	Driving COS/MOS-Type Load (e.g. Term 3 Phase Comparator Input)		5,10,15	–	–	0.05	V
High Level, V_{OH}			5	4.95	–	–	
			10	9.95	–	–	
			15	14.95	–	–	
VCO Output Duty Cycle			5,10,15	–	50	–	%
VCO Output Transition Times, t_{THL}, t_{TLH}		V_O Volts	5	–	100	–	ns
			10	–	50	–	
			15	–	40	–	
VCO Output Drive Current: n-Channel (Sink), I_{DN}		0.4	5	0.51	1	–	mA
		0.5	10	1.3	2.6	–	
		1.5	15	3.4	6.8	–	
p-Channel (Source), I_{DP}		4.6	5	–0.51	–1	–	
		9.5	10	–1.3	–2.6	–	
		13.5	15	–3.4	–6.8	–	
Source-Follower Output (Demodulated Output): Offset Voltage ($VCO_{IN}-V_{DEM}$)	R_S > 10 kΩ		5,10	–	1.5	–	V
			15	–	1.5	–	
Linearity	R_S>50kΩ, VCO_{IN} = 2.5±0.3 V		5	–	0.1	–	%
	= 5±2.5 V		10	–	0.6	–	
	= 7.5±5 V		15	–	0.8	–	
Zener Diode Voltage (V_Z)	I_Z = 50 μA			–	5.2	–	V
Zener Dynamic Resistance, R_Z	I_Z = 1 mA			–	50	–	Ω

• Positive coefficient.

frequency, the p-type output driver is maintained ON most of the time, and both the n and p drivers OFF (3 state) the remainder of the time. If the signal-input frequency is lower than the comparator-input frequency, the n-type output driver is maintained ON most of the time, and both the n and p drivers OFF (3 state) the remainder of the time. If the signal- and comparator-input frequencies are the same, but the signal input lags the comparator input in phase, the n-type output driver is maintained ON for a time corresponding to the phase difference. If the signal- and comparator-input frequencies are the same, but the comparator input lags the signal in phase, the p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the capacitor voltage of the low-pass filter connected to this phase comparator is adjusted until the signal and comparator inputs are equal in both phase and frequency. At this stable point both p- and n-type output drivers remain OFF and thus the phase comparator output becomes an open circuit and holds the voltage on the capacitor of the low-pass filter constant. Moreover the signal at the "phase pulses" output is a high level which can be used for indicating a locked condition. Thus, for phase comparator II, no phase difference exists between signal and comparator input over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both the p- and n-type output drivers are OFF for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator II. Fig. 4 shows typical waveforms for a COS/MOS PLL employing phase comparator II in a locked condition.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	TEST CONDITIONS	V_O (V)	V_{DD} (V)	LIMITS ALL PACKAGE TYPES Min.	Typ.	Max.	UNITS
Phase Comparator Section							
Total Quiescent Device Current, I_{DD} Term. 14 Open	Term. 15 open, Term. 5 at V_{DD}, Terms. 3 & 9 at V_{SS}		5	–	25	–	μA
			10	–	200	–	
			15	–	600	–	
Term. 14 at V_{SS} or V_{DD}			5	–	5	–	
			10	–	25	–	
			15	–	40	–	
			20	–	60	–	
Term. 14 (SIGNAL IN) Input Resistance R_{14}			5	–	2	–	MΩ
			10	–	0.4	–	
			15	–	0.2	–	
AC-Coupled Signal Input Voltage Sensitivity* (peak-to-peak)	See Fig.7		5	–	200	–	mV
			10	–	400	–	
			15	–	700	–	
DC-Coupled Signal Input and Comparator Input Voltage Sensitivity Low Level			5	1.5	2.25	–	V
			10	3	4.5	–	
			15	4.5	6.75	–	
High Level		V_O Volts	5	–	2.75	3.5	
			10	–	5.5	7	
			15	–	8.25	11	
Output Drive Current: n-Channel (Sink), I_{DN}	Phase Comparator I & II (Term. 2 & 13) and Phase Pulses	0.4	5	0.51	1	–	mA
		0.5	10	1.3	2.6	–	
		1.5	15	3.4	6.8	–	
p-Channel (Source), I_{DP}	Phase Comparator I & II (Term. 2 & 13) and Phase Pulses	4.6	5	−0.51	−1	–	
		9.5	10	−1.3	−2.6	–	
		13.5	15	−3.4	−6.8	–	
Input Current, I_{IN}	Any Input Except Term. 14	–	18	–	$\pm 10^{-5}$	±0.1	μA
3-State Output Leakage Current, I_{OUT}	Term. 13	0,18	18	–	$\pm 10^{-4}$	–	μA

* For sine wave, the frequency must be greater than 1 kHz for Phase Comparator II.

RECOMMENDED OPERATING CONDITIONS at T_A = Full Package-Temperature Range

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS Min.	Max.	UNITS
Supply-Voltage Range VCO Section:			
As Fixed Oscillator	3	18	V
Phased-Lock-Loop Operation	5	18	
Supply-Voltage Range Phase Comparator Section:			
Comparators	3	18	
VCO Operation	5	18	

DESIGN INFORMATION

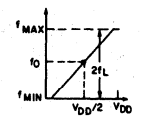
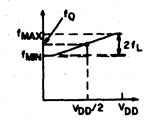
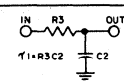
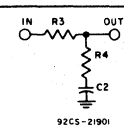
This information is a guide for approximating the values of external components for the CD4046A in a Phase-Locked-Loop system.

The selected external components must be within the following ranges:

$5\ k\Omega \leq R1, R2, R_S \leq 1\ M\Omega$

$C1 \geq 100\ pF$ at $V_{DD} \geq 5\ V$;

$C1 \geq 50\ pF$ at $V_{DD} \geq 10\ V$

Characteristics	Phase Comparator Used	Design Information	
VCO Frequency	1	VCO WITHOUT OFFSET $R_2 = \infty$	VCO WITH OFFSET
			
	2	Same as for No.1	
For No Signal Input	1	VCO will adjust to center frequency, f_o	
	2	VCO will adjust to lowest operating frequency, f_{min}	
Frequency Lock Range, $2f_L$	1	$2f_L$ = full VCO frequency range	
		$2f_L = f_{max} - f_{min}$	
	2	Same as for No.1	
Frequency Capture Range, $2f_C$	1	 $\tau 1 = R3C2$	(1), (2) $2f_C \approx \frac{1}{\pi}\sqrt{\frac{2\pi f_L}{\tau 1}}$
Loop Filter Component Selection			For $2f_C$, see Ref. (2)
	2	$f_C = f_L$	
Phase Angle Between Signal and Comparator	1	90^o at center frequency (f_o) approximating 0^o and 180^o at ends of lock range ($2f_L$)	
	2	Always 0^o in lock	
Locks On Harmonic of Center Frequency	1	Yes	
	2	No	
Signal Input Noise Rejection	1	High	
	2	Low	

For further information, see

(1) F. Gardner, "Phase-Lock Techniques" John Wiley and Sons, New York, 1966

(2) G. S. Moschytz, "Miniaturized RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.

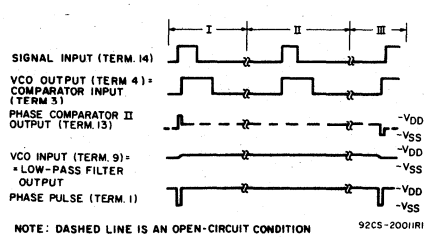


Fig.4 – Typical waveforms for COS/MOS phase-locked loop employing phase comparator II in locked condition.

CD4047B Types

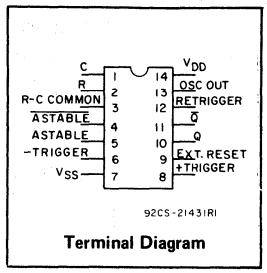
COS/MOS Low-Power Monostable/Astable Multivibrator

High Voltage Types (20-Volt Rating)

Preliminary Data

Features:

- **Low power consumption: special COS/MOS oscillator configuration**
- **Monostable (one-shot) or astable (free-running) operation**
- **True and complemented buffered outputs**
- **Only one external R and C required**
- **Buffered inputs**
- **100% tested for quiescent current at 20 V**
- **Standardized, symmetrical output characteristics**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**



Terminal Diagram

Monostable Multivibrator Features:

- **Internal power-on reset circuit**
- **Positive- or negative-edge trigger**
- **Output pulse width independent of trigger pulse duration**
- **Retriggerable option for pulse width expansion**
- **Internal power-on reset circuit**
- **Long pulse widths possible using small RC components by means of external counter provision**
- **Fast recovery time essentially independent of pulse width**
- **Pulse-width accuracy maintained at duty cycles approaching 100%**

Astable Multivibrator Features:

- **Free-running or gatable operating modes**
- **50% duty cycle**
- **Oscillator output available**
- **Good astable frequency stability:**
  Frequency deviation:
  = ±2% + 0.03%/°C @ 100 kHz
  = ±0.5% + 0.015%/°C @ 10 kHz
  (circuits "trimmed" to frequency V_{DD} = 10 V ±10%)

Applications:

Digital equipment where low-power dissipation and/or high noise immunity are primary design requirements:

- **Envelope detection**
- **Frequency multiplication**
- **Frequency division**
- **Frequency discriminators**
- **Timing circuits**
- **Time-delay applications**

The RCA-CD4047B consists of a gatable astable multivibrator with logic techniques incorporated to permit positive or negative edge-triggered monostable multivibrator action with retriggering and external counting options.

Inputs include +TRIGGER, -TRIGGER, ASTABLE, $\overline{\text{ASTABLE}}$, RETRIGGER, and EXTERNAL RESET. Buffered outputs are Q, $\overline{Q}$, and OSCILLATOR. In all modes of operation, an external capacitor must be connected between C-Timing and RC-Common terminals, and an external resistor must be connected between the R-Timing and RC-Common terminals.

Astable operation is enabled by a high level on the ASTABLE input. The period of the square wave at the Q and $\overline{Q}$ Outputs in this mode of operation is a function of the external components employed. "True" input pulses on the ASTABLE input or "Complement" pulses on the $\overline{\text{ASTABLE}}$ input allow the circuit to be used as a gatable multivibrator. The OSCILLATOR output period will be half of the Q terminal output in the astable mode. However, a 50% duty cycle is not guaranteed at this output.

In the monostable mode, positive-edge triggering is accomplished by application of a leading-edge pulse to the +TRIGGER input and a low level to the -TRIGGER input. For negative-edge triggering, a trailing-edge pulse is applied to the -TRIGGER and a high level is applied to the +TRIGGER. Input pulses may be of any duration relative to the output pulse. The multivibrator can be retriggered (on the leading edge only) by applying a common pulse to both the RETRIGGER and +TRIGGER inputs. In this mode the output pulse remains high as long as the input pulse period is shorter than the period determined by the RC components.

An external countdown option can be implemented by coupling "Q" to an external "N" counter and resetting the counter with the trigger pulse. The counter output pulse is fed back to the $\overline{\text{ASTABLE}}$ input and has a duration equal to N times the period of the multivibrator.

A high level on the EXTERNAL RESET input assures no output pulse during an "ON" power condition. This input can also be activated to terminate the output pulse at any time, For monostable operation, whenever V_{DD} is applied, an internal power-on reset circuit will clock the Q output low within one output period (t_M).

The CD4047B-Series types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

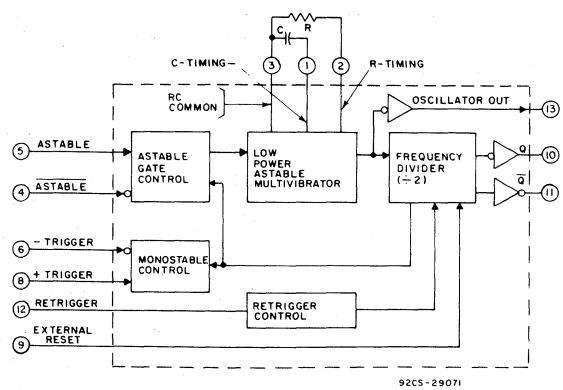


Fig. 1 – CD4047A logic block diagram.

CD4047B FUNCTIONAL TERMINAL CONNECTIONS
NOTE: IN ALL CASES EXTERNAL RESISTOR BETWEEN TERMINALS 2 AND 3▲
EXTERNAL CAPACITOR BETWEEN TERMINALS 1 AND 3▲

FUNCTION	TERMINAL CONNECTIONS			OUTPUT PULSE FROM	OUTPUT PERIOD OR PULSE WIDTH
	TO V_{DD}	TO V_{SS}	INPUT PULSE TO		
Astable Multivibrator:					
Free Running	4,5,6,14	7,8,9,12	–	10,11,13	$t_A(10,11) = 4.40\ RC$
True Gating	4,6,14	7,8,9,12	5	10,11,13	$t_A(13) = 2.20\ RC$
Complement Gating	6,14	5,7,8,9,12	4	10,11,13	
Monostable Multivibrator:					
Positive-Edge Trigger	4,14	5,6,7,9,12	8	10,11	
Negative-Edge Trigger	4,8,14	5,7,9,12	6	10,11	$t_M(10,11) = 2.48\ RC$
Retriggerable	4,14	5,6,7,9	8,12	10,11	
External Countdown*	14	5,6,7,8,9,12	–	10,11	

* Input Pulse to Reset of External Counting Chip
External Counting Chip Output To Terminal 4

▲ See Text.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . -0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . -55 to +125°C
PACKAGE TYPE E . . . . . -40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

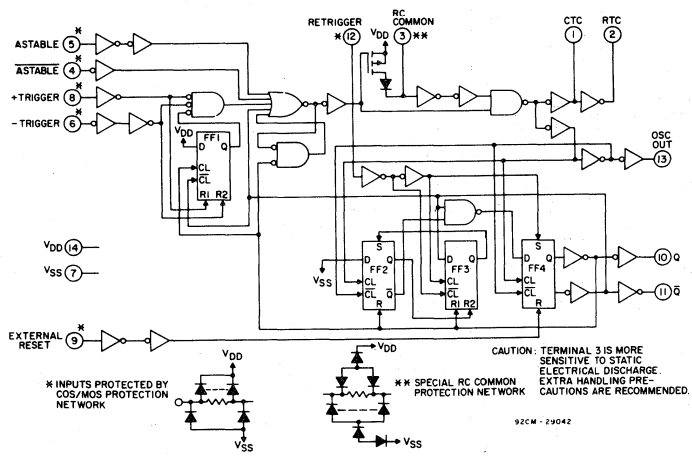


Fig. 2 – CD4047B logic diagram.

Retrigger Mode Operation

The CD4047B can be used in the retrigger mode to extend the output-pulse duration, or to compare the frequency of an input signal with that of the internal oscillator. In the retrigger mode the input pulse is applied to terminals 8 and 12, and the output is taken from terminal 10 or 11. As shown in Fig. 4, normal monostable action is obtained when one retrigger pulse is applied. Extended pulse duration is obtained when more than one pulse is applied. For two input pulses, $t_{RE} = t_1' + t_1 + 2t_2$. For more than two pulses, t_{RE} (Q OUTPUT) terminates at some variable time t_D after the termination of the last retrigger pulse. t_D is variable because t_{RE} (Q OUTPUT) terminates after the second positive edge of the oscillator output appears at flip-flop 4 (see Fig. 2).

External Counter Option

Time t_M can be extended by any amount with the use of external counting circuitry. Advantages include digitally controlled pulse duration, small timing capacitors for long time periods, and extremely fast recovery time. A typical implementation is shown in Fig. 5. The pulse duration at the output is

$$t_{ext} = (N - 1)(t_A) + (t_M + t_A/2)$$

where t_{ext} = pulse duration of the circuitry, and N is the number of counts used.

Timing-Component Limitations

The capacitor used in the circuit should be non-polarized and have low leakage (i.e. the parallel resistance of the capacitor should be an order of magnitude greater than the external resistor used). There is no upper or lower limit for either R or C value to maintain oscillation.

However, in consideration of accuracy, C must be much larger than the inherent stray capacitance in the system (unless this capacitance can be measured and taken into account). R must be much larger than the COS/MOS "ON" resistance in series with it, which typically is hundreds of ohms. In addition, with very large values of R, some short-term instability with respect to time may be noted.

The recommended values for these components to maintain agreement with previously calculated formulas without trimming should be:

$C \geqslant 100$ pF, up to any practical value, for astable modes;

$C \geqslant 1000$ pF, up to any practical value for monostable modes.

$10\ k\Omega \leqslant R \leqslant 1\ M\Omega$

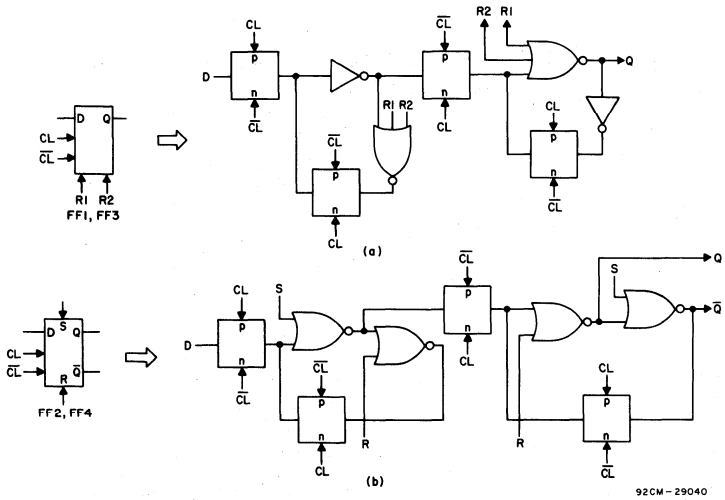


Fig. 3 – Detail logic diagram for flip-flops FF1 and FF3 (a) and for flip-flops FF2 and FF4 (b).

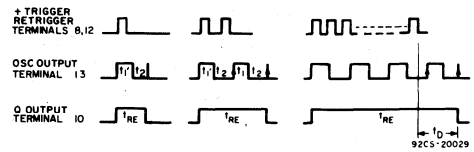


Fig. 4 – Retrigger-mode waveforms.

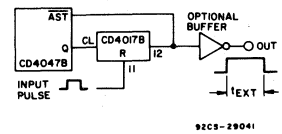


Fig. 5 – Implementation of external counter option.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at -55, +25, +125 Apply to D,K,F,H Packages Values at -40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	–	
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	–	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	–	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	

STATIC ELECTRICAL CHARACTERISTICS (CONTINUED)

Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	V
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5, 13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1.9	–	10	7				7	–	–	
	1.5, 13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS *at $T_A = 25°C$, Input t_r, $t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200$ kΩ*

CHARACTERISTICS	TEST CONDITIONS		TYPICAL VALUES	UNITS
		V_{DD} (Volts)		
Propagation Delay Time: t_{PHL}, t_{PLH} — Astable, $\overline{\text{Astable}}$ to Osc. Out		5	200	ns
		10	100	
		15	70	
Astable, $\overline{\text{Astable}}$ to Q, $\overline{Q}$		5	550	
		10	250	
		15	150	
+Trigger, – Trigger to Q, $\overline{Q}$		5	700	
		10	300	
		15	200	
+Trigger, Retrigger to Q, $\overline{Q}$		5	300	
		10	175	
		15	125	
External Reset to Q, $\overline{Q}$		5	300	
		10	125	
		15	75	
Transition Time: t_{THL}, t_{TLH} — Osc. Out Q, $\overline{Q}$		5	100	
		10	50	
		15	40	
Minimum Input Pulse Width (any input), t_W		5	500	
		10	200	
		15	140	
+Trigger, Retrigger Rise & Fall Time, t_r, t_f		5	Unlimited	μs
		10		
		15		
Input Capacitance, C_{IN}	Any Input		5	pF

CD4048B Types

COS/MOS Multifunction Expandable 8-Input Gate

High-Voltage Types (20-Volt Rating)

Preliminary Data

The RCA-CD4048B is an 8-input gate having four control inputs. Three binary control inputs – Ka, Kb, and Kc – provide the implementation of eight different logic functions. These functions are OR, NOR, AND, NAND, OR/AND, OR/NAND, AND/OR and AND/NOR.

A fourth control input – Kd provides the user with a 3-state output. When control input Kd is high the output is either a logic 1 or a logic 0 depending on the inner states. When control input Kd is low, the output is an open circuit. This feature enables the user to connect this device to a common bus line.

In addition to the eight input lines, an EXPAND input is provided that permits the user to increase the number of inputs to one CD4048B, (see Fig.2). For example, two CD4048B's can be cascaded to provide a 16-input multifunction gate. When the EXPAND input is not used, it should be connected to V_{SS}.

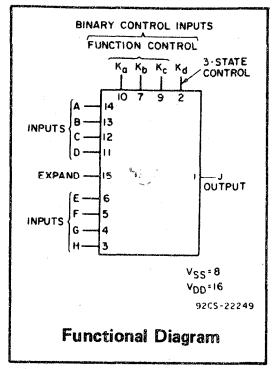
The CD4048B-Series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Three-state output**
- **Many logic functions available in one package**
- **100% tested for quiescent current at 20 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Standardized, symmetrical output characteristics**
- **Meets all requirements of JEDEC Tentative Standard No.13A, "Standard Specifications for Description of "B" Series CMOS Devices"**

Applications:

- **Selection of up to 8 logic functions**
- **Digital control of logic**
- **General-purpose gating logic**
  - **Decoding**
  - **Encoding**



Functional Diagram

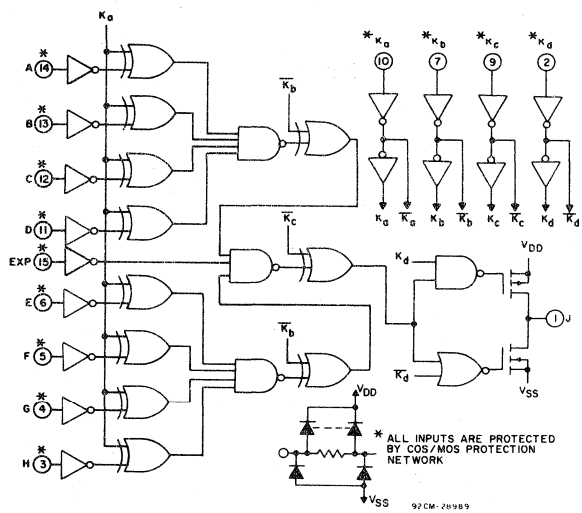


Fig.2 – Logic diagram.

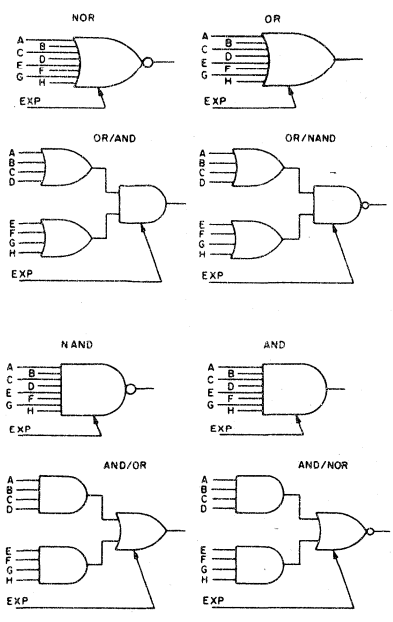


Fig.1 – Basic logic configurations.

FUNCTION TRUTH TABLE

OUTPUT FUNCTION	BOOLEAN EXPRESSION	K_a	K_b	K_c	UNUSED INPUT*
NOR	$J=\overline{A+B+C+D+E+F+G+H}$	0	0	0	V_{SS}
OR	$J=A+B+C+D+E+F+G+H$	0	0	1	V_{SS}
OR/AND	$J=(A+B+C+D)\cdot(E+F+G+H)$	0	1	0	V_{SS}
OR/NAND	$J=\overline{(A+B+C+D)\cdot(E+F+G+H)}$	0	1	1	V_{SS}
AND	$J=ABCDEFGH$	1	0	0	V_{DD}
NAND	$J=\overline{ABCDEFGH}$	1	0	1	V_{DD}
AND/NOR	$J=\overline{ABCD+EFGH}$	1	1	0	V_{DD}
AND/OR	$J=ABCD+EFGH$	1	1	1	V_{DD}

K_d=1 Normal Inverter Action

K_d=0 High Impedance Output

EXPAND Input=0

* See Figs. 1,2,3,4, and 5.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
									+25		
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				—	—	1.5	V
	1,9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	—	—	
	1,9	–	10	7				7	—	—	
	1.5,13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA
3-State Output Current, I_{OUT}	0,18	0,18	18	±0.4	±0.4	±12	±12	–	$\pm 10^{-4}$	±0.4	μA

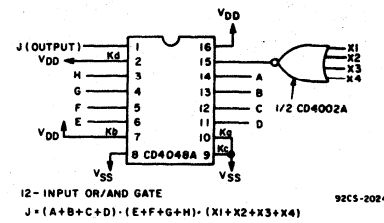


Fig.3 – 12-input OR/AND gate.

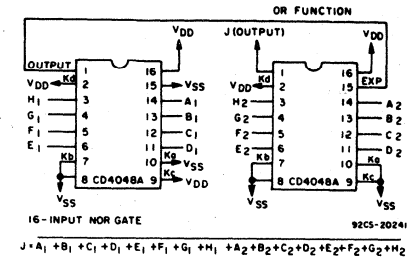
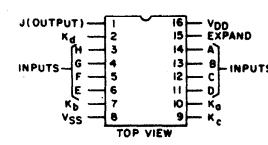


Fig.4 – 16-input NOR gate.



TERMINAL ASSIGNMENT

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 50 pF, Input t_r, t_f = 20 ns, R_L = 200 kΩ

CHARACTERISTIC	TEST COND. VDD (V)	TYPICAL VALUES	UNITS
Propagation Delay Time: t_{PHL}, t_{PLH}	5	300	ns
	10	130	
	15	100	
Transition Time: t_{THL}, t_{TLH}	5	100	ns
	10	50	
	15	40	
Input Capacitance C_{IN} (Any Input)	–	5	pF

Applications of Expand Input

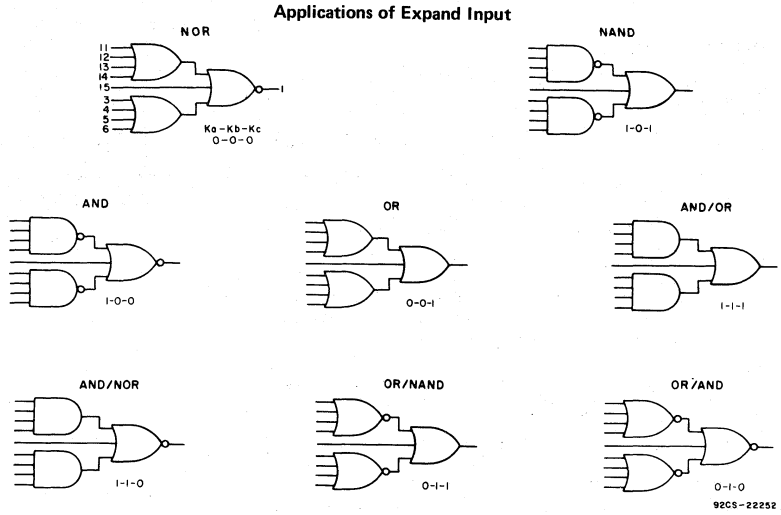


Fig.5 – Actual-circuit logic configurations.

IMPLEMENTATION OF EXPAND INPUT FOR 9 OR MORE INPUTS

OUTPUT FUNCTION	FUNCTION NEEDED AT EXPAND INPUT	OUTPUT BOOLEAN EXPRESSION
NOR	OR	$J=\overline{(A+B+C+D+E+F+G+H)+(EXP)}$
OR	OR	$J=(A+B+C+D+E+F+G+H)+(EXP)$
AND	NAND	$J=(ABCDEFGH)\cdot(EXP)$
NAND	NAND	$J=\overline{(ABCDEFGH)\cdot(EXP)}$
OR/AND	NOR	$J=(A+B+C+D)\cdot(E+F+G+H)\cdot(EXP)$
OR/NAND	NOR	$J=\overline{(A+B+C+D)\cdot(E+F+G+H)\cdot(EXP)}$
AND/NOR	AND	$J=\overline{(ABCD)+(EFGH)+(EXP)}$
AND/OR	AND	$J=(ABCD)+(EFGH)+(EXP)$

Note: (EXP) designates the EXPAND function (i.e., $X_1+X_2+\ldots X_N$).

NOTE:
Refer to FUNCTION TRUTH TABLE for connection of unused inputs.

COS/MOS Hex Buffer/Converters

High-Voltage Types (20-Volt Rating)

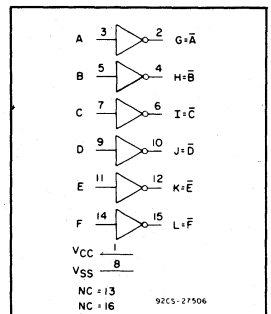
CD4049UB—Inverting Type
CD4050B—Non-Inverting Type

Features:

- High sink current for driving 2 TTL loads
- High-to-low level logic conversion
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- 5-, 10-, and 15-volt parametric ratings

Applications:

- COS/MOS to DTL/TTL hex converter
- COS/MOS current "sink" or "source" driver
- COS/MOS high-to-low logic-level converter

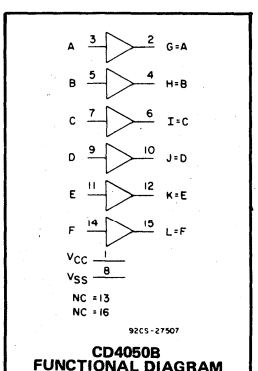


CD4049UB FUNCTIONAL DIAGRAM

The RCA-CD4049UB and CD4050B are inverting and non-inverting hex buffers, respectively, and feature logic-level conversion using only one supply voltage (V_{CC}). The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage when these devices are used for logic-level conversions. These devices are intended for use as COS/MOS to DTL/TTL converters and can drive directly two DTL/TTL loads. (V_{CC}=5 V, $V_{OL} \leq$ 0.4 V, and $I_{OL} \geq$ 3.2 mA.)

The CD4049UB and CD4050B are designated as replacements for CD4009UB and CD4010B, respectively. Because the CD4049UB and CD4050B require only one power supply, they are preferred over the CD4009UB and CD4010B and should be used in place of the CD4009UB and CD4010B in all inverter, current driver, or logic-level conversion applications. In these applications the CD4049UB and CD4050B are pin compatible with the CD4009UB and CD4010B respectively, and can be substituted for these devices in existing as well as in new designs. Terminal No. 16 is not connected internallyon the CD4049UB or CD4050B, therefore, connection to this terminal is of no consequence to circuit operation. For applications not requiring high sink-current or voltage conversion, the CD4069UB Hex Inverter is recommended.

The CD4049UB and CD4050B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).



CD4050B FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to +20.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

RECOMMENDED OPERATING CONDITIONS at T_A=25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (V_{CC}) (For T_A=Full Package-Temperature Range)	3	18	V
Input Voltage Range (V_{IN})	V_{CC}*	18	V

*The CD4049 and CD4050 have high-to-low-level voltage conversion capability but not low-to-high-level; therefore it is recommended that $V_{IN} \geq V_{CC}$.

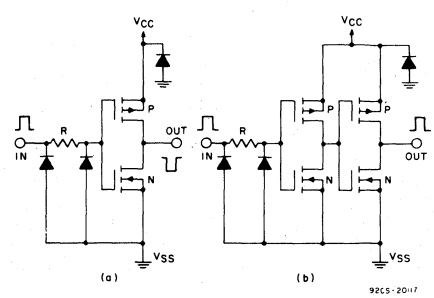


Fig. 1—a) Schematic diagram of CD4049UB, 1 of 6 identical units; b) Schematic diagram of CD4050B, 1 of 6 identical units.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			Limits At Indicated Temperatures (°C) *Values at −55,+25,+125 Apply to D,K,F,H Pkgs. Values at −40,+25,+85 Apply to E Package*							UNITS
	V_O (V)	V_{IN} (V)	V_{CC} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	4.5	3.3	3.1	2.1	1.8	2.6	5.2	–	mA
	0.4	0,5	5	4	3.8	2.9	2.4	3.2	6.4	–	
	0.5	0,10	10	10	9.6	6.6	5.6	8	16	–	
	1.5	0,15	15	26	25	20	18	24	48	–	
Output High (Source) Current I_{OH} Min.	4.6	0,5	5	−1	−0.9	−0.72	−0.6	−0.8	−1.6	–	
	2.5	0,5	5	−4	−3.6	−2.6	−2.3	−3.2	−6.4	–	
	9.5	0,10	10	−2.2	−2	−1.5	−1.3	−1.8	−3.6	–	
	13.5	0,15	15	−6.6	−6.4	−5	−4.4	−6	−12	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05					0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage: V_{IL} Max. CD4049UB	4.5	–	5	1				–	–	1	V
	9	–	10	2				–	–	2	
	13.5	–	15	2.5				–	–	3	
Input Low Voltage: V_{IL} Max. CD4050B	0.5	–	5	1.5				–	–	1.5	
	1	–	10	3				–	–	2.5	
	1.5	–	15	4				–	–	4	
Input High Voltage: V_{IH} Min. CD4049UB	0.5	–	5	4				4	–	–	
	1	–	10	8				8	–	–	
	1.5	–	15	12.5				12	–	–	
Input High Voltage: V_{IH} Min. CD4050B	4.5	–	5	3.5				3.5	–	–	
	9	–	10	7				7	–	–	
	13.5	–	15	11				11	–	–	
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

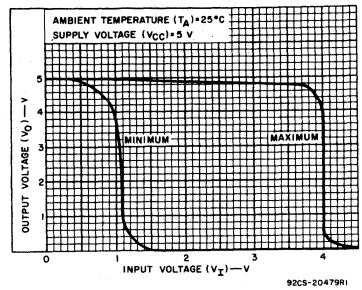


Fig. 2—Minimum and maximum voltage transfer characteristics for CD4049UB.

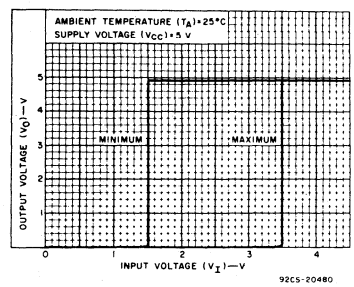


Fig. 3—Minimum and maximum voltage transfer characteristics for CD4050B.

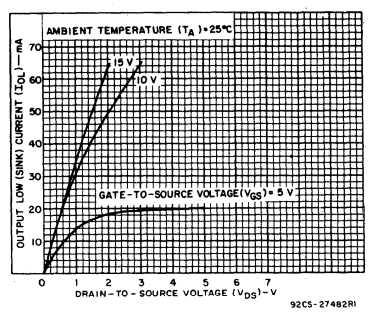


Fig. 4 — Typical output low (sink) current characteristics.

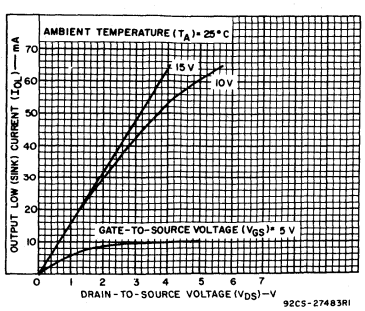


Fig. 5 — Minimum output low (sink) current drain characteristics.

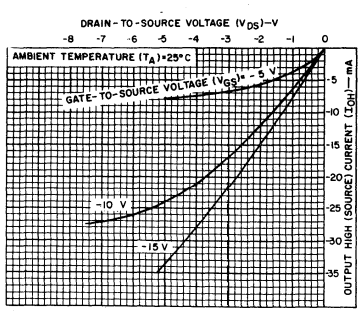


Fig. 6 — Typical output high (source) current characteristics.

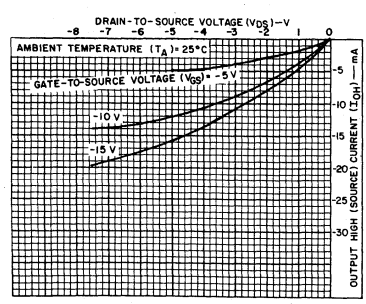


Fig. 7 — Minimum output high (source) current characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C; Input t_r,t_f=20 ns, C_L=50 pF, R_L=200 kΩ

CHARACTERISTIC	CONDITIONS		LIMITS ALL PKGS.		UNITS
	V_{IN}	V_{CC}	Typ.	Max.	
Propagation Delay Time:					
Low-to-High, t_{PLH}	5	5	60	120	ns
	10	10	32	65	
CD4049UB	10	5	45	90	
	15	15	25	50	
	15	5	45	90	
	5	5	70	140	
	10	10	40	80	
CD4050B	10	5	45	90	
	15	15	30	60	
	15	5	40	80	
High-to-Low, t_{PHL}	5	5	32	65	ns
	10	10	20	40	
CD4049UB	10	5	15	30	
	15	15	15	30	
	15	5	10	20	
	5	5	55	110	
	10	10	22	55	
CD4050B	10	5	50	100	
	15	15	15	30	
	15	5	50	100	
Transition Time:					
Low-to-High, t_{TLH}	5	5	80	160	ns
	10	10	40	80	
	15	15	30	60	
	5	5	30	60	
High-to-Low, t_{THL}	10	10	20	40	
	15	15	15	30	
Input Capacitance, C_{IN}					
CD4049UB	–	–	15	22.5	pF
CD4050B	–	–	5	7.5	

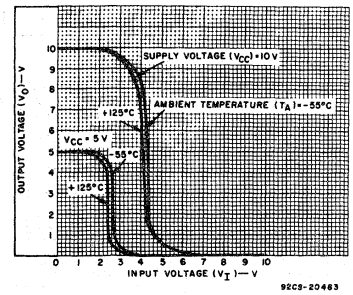


Fig. 8 – Typical voltage transfer characteristics as a function of temperature for CD4049UB.

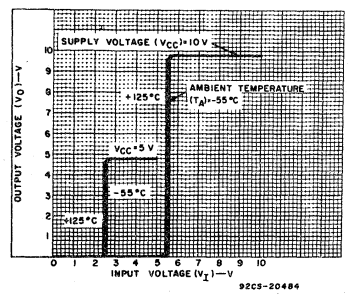


Fig. 9 – Typical voltage transfer characteristics as a function of temperature for CD4050B.

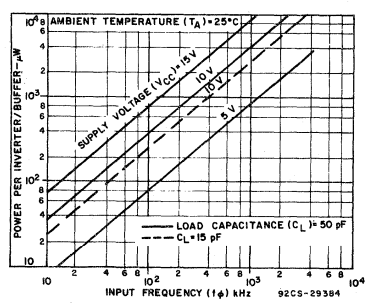


Fig. 10 – Typical power dissipation vs. frequency characteristics.

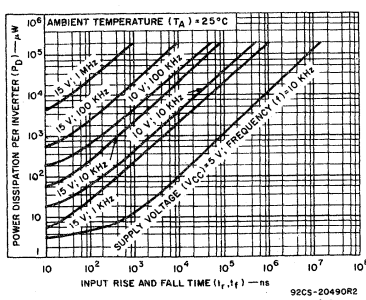


Fig. 11 – Typical power dissipation vs. transition time per inverter for CD4049UB.

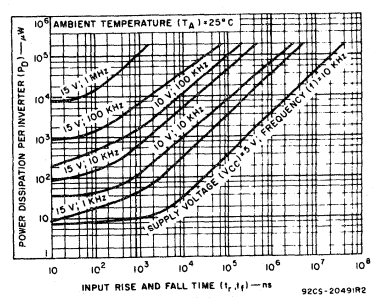


Fig. 12 – Typical power dissipation vs. transition timer per inverter for CD4050B.

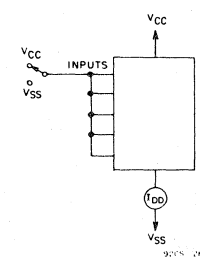


Fig. 13 – Quiescent device current test circuit.

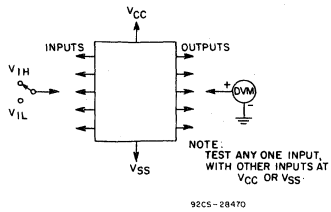


Fig. 14 – Input voltage test circuit.

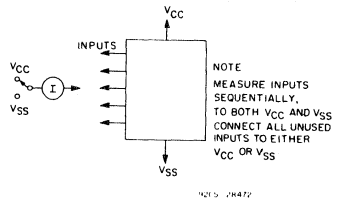


Fig. 15 – Input current test circuit.

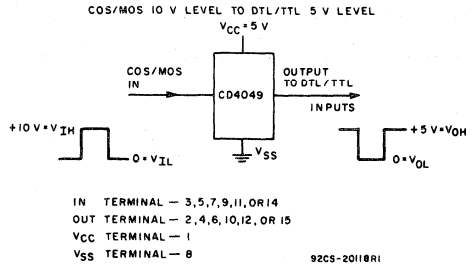
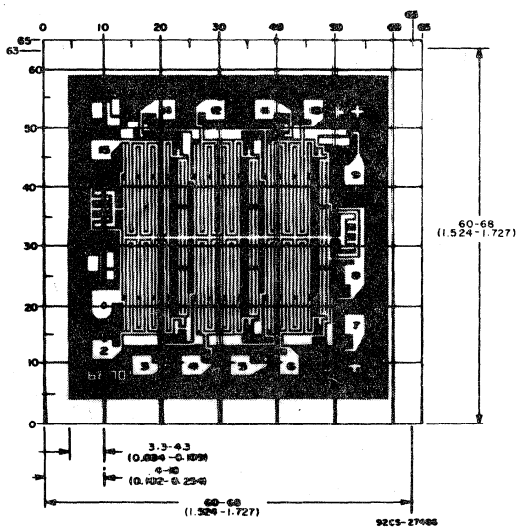


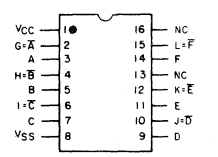
Fig. 16 – Logic-level conversion application.



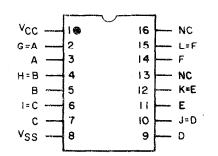
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Photograph of chip for CD4049UB. Dimensions and pad layout for CD4050B are identical.

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.



CD4049



CD4050

TERMINAL ASSIGNMENTS

COS/MOS Analog Multiplexers/Demultiplexers*

With Logic-Level Conversion

High-Voltages Types (20-Volt Rating)

CD4051B — Single 8-Channel
CD4052B — Differential 4-Channel
CD4053B — Triple 2-Channel

RCA-CD4051B, CD4052B, and CD4053B analog multiplexers/demultiplexers are digitally controlled analog switches having low ON impedance and very low OFF leakage current. Control of analog signals up to 20 V peak-to-peak can be achieved by digital signal amplitudes of 4.5 to 20 V (if V_{DD}-V_{SS} = 3 V, a V_{DD}-V_{EE} of up to 13 V can be controlled; for V_{DD}-V_{EE} level differences above 13 V, a V_{DD}-V_{SS} of at least 4.5 V is required). For example, if V_{DD} = +5 V, V_{SS} = 0, and V_{EE} = −13.5 V, analog signals from −13.5 V to +4.5 V can be controlled by digital inputs of 0 to 5 V. These multiplexer circuits dissipate extremely low quiescent power over the full V_{DD}-V_{SS} and V_{DD}-V_{EE} supply-voltage ranges, independent of the logic state of the control signals. When a logic "1" is present at the inhibit input terminal all channels are off.

The CD4051B is a single 8-channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output.

The CD4052B is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

The CD4053B is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole double-throw configuration.

The CD4051B, CD4052B, and CD4053B are supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead plastic dual-in-line packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

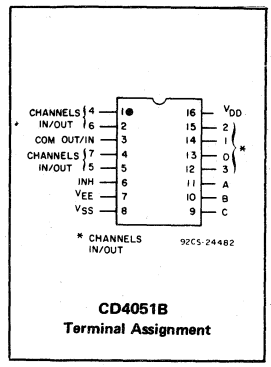
* When these devices are used as demultiplexers, the "CHANNEL IN/OUT" terminals are the outputs and the "COMMON OUT/IN" terminals are the inputs.

Applications:

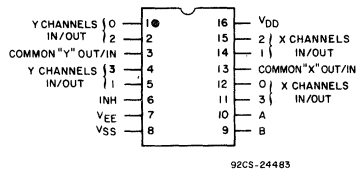
- Analog and digital multiplexing and demultiplexing
- A/D and D/A conversion
- Signal gating

Features:

- Wide range of digital and analog signal levels: digital 3 to 20 V, analog to 20 V_{p-p}
- Low ON resistance: 125 Ω (typ.) over 15 V_{p-p} signal-input range for V_{DD}-V_{EE} = 15 V
- High OFF resistance: channel leakage of ±100 pA (typ.) @ V_{DD}-V_{EE} = 18 V
- Logic-level conversion for digital addressing signals of 3 to 20 V (V_{DD}-V_{SS} = 3 to 20 V) to switch analog signals to 20 V p-p (V_{DD}-V_{EE} = 20 V); see introductory text
- Matched switch characteristics: R_{ON} = 5 Ω (typ.) for V_{DD}-V_{EE} = 15 V
- Very low quiescent power dissipation under under all digital-control input and supply conditions: 0.2 μW (typ.) @ V_{DD}-V_{SS} = V_{DD}-V_{EE} = 10 V
- Binary address decoding on chip
- 5-, 10-, and 15-V parametric ratings
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"



CD4051B
Terminal Assignment



CD4052B

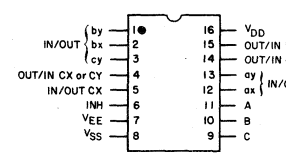
Terminal Assignment

RECOMMENDED OPERATING CONDITIONS AT T_A =25°C (Unless Otherwise Specified)

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges. Values shown apply to all types except as noted.

CHARACTERISTIC	V_{DD}	Min.	Max.	Units
Supply-Voltage Range (T_A = Full Package-Temp. Range)	–	3	18	V
Multiplexer Switch Input Current Capability*	–	–	25	mA
Output Load Resistance	–	100	–	Ω

* In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R_{ON} values shown in ELECTRICAL CHARACTERISTICS CHART). No V_{DD} current will flow through R_L if the switch current flows into terminal 3 on the CD4051; terminals 3 and 13 on the CD4052; terminals 4,14, and 15 on the CD4053.



CD4053B

Terminal Assignment

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} or V_{EE}, whichever is more negative) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

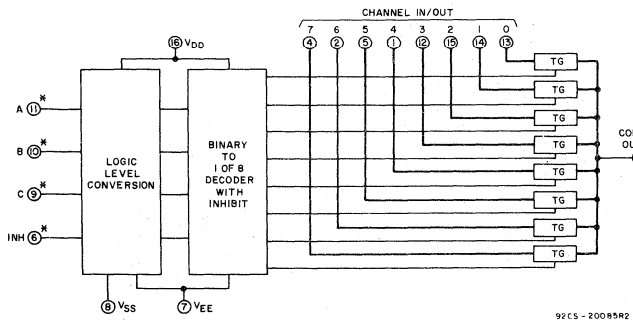


Fig. 1 – Functional diagram of CD4051B.

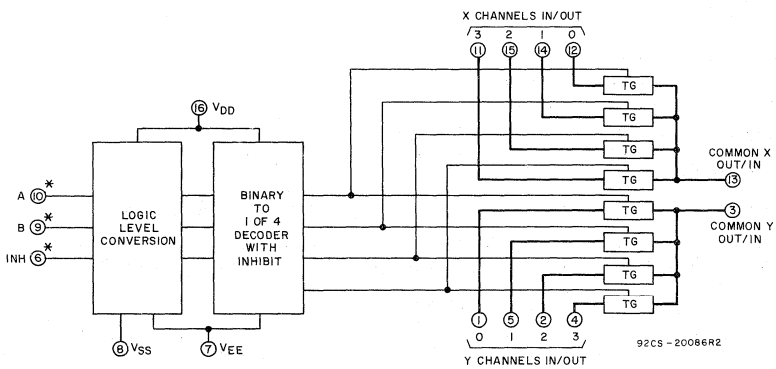


Fig. 2 – Functional diagram of CD4052B.

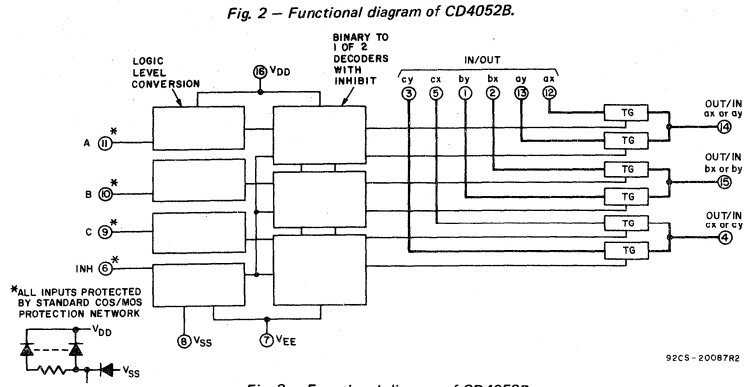


Fig. 3 – Functional diagram of CD4053B.

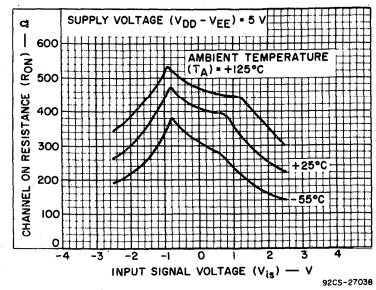


Fig.4 – Typical channel ON resistance vs input signal voltage (all types).

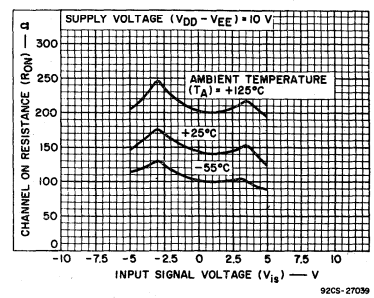


Fig.5 – Typical channel ON resistance vs. input signal voltage (all types).

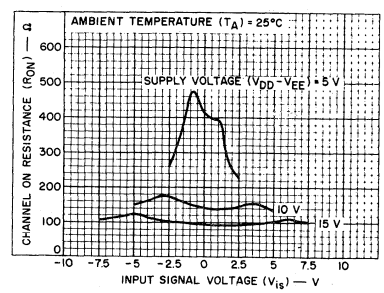


Fig.6 – Typical channel ON resistance vs. input signal voltage (all types).

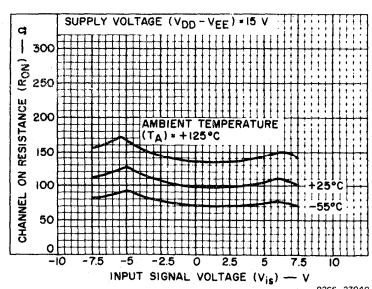


Fig.7 – Typical channel ON resistance vs. input signal voltage (all types).

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_{is} (V)	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	LIMITS at Indicated Temperature (°C) Values at −55,+25,+125, apply to D,F,K,H pkg Values at −40,+25,+85, apply to E pkgs −55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	Units
SIGNAL INPUTS (V_{is}) AND OUTPUTS (V_{OS})												
Quiescent Device Current, I_{DD} Max.				5	5	5	150	150	–	0.04	5	μA
				10	10	10	300	300	–	0.04	10	
				15	20	20	600	600	–	0.04	20	
				20	100	100	3000	3000	–	0.08	100	
ON Resistance $0 \leqslant V_{is} \leqslant V_{DD}$												
R_{ON} Max.		0	0	5	2000	2100	3200	3500	–	470	2500	Ω
		0	0	10	310	330	520	580	–	180	400	
		0	0	15	220	230	360	400	–	125	280	
Δ ON Resistance (Between Any Two Channels)												
ΔR_{ON}		0	0	5	–	–	–	–	–	10	–	Ω
		0	0	10	–	–	–	–	–	10	–	
		0	0	15	–	–	–	–	–	5	–	
OFF Channel Leakage Current:												
Any Channel OFF Max.		0	0	10			±200*		–	±0.01	±200*	nA
		0	0	15			±500*		–	±0.01	±200*	
		0	0	20			±1000*		–	±0.01	±200*	
All Channels OFF (Common OUT/IN) Max.		0	0	10			±200*		–	±0.01	±200*	
		0	0	15			±500*		–	±0.01	±200*	
		0	0	20			±1000*		–	±0.01	±200*	
Capacitance: Input, C_{is}					–	–	–	–	–	5	–	pF
Output, C_{os}												
CD4051		−5	−5	5	–	–	–	–	–	30	–	
CD4052					–	–	–	–	–	18	–	
CD4053					–	–	–	–	–	9	–	
Feedthrough, C_{ios}					–	–	–	–	–	0.2	–	
Propagation Delay Time (Signal Input to Output	10V	$R_L = 10\,k\Omega$		5	–	–	–	–	–	30	–	ns
		$C_L = 50$ pF		10	–	–	–	–	–	15	–	
		$t_r, t_f = 20$ ns		15	–	–	–	–	–	11	–	

* Determined by minimum feasible leakage measurement for automatic testing.

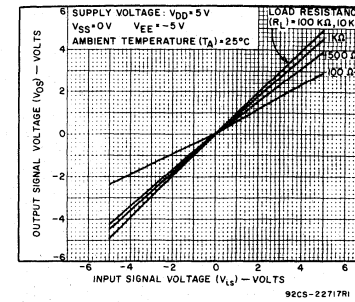


Fig.8 – Typical ON characteristics for 1 of 8 channels (CD4051B).

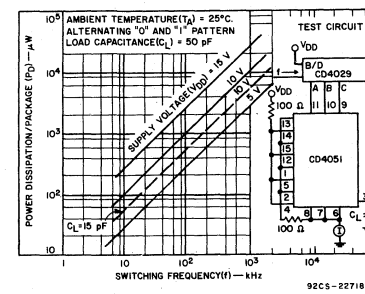


Fig.9 – Typical dynamic power dissipation vs. switching frequency (CD4051B).

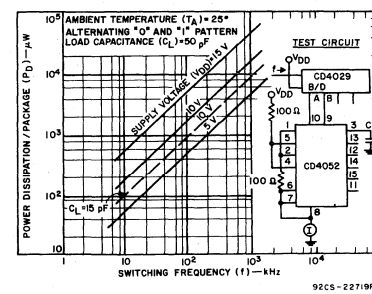


Fig.10 – Typical dynamic power dissipation vs. switching frequency (CD4052B).

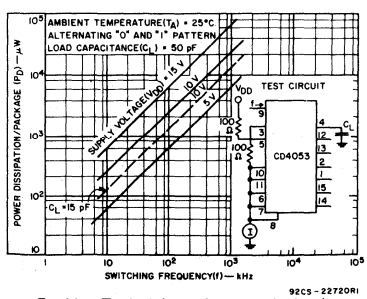
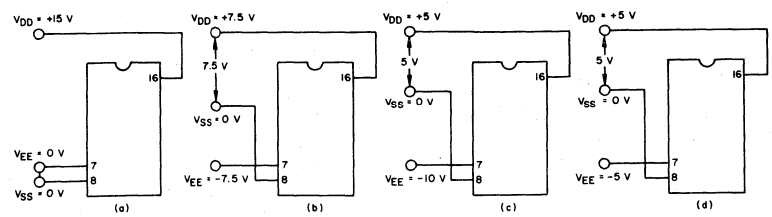


Fig.11 – Typical dynamic power dissipation vs. switching frequency (CD4053B).



The ADDRESS (digital-control inputs) and INHIBIT logic levels are: "0" = V_{SS} and "1" = V_{DD}. The analog signal (through the TG) may swing from V_{EE} to V_{DD}.

Fig.12 – Typical bias voltages.

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	CONDITIONS V_{is} (V)	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	LIMITS at Indicated Temperature (°C) Values at −55,+25,+125, apply to D,F,K,H pkg Values at −40,+25,+85, apply to E pkgs −55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	Units
CONTROL (ADDRESS or INHIBIT) V_C												
Input Low Voltage, V_{IL} Max.	=V_{DD} thru 1 kΩ	V_{EE}=V_{SS} R_L=1 kΩ to V_{SS} I_{IS}< 2 μA on all OFF Channels		5	1.5				–	–	1.5	V
				10	3				–	–	3	
				15	4				–	–	4	
Input High Voltage, V_{IH} Min.				5	3.5				3.5	–	–	
				10	7				7	–	–	
				15	11				11	–	–	
Input Current, I_{IN} Max.	V_{IN} = 0.18			18	±0.1	±0.1	±1	±1	–	±10^{-5}	±0.1	μA
Propagation Delay Time: Address-to-Signal OUT (Channels ON or OFF) See Figs.14,15,18	t_r,t_f = 20 ns, C_L = 50 pF											
		0	0	5	–	–	–	–	–	360	720	ns
		0	0	10	–	–	–	–	–	160	320	
		0	0	15	–	–	–	–	–	120	240	
		−5	0	5	–	–	–	–	–	225	450	
Inhibit-to-Signal OUT (Channel turning ON)	R_L=10 kΩ, C_L=50 pF t_r, t_f = 20 ns											
		0	0	5	–	–	–	–	–	360	720	ns
		0	0	10	–	–	–	–	–	160	320	
		0	0	15	–	–	–	–	–	120	240	
		−10	0	5	–	–	–	–	–	200	400	
Inhibit-to-Signal OUT (Channel turning OFF)	R_L=300Ω, C_L=50 pF t_r,t_f = 20 ns											
		0	0	5	–	–	–	–	–	200	450	ns
		0	0	10	–	–	–	–	–	90	210	
		0	0	15	–	–	–	–	–	70	160	
		−10	0	5	–	–	–	–	–	130	300	
Input Capacitance, C_{IN} (Any Address or Inhibit Input)					–	–	–	–	–	5	7.5	pF

INPUT STATES INHIBIT	C	B	A	"ON" CHANNEL(S)
CD4051B				
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	X	X	X	NONE
CD4052B				
INHIBIT	**B**	**A**		
0	0	0		0x, 0y
0	0	1		1x, 1y
0	1	0		2x, 2y
0	1	1		3x, 3y
1	X	X		NONE
CD4053B				
INHIBIT	**A or B or C**			
0	0			ax or bx or cx
0	1			ay or by or cy
1	X			NONE

X = Don't care

Fig. 13 – Truth tables.

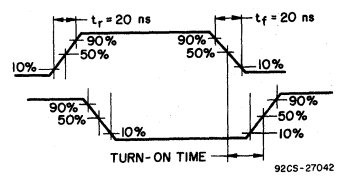


Fig. 14 – Waveforms, channel being turned ON (R_L = 10 kΩ).

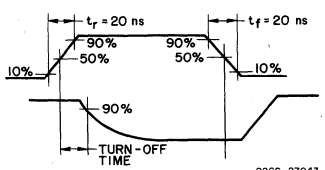


Fig. 15 – Waveforms, channel being turned OFF (R_L = 300 Ω).

TEST CIRCUITS

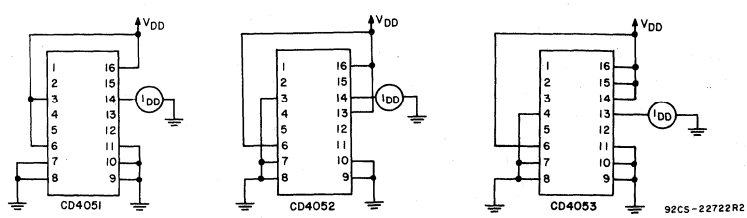


Fig. 16 – OFF channel leakage current – any channel OFF.

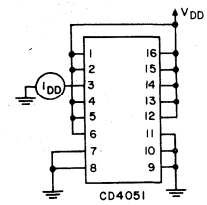
ELECTRICAL CHARACTERISTICS (Cont'd)

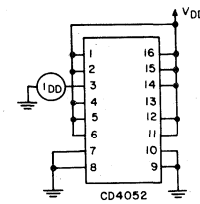
CHARACTERISTIC	TEST CONDITIONS					LIMITS	UNITS
	V_{is} (V)	V_{DD} (V)	R_L (kΩ)			TYPICAL VALUE	
Frequency Response Channel ON (Sine Wave Input)	5●	10	1	V_{os} at Common OUT/IN	CD4053	30	MHz
	$V_{EE} = V_{SS}$, $20 \log \frac{V_{os}}{V_{is}} = -3$ dB				CD4052	25	
					CD4051	20	
				V_{os} at Any Channel		60	
Sine Wave Response (Distortion)	2●	5	10			0.3	%
	3●	10				0.2	
	5●	15				0.12	
	$V_{EE} = V_{SS}$, f_{is} = 1 kHz						
Feedthrough (All Channels OFF)	5●	10	1	V_{os} at Common OUT/IN	CD4053	8	MHz
	$V_{EE} = V_{SS}$, $20 \log \frac{V_{os}}{V_{is}} = -40$dB				CD4052	10	
					CD4051	12	
				V_{os} at Any Channel		8	
Signal Crosstalk (Frequency at −40 dB)	5●	10	1	Between Any 2 Channels		3	MHz
	$V_{EE} = V_{SS}$, $20 \log \frac{V_{os}}{V_{is}} = -40$dB			Between Sections CD4052 Only	Measured on Common	6	
					Measured on Any Channel	10	
				Between Any 2 Sections CD4053 Only	In Pin 2, Out Pin 14	2.5	
					In Pin 15, Out Pin 14	6	
Address-or-Inhibit-to Signal Crosstalk	–	10	10#			65	mV (Peak)
	V_{EE}=0, V_{SS}=0, t_r, t_f =20 ns, $V_C = V_{DD} - V_{SS}$ (Square Wave)						

● Peak-to-peak voltage symmetrical about $\frac{V_{DD} - V_{EE}}{2}$

Both ends of channel

TEST CIRCUITS (Cont'd)





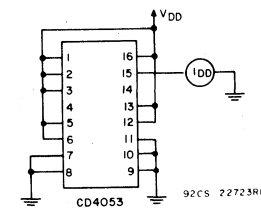


Fig.17 – OFF channel leakage current – all channels OFF.

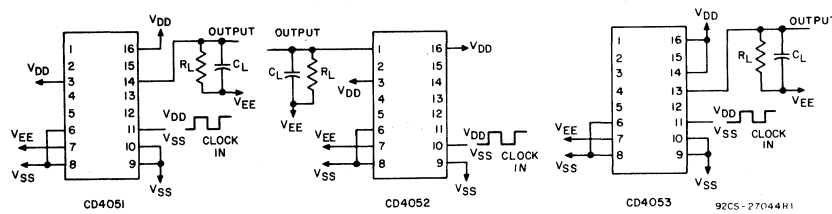


Fig.18 – Propagation delay – address input to signal output.

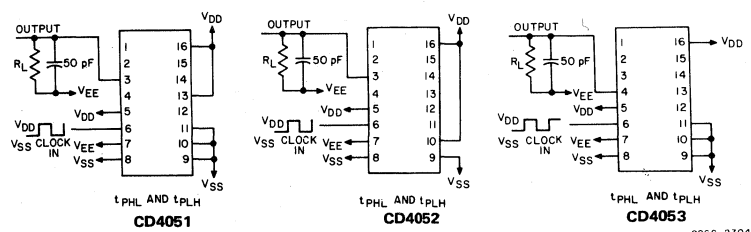


Fig.19 – Propagation delay – inhibit input to signal output.

TEST CIRCUITS (Cont'd)

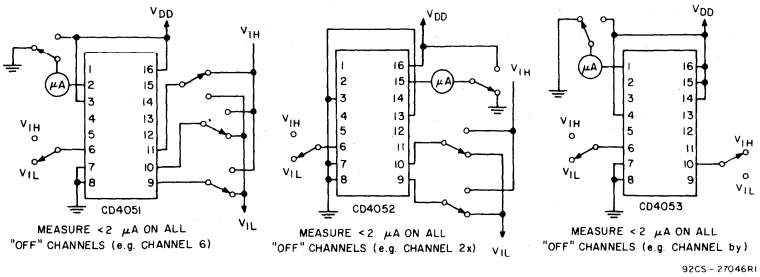


Fig. 20 – Input voltage.

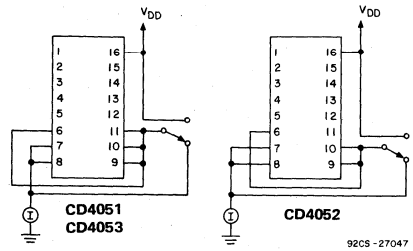


Fig.21 – Quiescent device current.

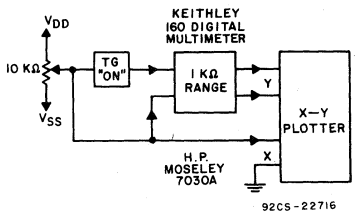
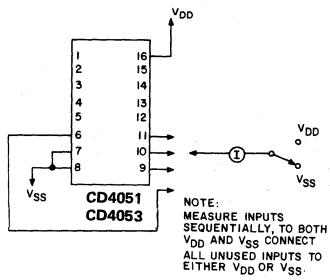


Fig.22 – Channel ON resistance measurement circuit.



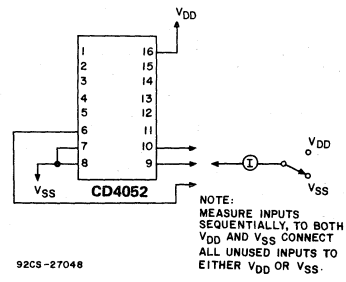


Fig. 23 – Input current.

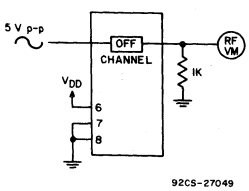
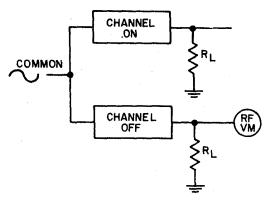


Fig.24 – Feedthrough (all types).



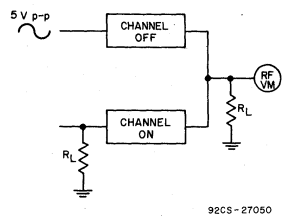


Fig.25 – Crosstalk between any two channels (all types).

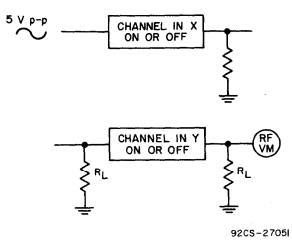


Fig.26 – Crosstalk between duals or triplets (CD4052B, CD4053B).

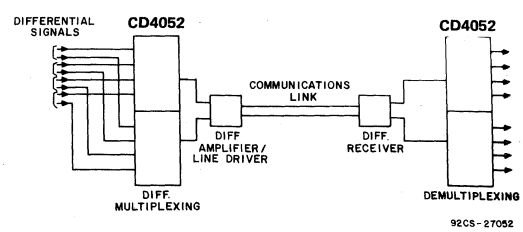


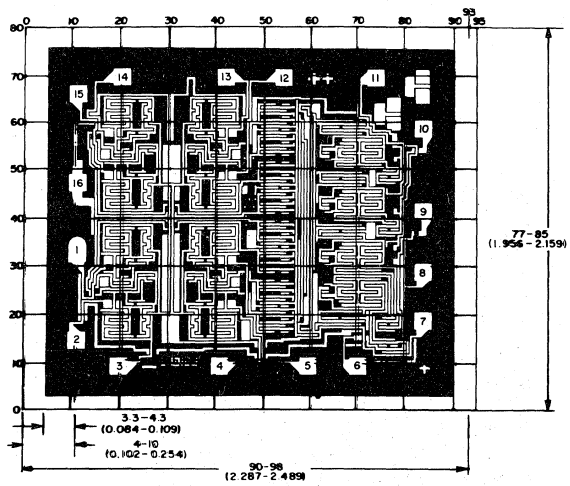
Fig.27 – Typical time-division application of the CD4052B.

SPECIAL CONSIDERATIONS

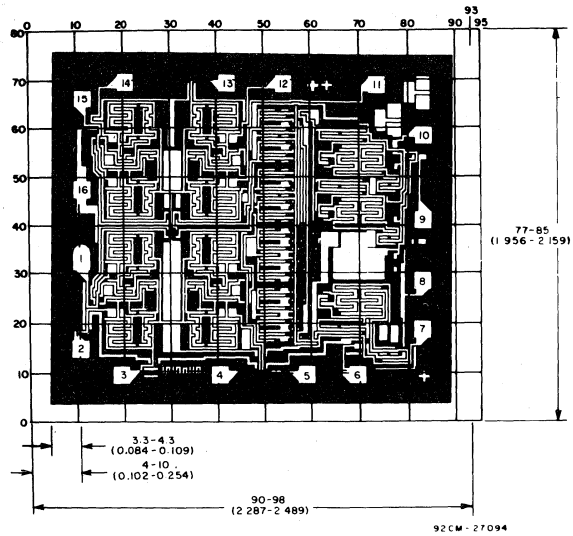
In applications where separate power sources are used to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load). This provision avoids permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from the CD4051B, CD4052B, or CD4053B.

When switching from one address to another, some of the ON periods of the channels of the multiplexers will overlap momentarily, which may be objectionable in certain applications. Also when a channel is turned ON or OFF by an address input, there is a momentary conductive path from the channel to V_{EE}, which will dump some charge from any capacitor connected to the input or output of the channel. The inhibit input turning ON a channel will similarly dump some charge to V_{EE}.

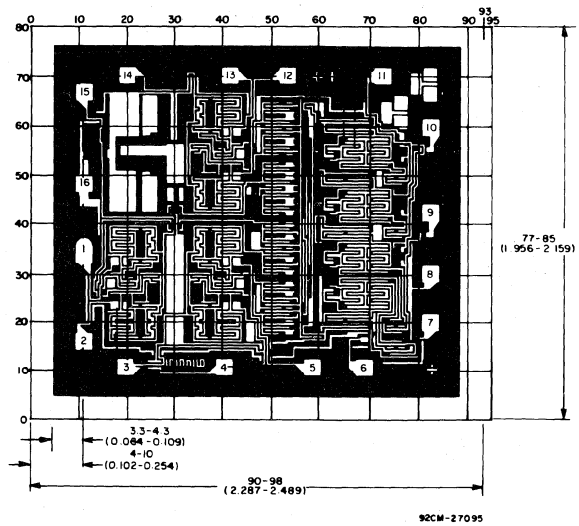
The amount of charge dumped is mostly a function of the signal level above V_{EE}. Typically, at V_{DD}-V_{EE} = 10 V, a 100 pF capacitor connected to the input or output of the channel will lose 3-4 % of its voltage at the moment the channel turns ON or OFF. This loss of voltage is essentially independent of the address or inhibit signal transition time, if the transition time is less than 1-2 μs. When the inhibit signal turns a channel OFF, there is no charge dumping to V_{EE}. Rather, there is a slight rise in the channel voltage level (65 mV typ.) due to capacitive coupling from inhibit input to channel input or output. Address inputs also couple some voltage steps onto the channel signal levels.



Dimensions and pad layout for CD4051BH. 92CM-27093



Dimensions and pad layout for CD4052BH.



Dimensions and pad layout for CD4053BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid Graduations are in Mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS Liquid-Crystal Display Drivers

High-Voltage Types (20-Volt Rating)

CD4054B – 4-Segment Display Driver
CD4055B – BCD to 7-Segment Decoder/Driver with "Display-Frequency" Output
CD4056B – BCD to 7-Segment Decoder/Driver with Strobed-Latch Function

The RCA CD4055B and CD4056B types are single-digit BCD-to-7-segment decoder/driver circuits that provide level-shifting functions on the chip. This feature permits the BCD input-signal swings (V_{DD} to V_{SS}) to be the same as or different from the 7-segment output-signal swings (V_{DD} to V_{EE}). For example, the BCD input-signal swings (V_{DD} to V_{SS}) may be as low as 0 to −3 V, whereas the output-display drive-signal swing (V_{DD} to V_{EE}) may be from 0 to −5 V. If V_{DD} to V_{EE} exceeds 15 V, V_{DD} to V_{SS} should be at least 4 V.

The 7-segment outputs are controlled by the DISPLAY-FREQUENCY (DF) input which causes the selected segment outputs to be low, high, or a square-wave output (for liquid-crystal displays). When the DF input is low the output segments will be high when selected by the BCD inputs. When the DF input is high, the output segments will be low when selected by the BCD inputs. When a square-wave is present at the DF input, the selected segments will have a square-wave output that is 180° out of phase with the DF input. Those segments which are not selected will have a square-wave output that is in phase with the input. DF square-wave repetition rates for liquid-crystal displays usually range from 30 Hz (well above flicker rate) to 200 Hz (well below the upper limit of the liquid-crystal frequency response). The CD4055B provides a level-shifted high-amplitude DF output which is required for driving the common electrode in liquid-crystal displays. The CD4056B provides a strobed-latch function at the BCD inputs. Decoding of all input combinations on the CD4055B and CD4056B provides displays of 0 to 9 as well as L, P, H, A, –, and a blank position. See page 8 for other letters.

The CD4054B provides level shifting similar to the CD4055B and CD4056B independently strobed latches, and common DF control on 4 signal lines. The CD4054B is intended to provide drive-signal compatibility with the CD4055B and CD4056B 7-segment decoder types for the decimal point, colon, polarity, and similar display lines. A level-shifted high-amplitude DF output can be obtained from any CD4054B output line by connecting the corresponding input and strobe lines to a low and high level, respectively. The CD4054B may also be utilized for logic-level "up conversion" or "down conversion". For example, input-signal swings (V_{DD} to V_{SS}) from +5 to 0 V can be converted to output-signal swings (V_{DD} to V_{EE}) of +5 to −5 V. The level-shifted function on all three types permits the use of different input- and output-signal swings. The input swings from a low level of V_{SS} to a high level of V_{DD} while the output swings from a low level of V_{EE} to the same high level of V_{DD}. Thus, the input and output swings can be selected independently of each other over a 3-to-18 V range. V_{SS} may be connected to V_{EE} when no level-shift function is required.

For the CD4054B and CD4056B, data are transferred from input to output by placing a high voltage level at the strobe input. A low voltage level at the strobe input latches the data input and the corresponding output segments remain selected (or non-selected) while the strobe is low.

Whenever the level-shifting function is required, the CD4055B can be used by itself to drive a liquid-crystal display (Fig.17 and Fig.19). The CD4056B, however, must be used together with a CD4054B to provide the common DF output (Fig.20). The capability of extending the voltage swing on the negative end (this voltage cannot be extended on the positive end) can be used to advantage in the setup of Fig.18. Fig.16 is common to all three types.

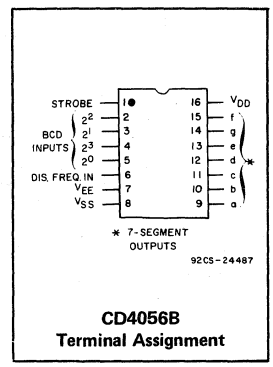
The CD4054B-, CD4055B-, and CD4056B-Series types are available in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

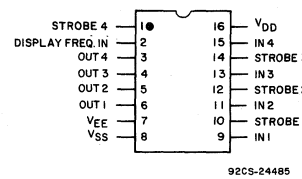
- **Operation of liquid crystals with COS/MOS circuits provides ultra-low-power displays**
- **Equivalent ac output drive for liquid-crystal displays – no external capacitor required**
- **Voltage doubling across display, e.g. $V_{DD} - V_{EE}$ = 18 V results in effective 36 V p-p drive across selected display segments**
- **Low- or high-output level dc drive for other types of displays**
- **On-chip logic-level conversion for different input- and output-level swings**
- **Full decoding of all input combinations: 0-9, L, H, P, A,–, and blank positions**
- **Strobed-latch function–CD4054B Series and CD4056B Series**
- **DISPLAY-FREQUENCY (DF) output for liquid-crystal common-line drive signal–CD4055B Series (CD4054B Series also: see introductory text)**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (over full package temperature range):**
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- **5-V, 10-V, and 15-V parametric ratings**

Applications

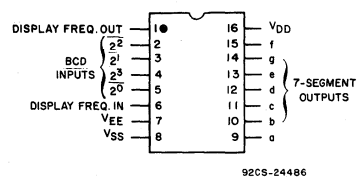
- **General-purpose displays**
- **Calculators and meters**
- **Wall and table clocks**
- **Industrial control panels**
- **Portable lab instruments**
- **Panel meters**
- **Auto dashboard displays**
- **Appliance control panels**



CD4056B Terminal Assignment



CD4054B Terminal Assignment



CD4055B Terminal Assignment

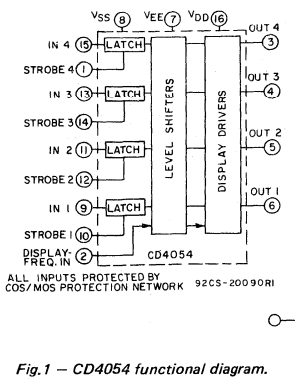


Fig.1 – CD4054 functional diagram.

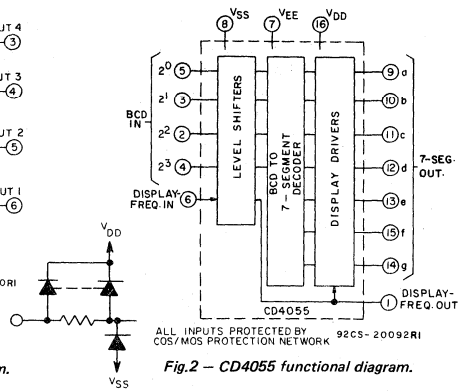


Fig.2 – CD4055 functional diagram.

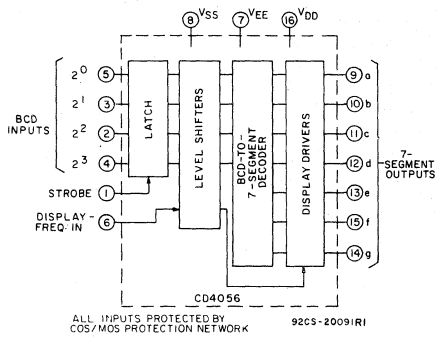


Fig.3 – CD4056 functional diagram.

TRUTH TABLE FOR CD4055B and CD4056B

INPUT CODE				OUTPUT STATE							DISPLAY CHARACTER
2^3	2^2	2^1	2^0	a	b	c	d	e	f	g	
0	0	0	0	1	1	1	1	1	1	0	0
0	0	0	1	0	1	1	0	0	0	0	1
0	0	1	0	1	1	0	1	1	0	1	2
0	0	1	1	1	1	1	1	0	0	1	3
0	1	0	0	0	1	1	0	0	1	1	4
0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	0	1	1	1	1	1	6
0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	1	1	1	1	0	1	1	9
1	0	1	0	0	0	0	1	1	1	0	—
1	0	1	1	0	1	1	0	1	1	1	H
1	1	0	0	1	1	0	0	1	1	1	L
1	1	0	1	1	1	1	0	1	1	1	⊐
1	1	1	0	0	0	0	0	0	0	1	—
1	1	1	1	0	0	0	0	0	0	0	BLANK

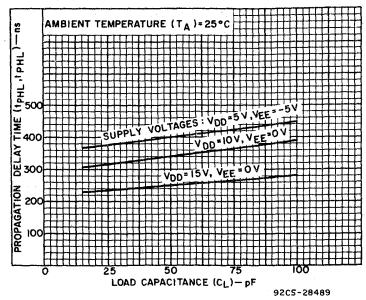


Fig.4 – Typical propagation delay time vs. load capacitance for CD4054B.

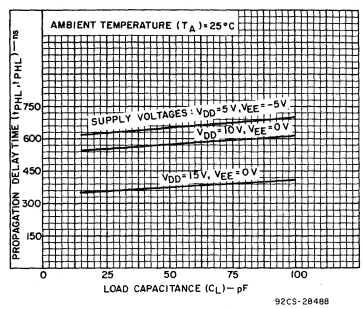


Fig.5 – Typical propagation delay time vs. load capacitance for CD4055 and CD4056B.

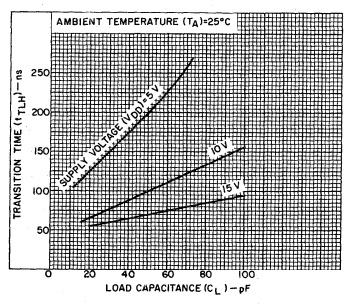


Fig.6 – Typical transition time vs. load capacitance.

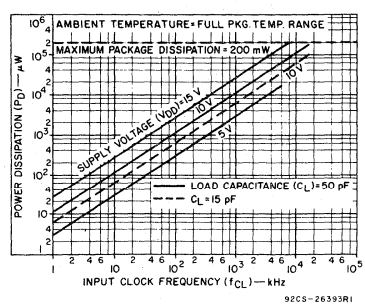


Fig.7 – Typical input clock frequency vs. power dissipation.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

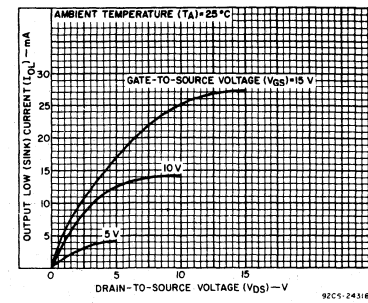


Fig.8 – Typical n-channel output low (sink) current characteristics.

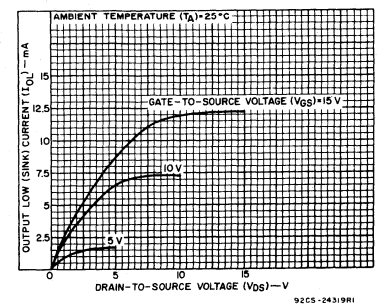


Fig.9 – Minimum n-channel output low (sink) current characteristics.

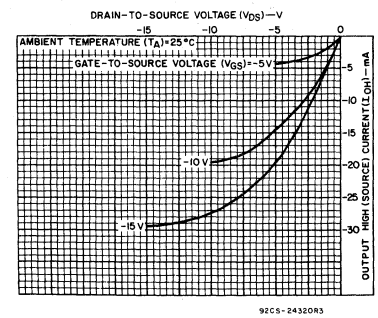


Fig.10 – Typical p-channel output high (source) current characteristics.

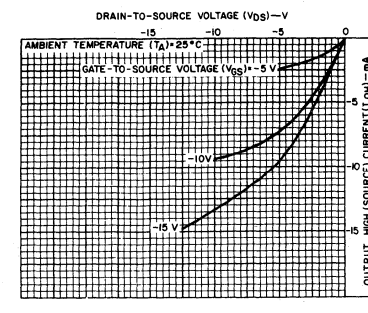


Fig.11 – Minimum p-channel output high (source) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	CONDITIONS V_{EE} (V)	V_{SS} (V)	V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS *Values at −55°,+25°,+125°C Apply to D,F,K,H Packages; Values at −40°,+25°,+85°C Apply to E Package* −55°	−40°	+85°	+125°	+25°C Min.	+25°C Typ.	+25°C Max.	Units
Quiescent Device Current, I_{DD} MAX.	−5	0			5	5		150	150	–	0.04	5	μA
	0	0			10	10		300	300	–	0.04	10	
	0	0			15	20		600	600	–	0.04	20	
	0	0			20	100		3000	3000	–	0.08	100	
Output Voltage: Low Level, V_{OL} MAX.	0	0		0,5	5	0.05				–	0	0.05	V
	0	0		0,10	10	0.05				–	0	0.05	
	0	0		0,15	15	0.05				–	0	0.05	
High Level, V_{OH} MIN.	0	0		0,5	5	4.95				4.95	5	–	
	0	0		0,10	10	9.95				9.95	10	–	
	0	0		0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} MAX.	−5	0	0.5, 4.5		5	1.5				–	–	1.5	V
	0	0	1,9		10	3				–	–	3	
	0	0	2,13		15	4				–	–	4	
Input High Voltage, V_{IH} MIN.	−5	0	0.5,4.5		5	3.5				3.5	–	–	
	0	0	1,9		10	7				7	–	–	
	0	0	2,13		15	11				11	–	–	
Output Low (Sink) Current, I_{OL}	−5	0	−4.5		5	1.6	1.5	1.1	0.9	1.3	2.6	–	mA
	0	0	0.5		10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	0	0	1.5		15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH}	−5	0	4.5		5	−0.6	−0.55	−0.35	−0.3	−0.45	−0.9	–	
	0	0	9.5		10	−0.6	−0.55	−0.35	−0.3	−0.45	−0.9	–	
	0	0	13.5		15	−1.9	−1.8	−1.2	−1.1	−1.5	−3	–	
Input Current, I_{IN}	0	0	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 50 pF, Input t_r,t_f = 20 ns, R_L = 200 kΩ

CHARACTERISTIC	CONDITIONS V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	LIMITS ALL PACKAGE TYPES CD4054 Typ.	CD4054 Max.	CD4055,CD4056 Typ.	CD4055,CD4056 Max.	UNITS
Propagation Delay Time, t_{PHL},t_{PLH} (Any Input to Any Output)	−5	0	5	400	800	650	1300	ns
	0	0	10	340	680	575	1150	
	0	0	15	250	500	375	750	
Transition Time, t_{THL},t_{TLH} (Any Output)	−5	0	5	100	200	100	200	ns
	0	0	10	100	200	100	200	
	0	0	15	75	150	75	150	
Minimum Data Setup Time, t_S*	−5	0	5	110	220	110	220	ns
	0	0	10	50	100	50	100	
			15	35	70	35	70	
Minimum Strobe Pulse Width, t_W*	−5	0	5	110	220	110	220	ns
	0	0	10	50	100	50	100	
	0	0	15	35	70	35	70	
Input Capacitance, C_{IN} (Any Input)	–	–	–	5	7.5	5	7.5	pF

* CD4054 and CD4056 only.

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C (Unless otherwise specified)

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply Voltage Range: (At T_A = Full Package Temperature Range)				3	18	V
Setup Time (t_s)●	−5	0	5	220	–	ns
	0	0	10	100	–	
	0	0	15	70	–	
Strobe Pulse Width (t_W)●	−5	0	5	220	–	ns
	0	0	10	100	–	
	0	0	15	70	–	

● For CD4054 and CD4056 only.

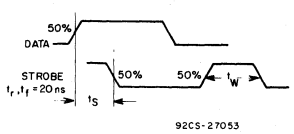
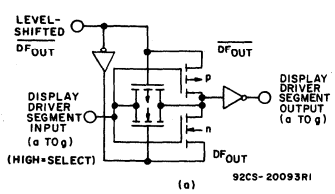


Fig. 15 – Data setup time and strobe pulse duration.



TEST CIRCUITS

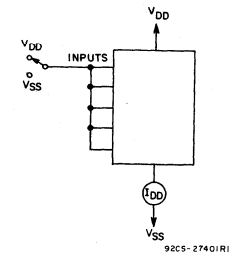


Fig. 12 – Quiescent-device current.

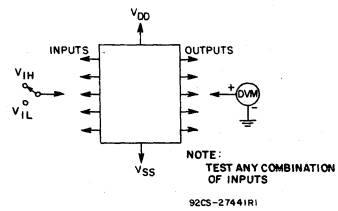


Fig. 13 – Input voltage.

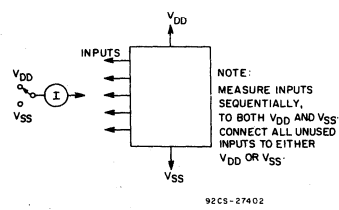


Fig. 14 – Input current.

APPLICATIONS

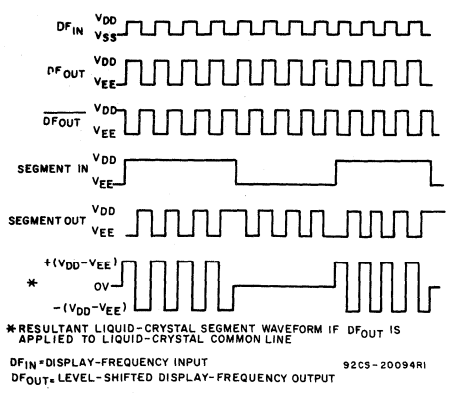


Fig. 16 – Display-driver circuit for one segment line and waveforms.

APPLICATIONS (Cont'd)

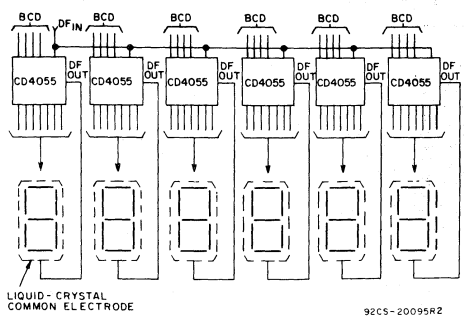


Fig.17 – Clock display: V_{DD} = 0 V, V_{SS} = –5 V, V_{EE} = –15 V, DF_{IN} = 30 Hz square wave.

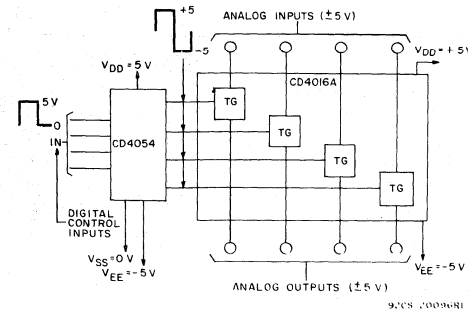


Fig.18 – Digital (0 to +5 V) to bidirectional analog control (+5 to –5 V) level shifter.

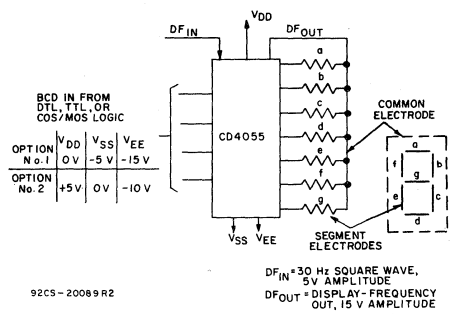


Fig.19 – Single-digit liquid-crystal display.

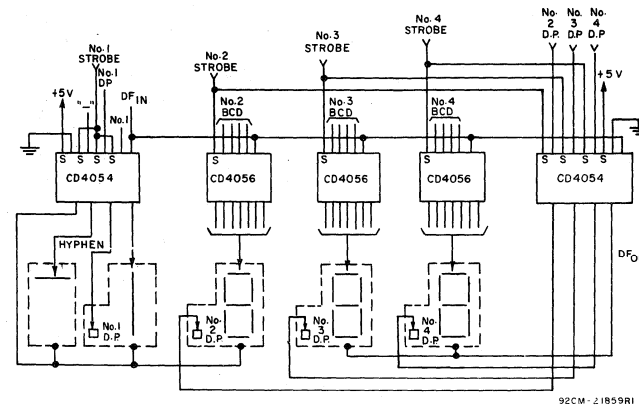


Fig.20 – Typical 3½-digit liquid-crystal display: V_{DD} = +5 V, V_{SS} = 0 V, V_{EE} = –10 V, DF_{IN} = 30 Hz square wave.

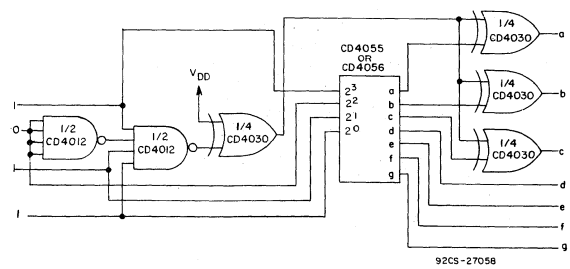
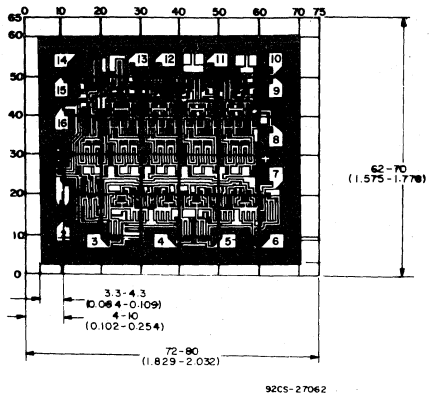


Fig.21 – Conversion of "H" display to "F" display.

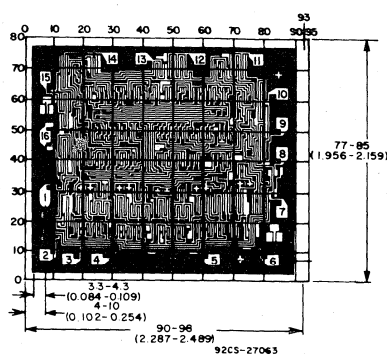
In addition to the letters L, H, P, and A (See the truth table), five other letters can be displayed through the use of simple logic circuits preceding and following the CD4055B or CD4056B devices. Fig.21 is an example of a circuit that converts an "H" display (code 1011) to an "F" display. One condition that must be met is that V_{EE}=V_{SS}. If V_{EE}≠V_{SS}, the CD4054B must be used to level shift in the appropriate places.

In a similar manner the letters C, E, J, and U can be displayed. These circuits can also be used to drive LED displays provided the exclusive-OR gates have sufficient output-current drive.

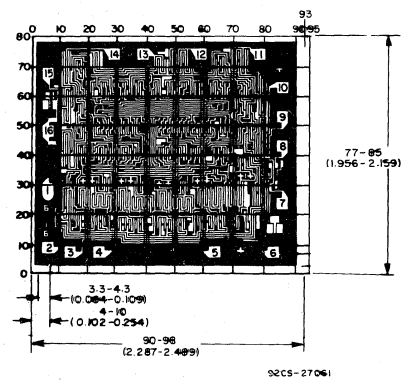
The letters B, D, G, I, O, and S may be represented by the codes for numbers 8, 0, 6, 1, 0, and 5, respectively, when there is preknowledge that only letters are to be displayed.



Dimensions and pad layout for CD4054BH.



Dimensions and pad layout for CD4055BH



Dimensions and pad layout for CD4056BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Preliminary Data

COS/MOS 14-Stage Ripple-Carry Binary Counter/Divider and Oscillator

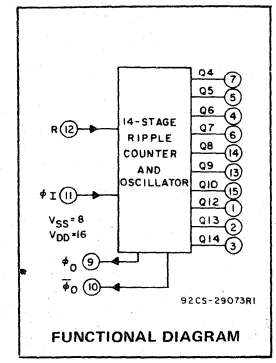
High-Voltage Types (20-Volt Rating)

The RCA-CD4060B consists of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. A RESET input is provided which resets the counter to the all-0's state and disables the oscillator. A high level on the RESET line accomplishes the reset function. All counter stages are master-slave flip-flops. The state of the counter is advanced one step in binary order on the negative transition of ϕ_1 (and ϕ_0). All inputs and outputs are fully buffered. Schmitt trigger action on the input pulses line permits unlimited input pulses rise and fall times.

The CD4060B-series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Medium-speed operation**
- **Common reset**
- **Fully static operation**
- **Buffered inputs and outputs**
- **100% tested for quiescent current at 20 V**
- **Standardized, symmetrical output characteristics**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for description of "B" Series CMOS Devices"**



FUNCTIONAL DIAGRAM

Oscillator Features:

- **All active components on chip**
- **RC or crystal oscillator configuration**

Applications

- **Control counters**
- **Timers**
- **Frequency dividers**
- **Time-delay circuits**

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . 0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . 0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A 40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A 55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . 55 to +125°C
PACKAGE TYPE E . . . . . 40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . 65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

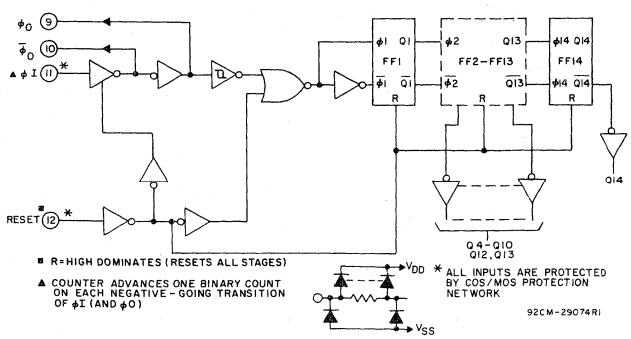


Fig.1 – Logic diagram.

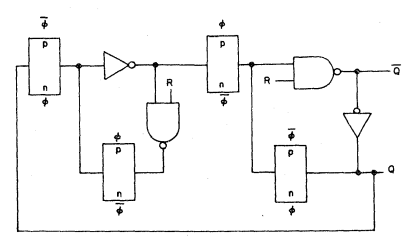
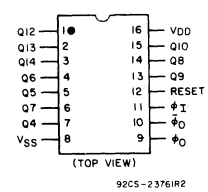


Fig.2 – Detail of typical flip-flop stage.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
									+25		
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

TERMINAL DIAGRAM



92CS-23761R2

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	TYPICAL VALUES	UNITS
Input-Pulse Operation				
Propagation Delay Time, ϕ_1 to Q4 Out; t_{PHL}, t_{PLH}		5	800	ns
		10	340	
		15	240	
Propagation Delay Time, Q_n to Q_{n+1}; t_{PHL}, t_{PLH}		5	200	ns
		10	85	
		15	60	
Transition Time, t_{THL}, t_{TLH}		5	100	ns
		10	50	
		15	40	
Min. Input-Pulse Width, t_W	f = 100 kHz	5	70	ns
		10	30	
		15	20	
Input-Pulse Rise & Fall Time, $t_{r\phi}$, $t_{f\phi}$		5	Unlimited	μs
		10		
		15		
Max. Input-Pulse Frequency, f_ϕ		5	7	MHz
		10	16	
		15	24	
Input Capacitance, C_I	Any Input		5	pF
Reset Operation				
Propagation Delay Time, t_{PHL}		5	300	ns
		10	140	
		15	100	
Minimum Reset Pulse Width, t_W		5	375	ns
		10	200	
		15	150	

COS/MOS 4-Bit Magnitude Comparator

High Voltage Types (20-Volt Rating)

The RCA-CD4063B is a 4-bit magnitude comparator designed for use in computer and logic applications that require the comparison of two 4-bit words. This logic circuit determines whether one 4-bit word (Binary or BCD) is "less than", "equal to", or "greater than" a second 4-bit word.

The CD4063B has eight comparing inputs (A3, B3, through A0, B0), three outputs (A < B, A = B, A > B) and three cascading inputs (A < B, A = B, A > B) that permit systems designers to expand the comparator function to 8, 12, 16 . . . 4N bits. When a single CD4063B is used, the cascading inputs are connected as follows: (A < B) = low, (A = B) = high, (A > B) = low.

For words longer than 4 bits, CD4063B devices may be cascaded by connecting the outputs of the less-significant comparator to the corresponding cascading inputs of the more-significant comparator. Cascading inputs (A < B, A = B, and A > B) on the least significant comparator are connected to a low, a high, and a low level, respectively.

The CD4063B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix). This device is pin-compatible with the standard 7485 TTL type.

RECOMMENDED OPERATING CONDITIONS
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

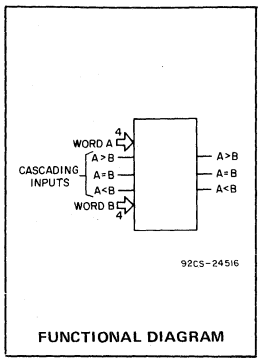
CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)	3	18	V

Features:

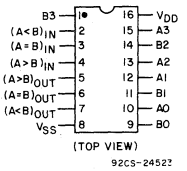
- Expansion to 8, 12, 16....4N bits by cascading units
- Medium-speed operation:
  compares two 4-bit words
  in 250 ns (typ.) at 10 V
- 100% tested for quiescent current at 20 V
- Standardized symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package temperature range)
  range) = 1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Servo motor controls
- Process controllers



FUNCTIONAL DIAGRAM



TERMINAL ASSIGNMENT

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
									+25		
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				–	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

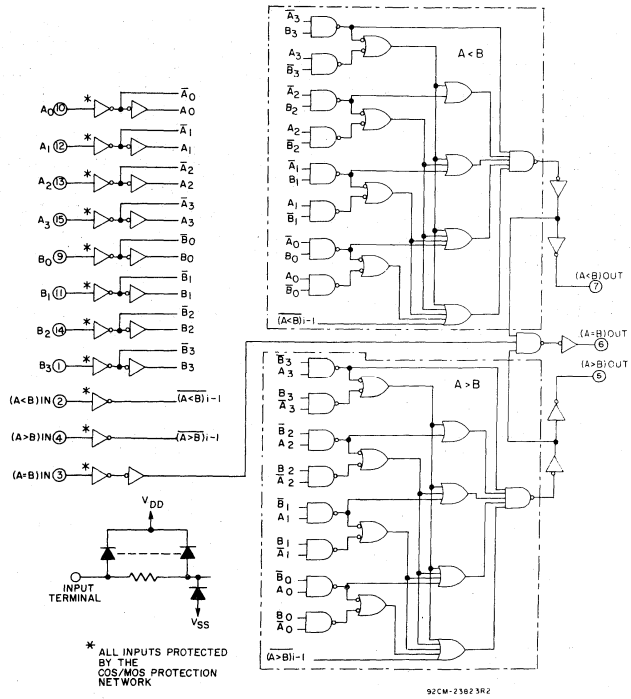


Fig. 1 – Logic diagram for CD4063B .

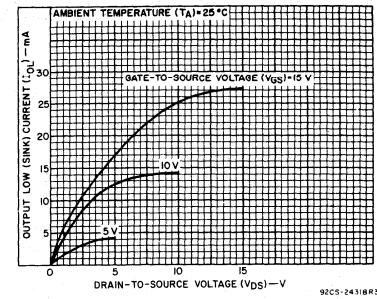


Fig. 2 – Typical output low (sink) current characteristics.

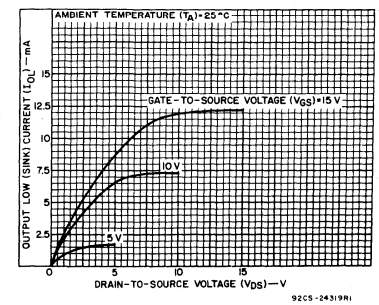


Fig. 3 – Minimum output low (sink) current characteristics.

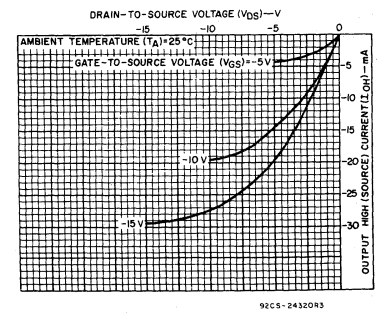


Fig. 4 – Typical output high (source) current characteristics.

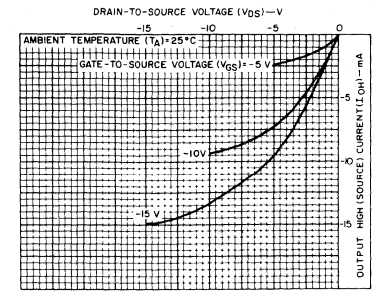


Fig. 5 – Minimum output high (source) current characteristics.

TRUTH TABLE

INPUTS							OUTPUTS		
COMPARING				CASCADING					
A3, B3	A2, B2	A1, B1	A0, B0	A < B	A = B	A > B	A < B	A = B	A > B
A3 > B3	X	X	X	X	X	X	0	0	1
A3 = B3	A2 > B2	X	X	X	X	X	0	0	1
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	0	1	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	1	0	0	1	0
A3 = B3	A2 = B2	A1 = B1	A0 = B0	1	0	0	1	0	0
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	1	0	0
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	1	0	0
A3 = B3	A2 < B2	X	X	X	X	X	1	0	0
A3 < B3	X	X	X	X	X	X	1	0	0

X = Don't Care Logic 1 ≡ High Level Logic 0 ≡ Low Level

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200kΩ

CHARACTERISTIC	TEST CONDITIONS	ALL TYPES LIMITS		UNITS
	V_{DD} Volts	Typ.	Max.	
Propagation Delay Time: Comparing Inputs to Outputs, t_{PHL}, t_{PLH}	5	625	1250	ns
	10	250	500	
	15	175	350	
Cascading Inputs to Outputs, t_{PHL}, t_{PLH}	5	500	1000	
	10	200	400	
	15	140	280	
Transition Time, t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Input Capacitance, C_{IN}	Any Input	5	7.5	pF

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

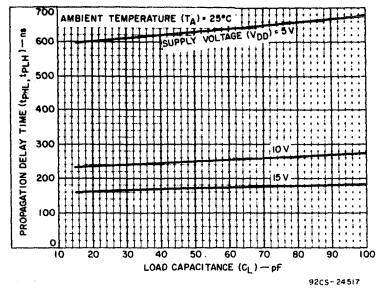


Fig. 6—Typical propagation delay time vs. load capacitance.

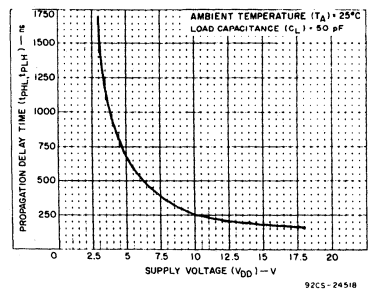


Fig. 7—Typical propagation delay time vs. supply voltage ("comparing inputs" to outputs).

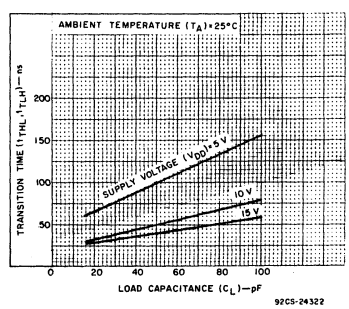


Fig. 8—Typical transition time vs. load capacitance.

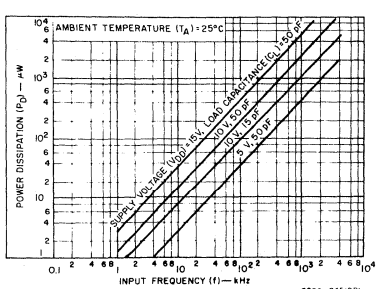


Fig. 9 — Typical power dissipation vs. frequency (see Fig. 11 — dynamic power dissipation test circuit).

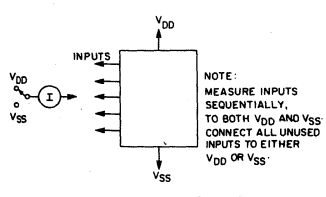


Fig. 10 — Input current test circuit.

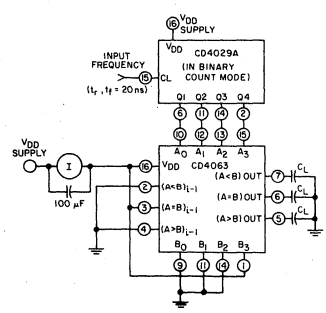


Fig. 11—Dynamic power dissipation test circuit

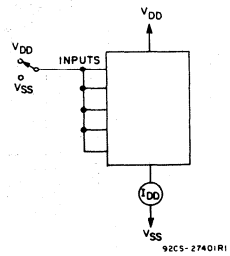


Fig. 12—Quiescent-device-current test circuit.

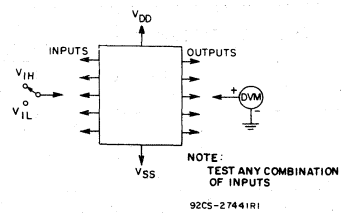
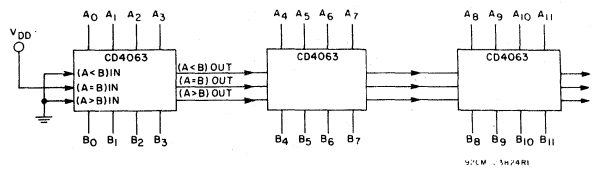


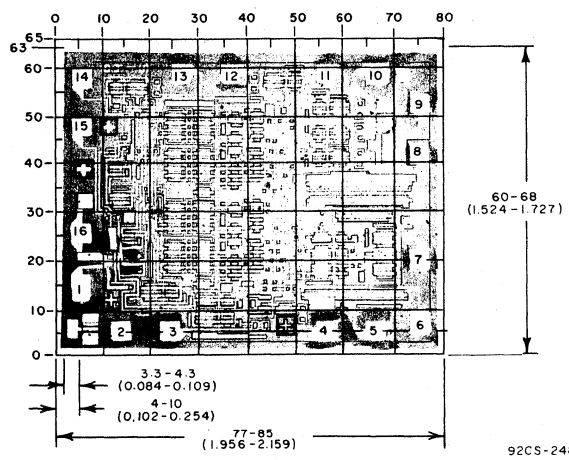
Fig. 13 – Input-voltage test circuit.



$t_{P\ TOTAL} = t_P\left(\frac{COMPARE}{INPUTS}\right) + 2 \times t_P\left(\frac{CASCADE}{INPUTS}\right)$, AT $V_{DD} = 10V$
(3 STAGES)

$= 250 + (2 \times 200) = 650$ ns (TYP.)

Fig. 14—Typical speed characteristics of a 12-bit comparator.



Dimensions and pad layout for CD4063BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

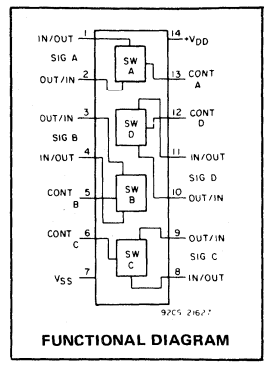
CD4066B Types

COS/MOS Quad Bilateral Switch

Preliminary Data

For Transmission or Multiplexing of Analog or Digital Signals

High-Voltage Types (20-Volt Rating)



FUNCTIONAL DIAGRAM

RCA-CD4066B is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with RCA-CD4016B, but exhibits a much lower ON resistance. In addition, the ON resistance is relatively constant over the full input-signal range.

The CD4066B consists of four independent bilateral switches. A single control signal is required per switch. Both the p and the n device in a given switch are biased ON or OFF simultaneously by the control signal. As shown in Fig.1, the well of the n-channel device on each switch is either tied to the input when the switch is ON or to V_{SS} when the switch is OFF. This configuration eliminates the variation of the switch-transistor threshold voltage with input signal, and thus keeps the ON resistance low over the full operating-signal range.

The advantages over single-channel switches include peak input-signal voltage swings equal to the full supply voltage, and more constant ON impedance over the input-signal range. For sample-and-hold applications, however, the CD4016B is recommended.

The CD4066B is available in 14-lead ceramic dual-in-line packages (D and F suffixes), 14-lead plastic dual-in-line packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **15-V digital or ± 7.5-V peak-to-peak switching**
- **80 Ω typical ON resistance for 15-V operation**
- **Switch ON resistance matched to within 5 Ω over 15-V signal-input range**
- **ON resistance flat over full peak-to-peak signal range**
- **High ON/OFF output-voltage ratio: 65 dB typ. @ f_{is} = 10 kHz, R_L = 10 kΩ**
- **High degree of linearity: <0.5% distortion typ. @ f_{is} = 1 kHz, V_{is} = 5 Vp-p, $V_{DD} - V_{SS} \geq 10$ V, R_L = 10 kΩ**
- **Extremely low OFF switch leakage resulting in very low offset current and high effective OFF resistance: 10 pA typ. @ $V_{DD} - V_{SS}$ = 10 V, T_A = 25°C**
- **Extremely high control input impedance (control circuit isolated from signal circuit): 10^{12} Ω typ.**
- **Low crosstalk between switches: –50 dB typ. @ f_{is} = 0.9 MHz, R_L = 1 kΩ**
- **Matched control-input to signal-output capacitance: Reduces output signal transients**
- **Frequency response, switch ON = 40 MHz (typ.)**
- **100% tested for quiescent current at 20 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No.13A, "Standard Specifications for Description of "B" Series CMOS Devices"**

Applications:

- **Analog signal switching/multiplexing**
  Signal gating — Modulator
  Squelch control — Demodulator
  Chopper — Commutating switch
- **Digital signal switching/Multiplexing**
- **Transmission-gate logic implementation**
- **Analog-to-digital & digital-to-analog conversion**
- **Digital control of frequency, impedance, phase, and analog-signal gain**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . –0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = –40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
PACKAGE TYPE E . . . . . –40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

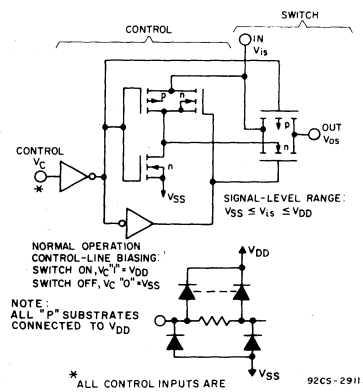


Fig.1 – Schematic diagram of 1 of 4 identical switches and its associated control circuitry.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

ELECTRICAL CHARACTERISTICS at T_A = 25°C

Characteristic	Test Conditions *All Voltage Values are in Volts*			Typical Values	Unit
			V_{DD} (V)		
Quiescent Device Current, I_{DD} max (All switches ON or all Switches OFF)			5	0.01	μA
			10	0.01	
			15	0.01	
			20	0.02	
Signal Inputs (V_{is}) and Outputs (V_{os})					
ON Resistance, R_{ON}	V_C= V_{DD}	V_{SS}	V_{is}	80	Ω
	R_L = 10 kΩ●				
	+7.5	−7.5	−7.5 to +7.5		
	+15	0	0 to +15		
	+5	−5	−5 to +5	120	
	+10	0	0 to +10		
	+2.5	−2.5	−25 to +2.5	250	
	−5	0	0 to +5		
ΔON Resistance Between Any 2 of 4 Switches ΔR_{ON}	R_L = 10 kΩ●			5	Ω
	+7.5 or +15	−7.5 or 0	+7.5 to −7.5		
			+15 to 0		
	+5 or +10	−5 or 0	+5 to −5	10	
			+10 to 0		
	+2.5 or +5	−2.5 or 0	−2.5 to +2.5	25	
			0 to +5		
Sine Wave Response (Distortion)	+5	−5	5V p-p▲	0.4	%
	R_L = 10 kΩ, f_{is} = 1 kHz				
Frequency Response Switch ON (Sine-Wave Input)	+5	−5	5 p-p	40	MHz
	R_L = 1 kΩ, $20\log_{10}\frac{V_{os}}{V_{is}}$ = −3 dB				

● For all test conditions.
▲ Symmetrical about 0 volts.

ELECTRICAL CHARACTERISTICS (Cont'd)

Characteristic	Test Conditions *All Voltage Values are in Volts*	V_{DD} (V)	Typical Values	Unit
Feedthrough Switch OFF	$V_{CC} = V_{DD} = +5$ $V_{SS} = -5$ $R_L = 1\ k\Omega$ $20\log_{10}\frac{V_{os}}{V_{is}} = -50$ dB	−5 p-p	1.25	MHz
Input or Output Leakage Current Switch OFF (Effective OFF Resistance)	V_{DD} / $V_C = V_{SS}$			
	+7.5 / −7.5	±7.5	±0.1	nA
	+5 / −5	±5	±0.1	
Crosstalk Between Any 2 of 4 Switches (f = −50 dB)	$V_C(A) = V_{DD} = +5$ $V_C(B) = V_{SS} = -5$ $V_{is}(A) = 5$ p-p $R_L = 1\ k\Omega$ $20\log_{10}\frac{V_{os}(B)}{V_{is}(A)} = -50$ dB		0.9	MHz
Propagation Delay (Signal Input to Signal Output) t_{pd}	$V_C = V_{DD}$ $V_{SS} = GND$ $C_L = 50$ pF $V_{is} = 10$ Sq.Wave $t_r, t_f = 20$ ns	5	40	ns
		10	20	
		15	15	
Capacitance: Input, C_{is}	$V_{DD} = +5$ $V_{CC} = V_{SS} = -5$		8	pF
Output, C_{os}			8	
Feedthrough, C_{ios}			0.5	
Control (V_C)				
Switch Threshold Voltage, V_{TH}	$I_{is} = 10\ \mu A$	5	2.25	V
		10	4.5	
		15	6.75	
Input Current, I_{IN} Max.	$V_{is} \leqslant V_{DD}$ $V_{DD} - V_{SS} = 18$ $V_{CC} \leqslant V_{DD} - V_{SS}$	18	$\pm 10^{-5}$	μA
Crosstalk (Control Input to Signal Output)	$V_C = 10$ (Sq.Wave) $t_r, t_f = 20$ ns $R_L = 10\ k\Omega$	10	50	mV
Turn-On Propagation Delay, t_p dc	$V_{DD} - V_{SS} = 10$ $t_r, t_f = 20$ ns $C_L = 50$ pF $R_L = 1\ k\Omega$	5	35	ns
		10	20	
		15	15	
Maximum Allowable Control Input Repetition Rate	$V_{DD} = 10$ $V_{SS} = GND$ $R_L = 1\ k\Omega$ $C_L = 50$ pF $V_{CC} = 10$ (Sq. Wave) $t_r, t_f = 20$ ns		10	MHz
Input Capacitance, C_{IN}			5	μF

COS/MOS Analog Multiplexers/Demultiplexers

High-Voltage Types (20-Volt Rating)

CD4067B – Single 16-Channel Multiplexer/Demultiplexer
CD4097B – Differential 8-Channel Multiplexer/Demultiplexer

The RCA-CD4067B and CD4097B COS/MOS analog multiplexers/demultiplexers* are digitally controlled analog switches having low ON impedance, low OFF leakage current, and internal address decoding. In addition, the ON resistance is relatively constant over the full input-signal range.

The CD4067B is a 16-channel multiplexer with four binary control inputs, A,B,C,D, and an inhibit input, arranged so that any combination of the inputs selects one switch.

The CD4097B is a differential 8-channel multiplexer having three binary control inputs A, B, C, and an inhibit input. The inputs permit selection of one of eight pairs of switches.

A logic "1" present at the inhibit input turns all channels off.

The CD4067 and CD4097 are supplied in 24-lead dual-in-line white ceramic packages (D suffix), 24-lead ceramic flat-packs (K suffix), 24-lead dual-in-line frit-seal ceramic packages (F suffix), 24-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

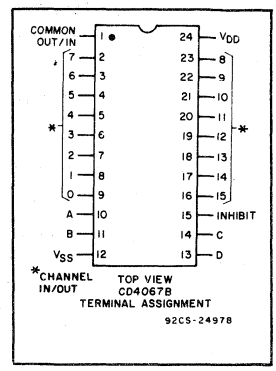
*When these devices are used as demultiplexers, the channel in/out terminals are the outputs and the common out/in terminals are the inputs.

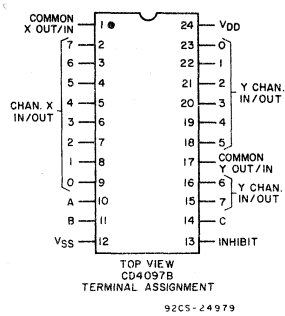
Features:

- **Low ON resistance: 125 Ω (typ.) over 15 V_{p-p} signal-input range for $V_{DD}-V_{SS}=15$ V**
- **High OFF resistance: channel leakage of ±10 pA (typ.) @ $V_{DD}-V_{SS}=10$ V**
- **Matched switch characteristics: $R_{ON}=5$ Ω (typ.) for $V_{DD}-V_{SS}=15$ V**
- **Very low quiescent power dissipation under all digital-control input and supply conditions: 0.2 μW (typ.) @ $V_{DD}-V_{SS}=10$ V**
- **Binary address decoding on chip**
- **5-V, 10-V, and 15-V parametric ratings**
- **100% tested for quiescent current at 20 V**
- **Standardized symmetrical output characteristics**
- **Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

- **Analog and digital multiplexing and demultiplexing**
- **A/D and D/A conversion**
- **Signal gating**





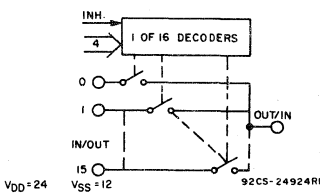


Fig. 1 – CD4067 functional diagram.

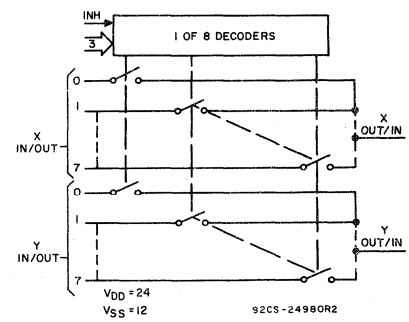


Fig. 2–CD4097 functional diagram.

Recommended Operating Conditions at $T_A = 25°C$ (Unless Otherwise Specified)

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges. Values shown apply to all types except as noted.

Characteristic	Min.	Max.	Units
Supply-Voltage Range (T_A=Full Package-Temp. Range)	3	18	V
Multiplexer Switch Input Current Capability	–	25	mA
Output Load Resistance	100	–	Ω

NOTE:
In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R_{ON} values shown in ELECTRICAL CHARACTERISTICS CHART). No V_{DD} current will flow through R_L if the switch current flows into terminal 1 on the CD4067; terminals 1 and 17 on the CD4097.

CD4067 TRUTH TABLE

A	B	C	D	Inh	Selected Channel
X	X	X	X	1	None
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15

CD4097 TRUTH TABLE

A	B	C	Inh	Selected Channel
X	X	X	1	None
0	0	0	0	0X, 0Y
1	0	0	0	1X, 1Y
0	1	0	0	2X, 2Y
1	1	0	0	3X, 3Y
0	0	1	0	4X, 4Y
1	0	1	0	5X, 5Y
0	1	1	0	6X, 6Y
1	1	1	0	7X, 7Y

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS at Indicated Temperature (°C) Values at −55,+25,+125,apply to D,K,H pkg Values at −40,+25,+85,apply to E pkg							Units
	V_{is} (V)	V_{SS} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
SIGNAL INPUTS (V_{is}) AND OUTPUTS (V_{OS})											
Quiescent Device Current, I_{DD} Max.			5	5	5	150	150	–	0.04	5	μA
			10	10	10	300	300	–	0.04	10	
			15	20	20	600	600	–	0.04	20	
			20	100	100	3000	3000	–	0.08	100	
ON Resistance $V_{SS} \leq V_{is} \leq V_{DD}$ R_{ON} Max.		0	5	2000	2100	3200	3500	–	470	2500	Ω
		0	10	310	330	520	580	–	180	400	
		0	15	220	230	360	400	–	125	280	
ΔON Resistance (Between Any Two Channels) ΔR_{ON}		0	5	–	–	–	–	–	10	–	Ω
		0	10	–	–	–	–	–	10	–	
		0	15	–	–	–	–	–	5	–	
OFF Channel Leakage Current: Any Channel OFF Max.		0	10	±200*				–	±0.1	±200*	nA
		0	15	±500*				–	±0.1	±200*	
		0	20	±1000*				–	±0.1	±200*	
All Channels OFF (Common OUT/IN) Max.		0	10	±200*				–	±0.1	±200*	
		0	15	±500*				–	±0.1	±200*	
		0	20	±1000*				–	±0.1	±200*	
Capacitance: Input, C_{is}		–5	5	–	–	–	–	–	5	–	pF
Output, C_{os} CD4067				–	–	–	–	–	55	–	
CD4097				–	–	–	–	–	35		
Feedthrough, C_{ios}				–	–	–	–	–	0.2		
Propagation Delay Time (Signal Input to Output	10 V	R_L=10 KΩ C_L=50 pF t_r, t_f=20 ns	5	–	–	–	–	–	30	–	ns
			10	–	–	–	–	–	15	–	
			15	–	–	–	–	–	11	–	
Input Low Voltage, V_{IL} Max.	=V_{DD} thru 1 KΩ	R_L=1 KΩ to V_{SS} I_{IS}<2 μA on all OFF Channels	5	1.5				–	–	1.5	V
			10	3				–	–	3	
			15	4				–	–	4	
Input High Voltage, V_{IH} Min.			5	3.5				3.5	–	–	
			10	7				7	–	–	
			15	11				11	–	–	

Determined by minimum feasible leakage measurement for automatic testing.

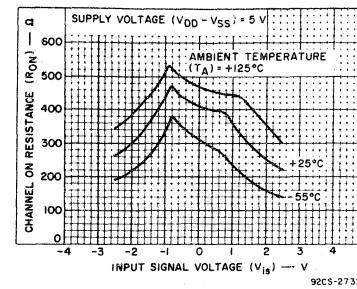


Fig. 3—Typical ON resistance vs. input signal voltage (all types).

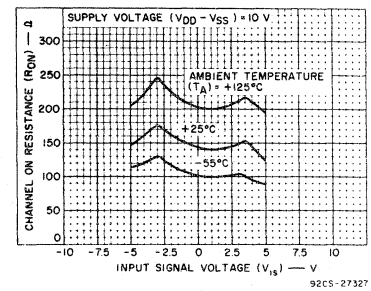


Fig. 4—Typical ON resistance vs. input signal voltage (all types).

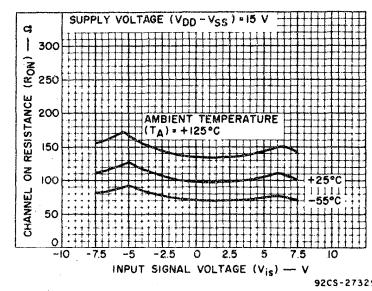


Fig. 5—Typical ON resistance vs. input signal voltage (all types).

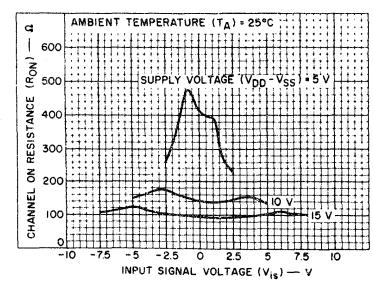


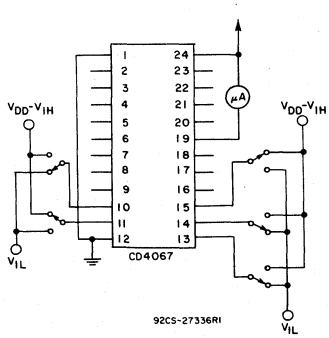
Fig. 6—Typical ON resistance vs. input signal voltage (all types).

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	CONDITIONS			LIMITS at Indicated Temperature (°C) Values at −55,+25,+125,apply to D,K,H pkg Values at −40,+25,+85,apply to E pkg							Units
	V_{is} (V)	V_{SS} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
CONTROL (ADDRESS or INHIBIT) V_C											
Input Current, I_{IN} Max.	V_{IN} = 0, 18 V		18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA
Propagation Delay Time: Address or Inhibit-to-Signal OUT (Channel turning ON)	R_L=10 KΩ,C_L= 50 pF, t_r,t_f=20 ns	0	5	–	–	–	–	–	325	650	ns
		0	10	–	–	–	–	–	135	270	
		0	15	–	–	–	–	–	95	190	
Address or Inhibit-to-Signal OUT (Channel turning OFF)	R_L=300 Ω,C_L= 50 pF, t_r,t_f=20 ns	0	5	–	–	–	–	–	220	440	ns
		0	10	–	–	–	–	–	90	180	
		0	15	–	–	–	–	–	65	130	
Input Capacitance, C_{IN}	Any Address or Inhibit Input			–	–	–	–	–	5	7.5	pF

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C



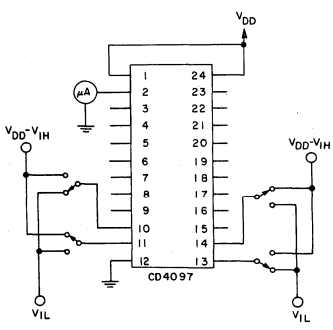


Fig. 8—Input voltage—measure <2 μA on all OFF channels (e.g., channel 12).

TEST CIRCUITS

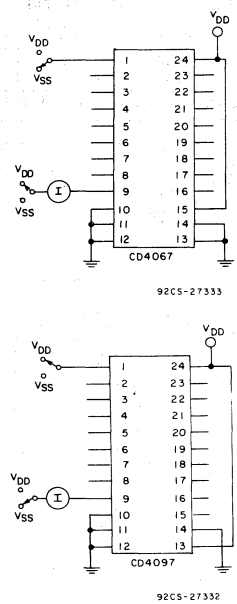


Fig. 7—OFF channel leakage current—any channel OFF.

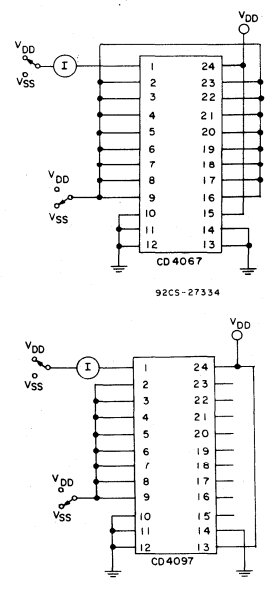


Fig. 9—OFF channel leakage current—all channels OFF.

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	TEST CONDITIONS V_{is} (V)	V_{DD} (V)	R_L (KΩ)			TYPICAL VALUES	UNITS
Frequency Response Channel ON (Sine Wave Input)	5●	10	1	V_{os} at Common OUT/IN	CD4067	14	MHz
	$20 \log \frac{V_{os}}{V_{is}} = -3$ dB				CD4097	20	
				V_{os} at Any Channel		60	
Sine Wave Response (Distortion)	2●	5	10			0.3	%
	3●	10				0.2	
	5●	15				0.12	
	f_{is} = 1 kHz						
Feedthrough (All Channels OFF)	5●	10	1	V_{os} at Common OUT/IN	CD4067	20	MHz
	$20 \log \frac{V_{os}}{V_{is}} = -40$ dB				CD4097	12	
				V_{os} at Any Channel		8	
Signal Crosstalk (Frequency at −40 dB)	5●	10	1	Between Any 2 Channels▲		1	MHz
	$20 \log \frac{V_{os}}{V_{is}} = -40$ dB			Between Sections CD4097 Only	Measured on Common	10	
					Measured on Any Channel	18	
Address-or-Inhibit-to-Signal Crosstalk	—	10	10*			75	mV (Peak)
	V_{SS}=0, t_r,t_f=20 ns, $V_C = V_{DD} - V_{SS}$ (Square Wave)						

● Peak-to-peak voltage symmetrical about $\frac{V_{DD} - V_{SS}}{2}$.

▲ Worst case.

* Both ends of channel.

TEST CIRCUITS (Cont'd)

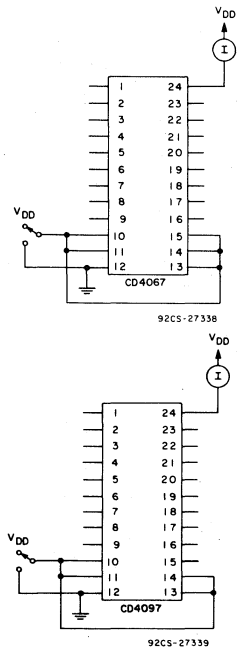
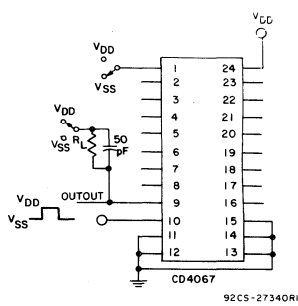


Fig. 10— Quiescent device current.



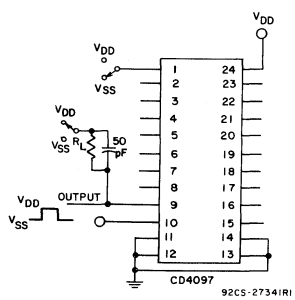
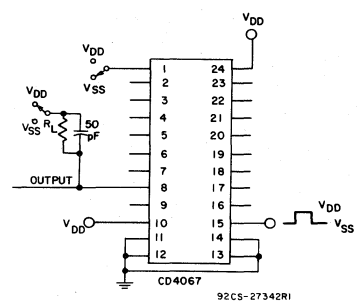


Fig. 11— Turn-on and turn-off propagation delay—address select input to signal output (e.g. measured on channel 0).



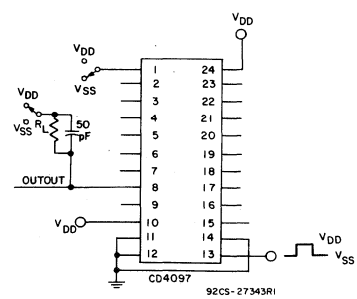


Fig. 12— Turn-on and turn-off propagation delay—inhibit input to signal output (e.g. measured on channel 1).

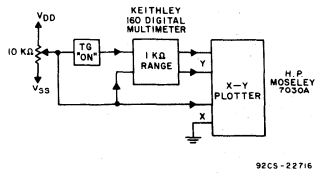


Fig. 13—Channel ON resistance measurement circuit.

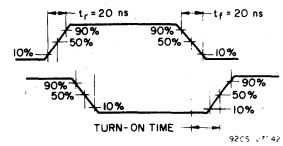


Fig. 14—Propagation delay waveform channel being turned ON (R_L=10 KΩ, C_L= 50 pF).

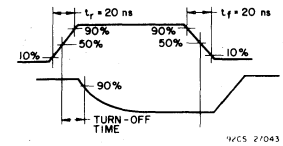


Fig. 15—Propagation delay waveform, channel being turned OFF (R_L = 300 Ω, C_L = 50 pF).

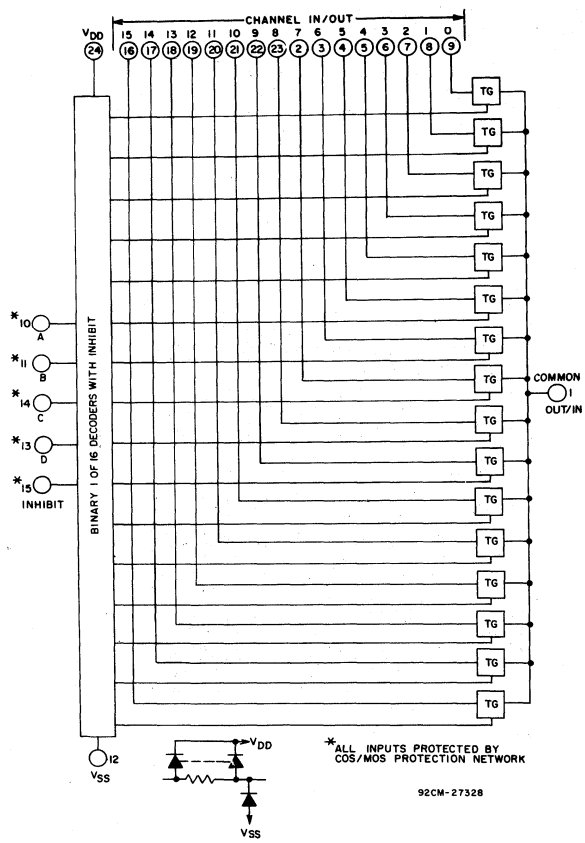


Fig. 16—CD4067 logic diagram.

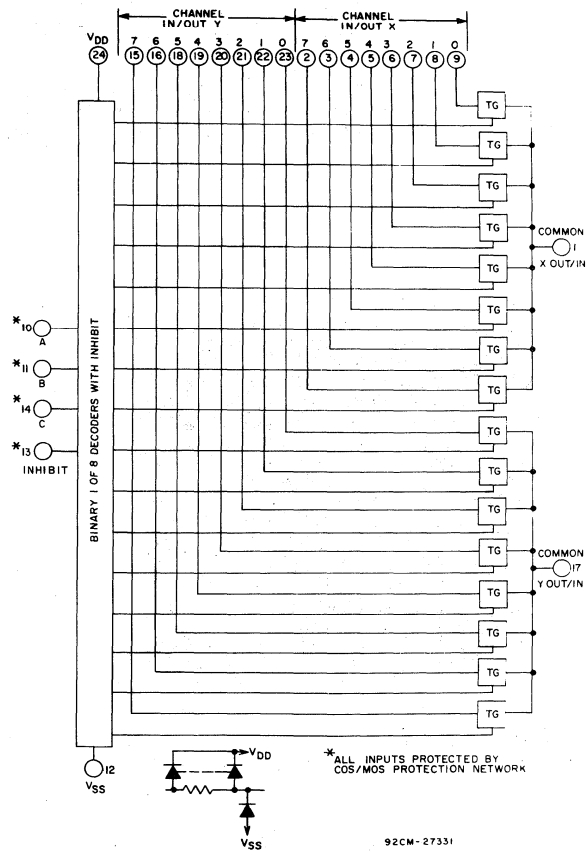


Fig. 17—CD4097 logic diagram.

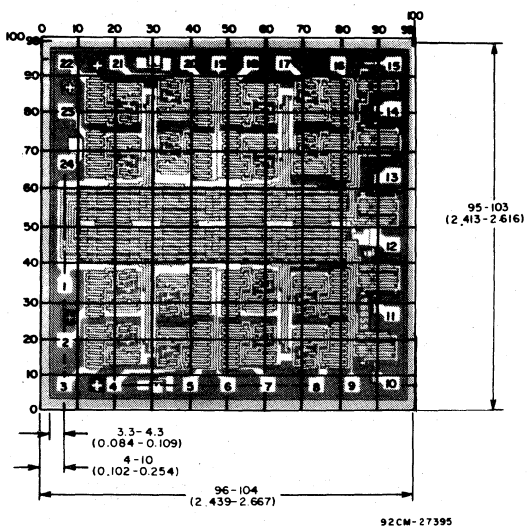
SPECIAL CONSIDERATIONS

In applications where separate power sources are used to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L=effective external load). This provision avoids permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from the CD4067B or CD4097B.

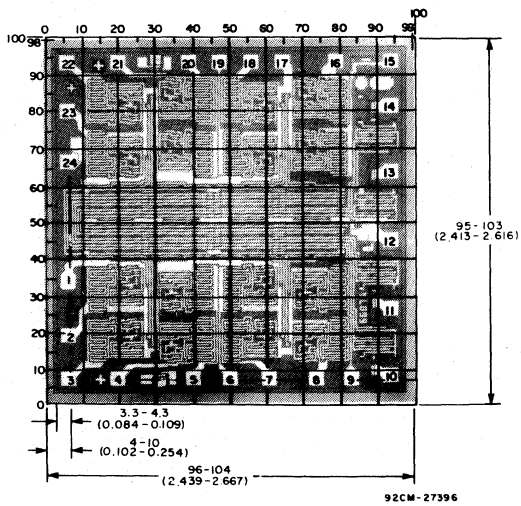
When switching from one address to another, some of the ON periods of the channels of the multiplexers will overlap momentarily, which may be objectionable in certain applications. Also when a channel is turned on or off by an address input, there is a momentary conductive path from the channel to V_{SS}, which will dump some charge from any capacitor connected to the input or output of the channel. The inhibit input turning on a channel will similarly dump some charge to V_{SS}.

The amount of charge dumped is mostly a function of the signal level above V_{SS}. Typically, at $V_{DD}-V_{SS}$=10 V, a 100-pF capacitor connected to the input or output of the channel will lose 3-4% of its voltage at the moment the channel turns on or off. This loss of voltage is essentially independent of the address or inhibit signal transition time, if the transition time is less than 1-2 μs. When the inhibit signal turns a channel off, there is no charge dumping to V_{SS}. Rather, there is a slight rise in the channel voltage level (65 mV typ.) due to capacitive coupling from inhibit input to channel input or output. Address inputs also couple some voltage steps onto the channel signal levels.

In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R_{ON} values shown in ELECTRICAL CHARACTERISTICS CHART). No V_{DD} current will flow through R_L if the switch current flows into terminal 1 on the CD4067B, terminals 1 and 17 on the CD4097B.



Dimensions and pad layout for CD4067BH.



Dimensions and pad layout for CD4097BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

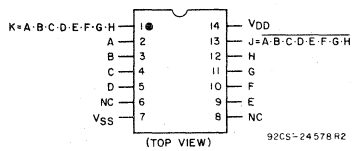
The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS 8-Input NAND/AND Gate

High-Voltage Types (20-Volt Rating)

The RCA-CD4068B NAND/AND gate provides the system designer with direct implementation of the positive-logic 8-input NAND and AND functions and supplements the existing family of COS/MOS gates.

The CD4068B types are supplied in 14-lead dual-in-line ceramic packages (D and F suffixes); 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

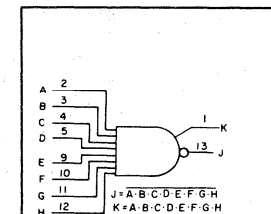


NC = NO CONNECTION

TERMINAL ASSIGNMENT

Features:

- Medium-Speed Operation: t_{PHL}, t_{PLH} = 75 ns (typ.) at V_{DD} = 10 V
- Buffered inputs and output
- 5-V, 10-V, and 15-V parametric ratings
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range): 1 V at V_{DD} = 5 V; 2 V at V_{DD} = 10 V; 2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"



FUNCTIONAL DIAGRAM

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	Min.	Max.	Units
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

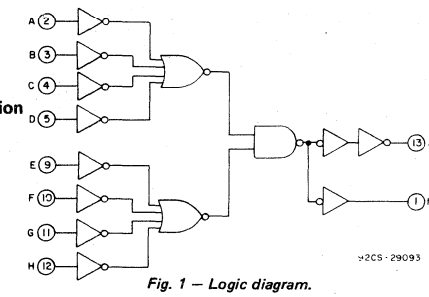


Fig. 1 — Logic diagram.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
									+25		
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

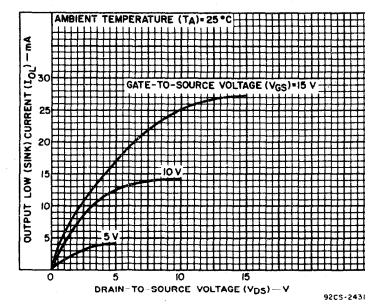


Fig. 2 — Typical output low (sink) current characteristics.

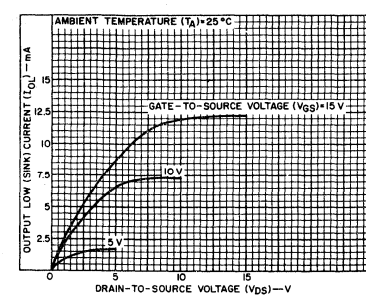


Fig. 3 — Minimum output low (sink) current characteristics.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200kΩ

CHARACTERISTIC	TEST CONDITIONS		ALL TYPES LIMITS		UNITS
		V_{DD} VOLTS	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH}		5	150	300	ns
		10	75	150	
		15	55	110	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input		5	7.5	pF

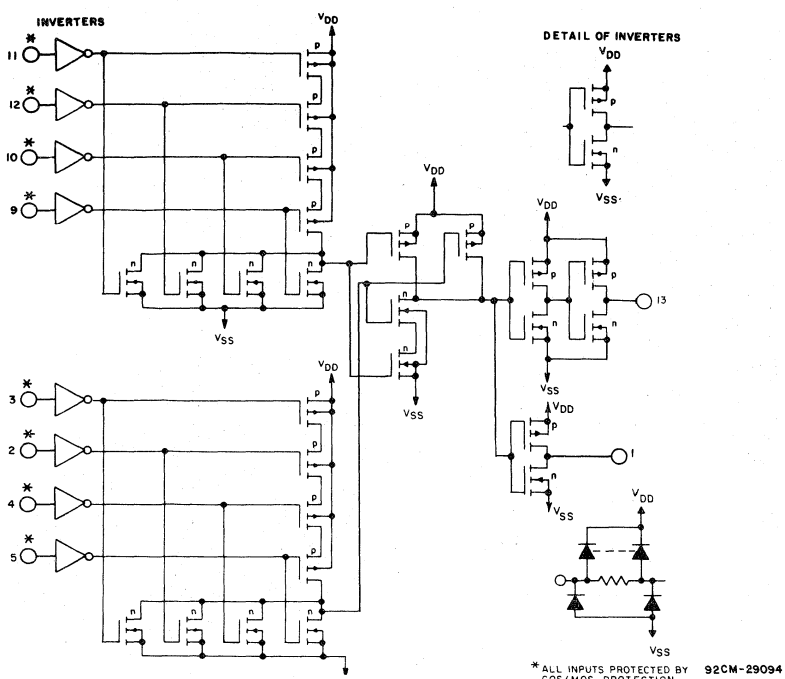


Fig. 7 — Schematic diagram.

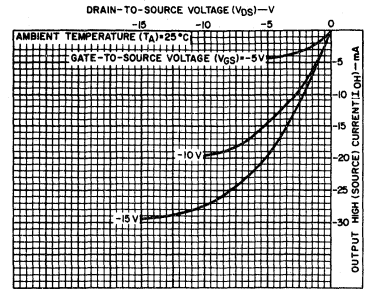


Fig. 4 — Typical output high (source) current characteristics.

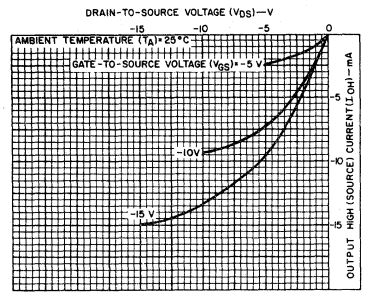


Fig. 5 — Minimum output high (source) current characteristics.

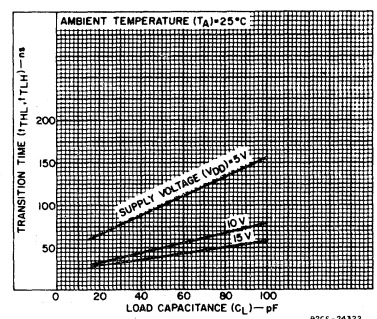


Fig. 6 — Typical transition time as a function of load capacitance.

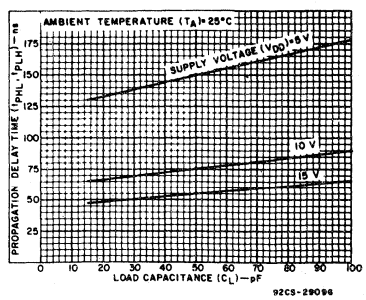


Fig. 8 — Typical propagation delay time as a function of load capacitance.

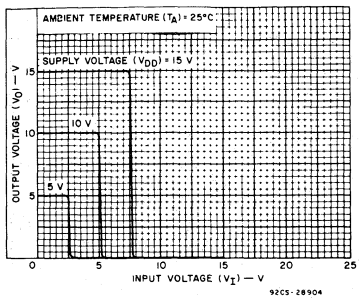


Fig. 9 — Typical voltage transfer characteristics (NAND output).

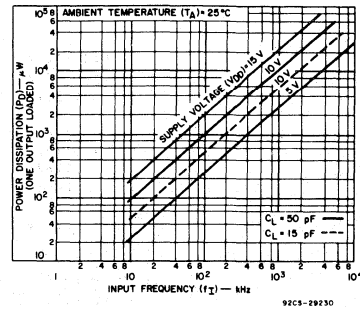


Fig. 10 — Typical dynamic power dissipation as a function of frequency.

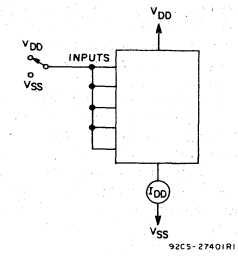


Fig. 11 — Quiescent-device-current test circuit.

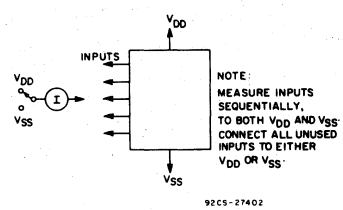


Fig. 12 — Input current test circuit.

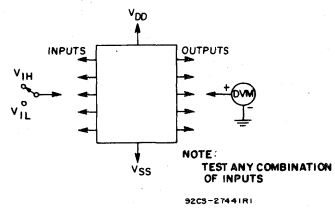


Fig. 13 — Input-voltage test circuit.

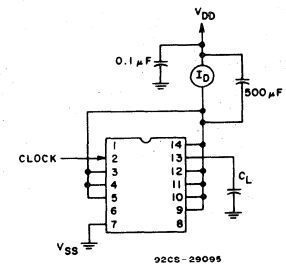
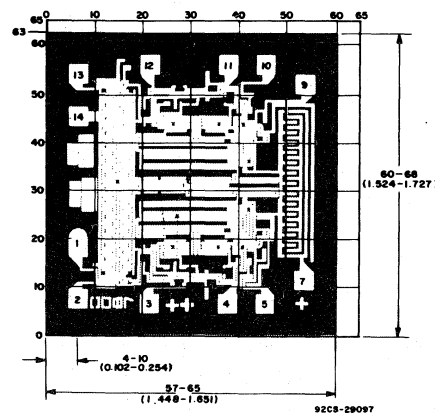


Fig. 14 — Dynamic power dissipation test circuit.



Dimensions and pad layout for CD4068BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS Hex Inverter

High-Voltage Types (20-Volt Rating)

The RCA-CD4069UB types consist of six COS/MOS inverter circuits. These devices are intended for all general-purpose inverter applications where the medium-power TTL-drive and logic-level-conversion capabilities of circuits such as the CD4009 and CD4049 Hex Inverter/Buffers are not required.

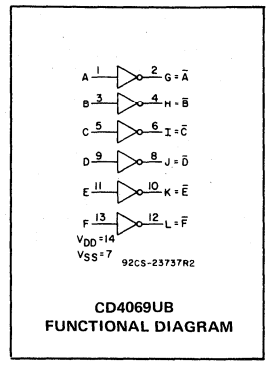
The CD4069UB-Series types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- **Standardized symmetrical output characteristics**
- **Medium Speed Operation—t_{PHL},t_{PLH}=30 ns (typ.) at 10 V**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

- **Logic inversion**
- **Pulse shaping**
- **Oscillators**
- **High-input-impedance amplifiers**



CD4069UB FUNCTIONAL DIAGRAM

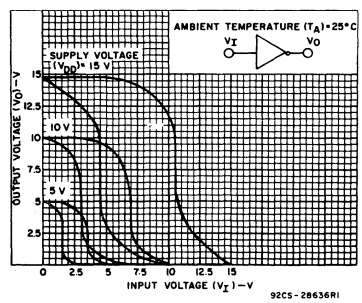


Fig. 1 — Minimum and maximum voltage transfer characteristics.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

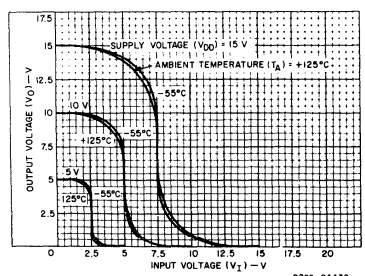


Fig. 2 — Typical voltage transfer characteristics as a function of temperature.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC		CONDITIONS V_{DD} V	ALL TYPES LIMITS Typ.	ALL TYPES LIMITS Max.	UNITS
Propagation Delay Time;	t_{PLH}, t_{PHL}	5	55	110	ns
		10	30	60	
		15	25	50	
Transition Time;	t_{THL}, t_{TLH}	5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance;	C_{IN}	Any Input	10	15	pF

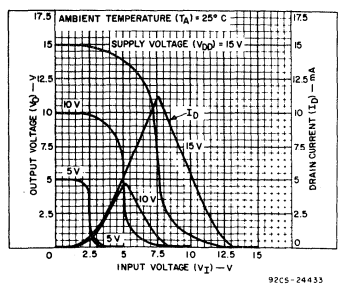


Fig. 3 — Typical current and voltage transfer characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	4.5	–	5	1				—	—	1	V
	9	–	10	2.5				—	—	2.5	
	13.5	–	15	3				—	—	3	
Input High Voltage, V_{IH} Min.	0.5	–	5	4				4	—	—	
	1	–	10	8				8	—	—	
	1.5	–	15	12.5				12.5	—	—	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

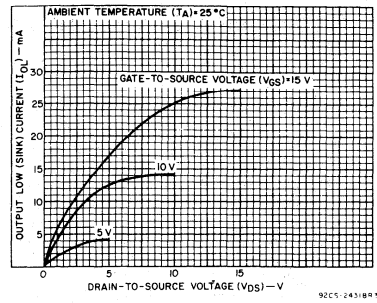


Fig. 4 — Typical output low (sink) current characteristics.

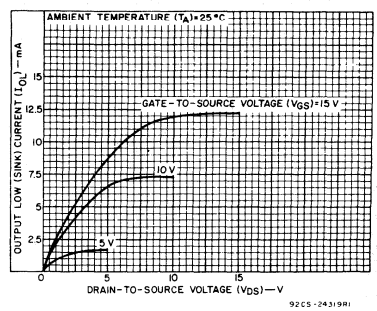


Fig. 5 — Minimum output low (sink) current characteristics.

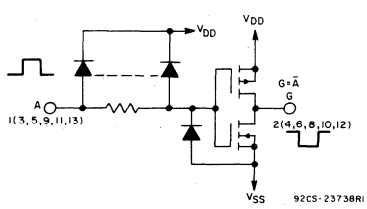


Fig. 6 — Schematic diagram of one of six identical inverters.

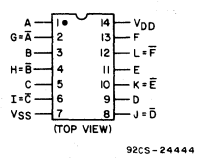


Fig. 7 — CD4069UB terminal assignment.

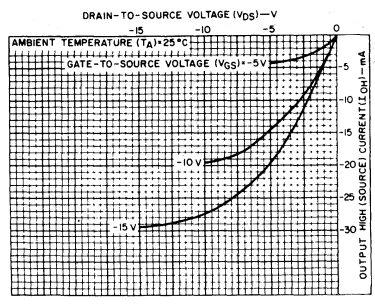


Fig. 8 — Typical output high (source) current characteristics.

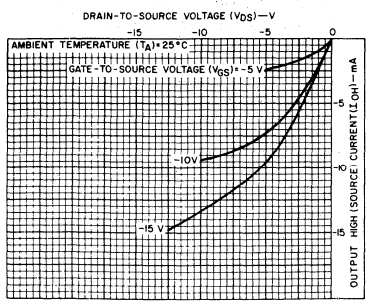


Fig. 9 — Minimum output high (source) current characteristics.

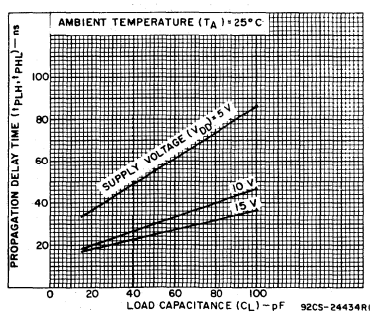


Fig. 10 — Typical propagation delay time vs. load capacitance.

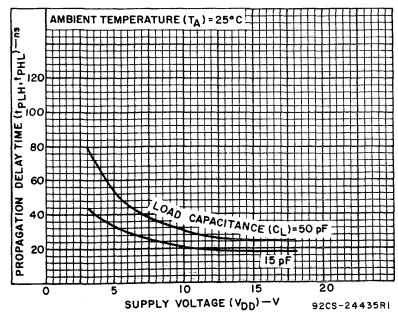


Fig. 11 — Typical propagation delay time vs. supply voltage.

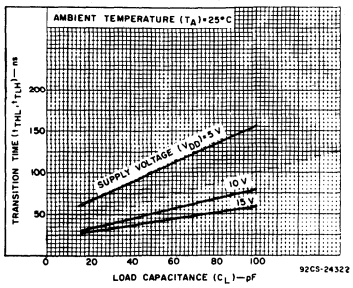


Fig. 12 – Typical transition time vs. load capacitance.

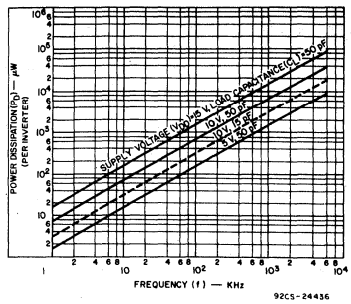


Fig. 13 – Typical dynamic power dissipation vs. frequency.

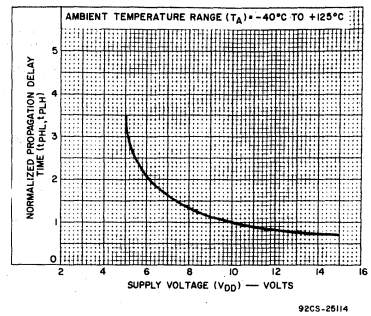


Fig. 14 – Variation of normalized propagation delay time (t_{PHL} and t_{PLH}) with supply voltage.

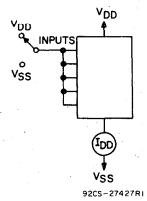


Fig. 15 – Quiescent device current test circuit.

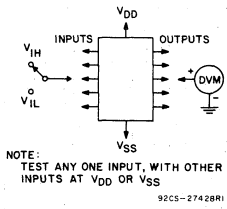


Fig. 16 – Noise immunity test circuit.

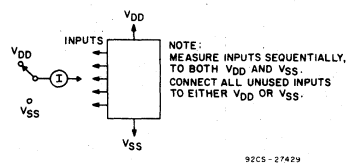
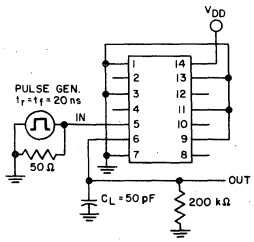


Fig. 17 – Input leakage current test circuit.



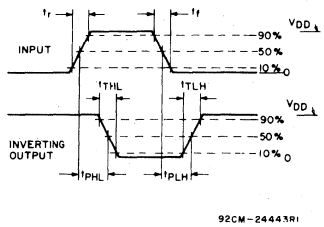


Fig. 18 – Dynamic electrical characteristics test circuit and waveforms.

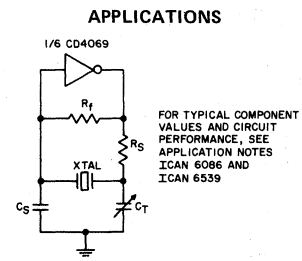


Fig. 19 – Typical crystal oscillator circuit.

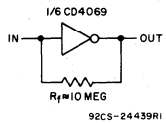


Fig. 20 – High-input impedance amplifier.

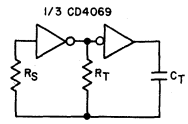


Fig. 21 – Typical RC oscillator circuit.

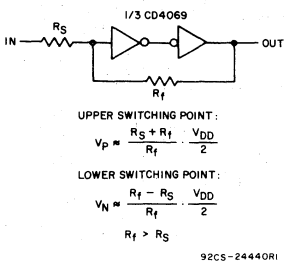
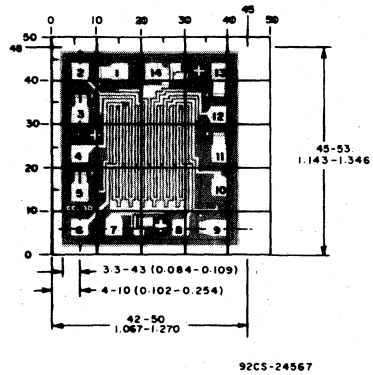


Fig. 22 – Input pulse shaping circuit (Schmitt trigger).

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

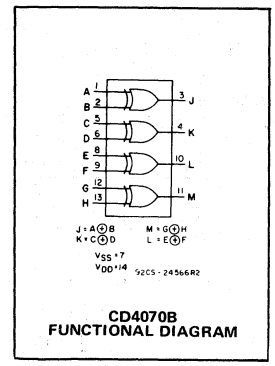


Dimensions and pad layout for CD4069UBH.

COS/MOS Quad Exclusive-OR and Exclusive-NOR Gates

High-Voltage Types (20-Volt Rating)

CD4070B – Quad Exclusive-OR Gate
CD4077B – Quad Exclusive-NOR Gate



CD4070B
FUNCTIONAL DIAGRAM

The RCA-CD4070B contains four independent Exclusive-OR gates. The RCA-CD4077B contains four independent Exclusive-NOR gates.

The CD4070B and CD4077B provide the system designer with a means for direct implementation of the Exclusive-OR and Exclusive-NOR functions, respectively. The CD4070B is similar to the RCA-CD4030A, but has greater output sourcing capability and higher input impedance.

The CD4070B- and CD4077B-Series types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- **Medium-speed operation–$t_{PHL} = t_{PLH}$ = 70 ns (typ.) at V_{DD} = 10 V, C_L = 50 pF**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 mA at 18 V and 25°C**
- **Noise margin (over full package-temperature range):**
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- **5-V, 10-V, and 15-V parametric ratings**
- **Standardized symmetrical output characteristics**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

- **Logical comparators**
- **Adders/subtractors**
- **Parity generators and checkers**

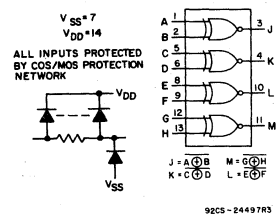


Fig. 1 – CD4077B functional diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . –0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = –40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
PACKAGE TYPE E . . . . . –40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)	3	18	V

TRUTH TABLE CD4070B
1 of 4 Gates

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

Where 1 = High Level
" 0 = Low Level
$J = A \oplus B$

TRUTH TABLE CD4077B
1 of 4 Gates

A	B	J
0	0	1
1	0	0
0	1	0
1	1	1

Where 1 = High Level
" 0 = Low Level
$J = \overline{A \oplus B}$

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55,+25,+125 Apply to D,K,F,H Pkgs. Values at −40,+25,+85 Apply to E Pkgs.							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

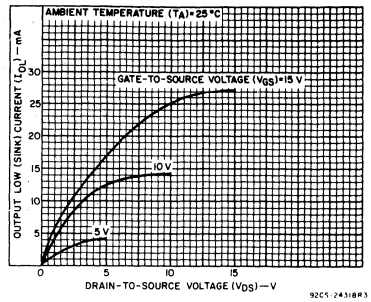


Fig. 2 – Typical output low (sink) current characteristics.

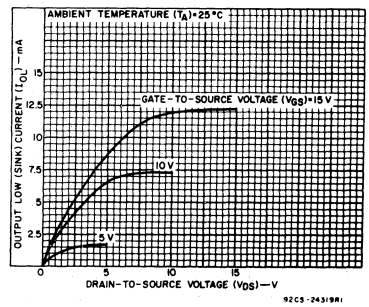


Fig. 3 – Minimum output low (sink) current characteristics.

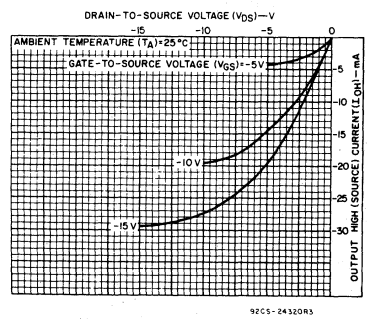


Fig. 4 – Typical output high (source) current characteristics.

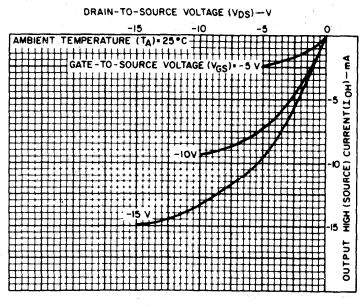


Fig. 5 – Minimum output high (source) current characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC		CONDITIONS V_{DD} V	ALL TYPES LIMITS Typ.	Max.	UNITS
Propagation Delay Time;	t_{PLH}, t_{PHL}	5	175	350	ns
		10	70	140	
		15	50	100	
Transition Time;	t_{THL}, t_{TLH}	5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance;	C_{IN}	Any Input	5	7.5	pF

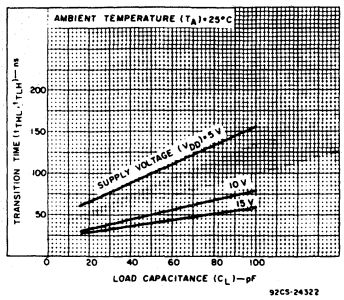


Fig. 6 – Typical transition time vs. load capacitance.

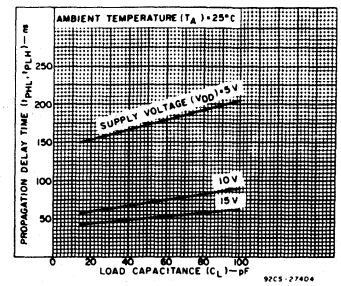


Fig. 7 – Typical propagation delay time vs. load capacitance.

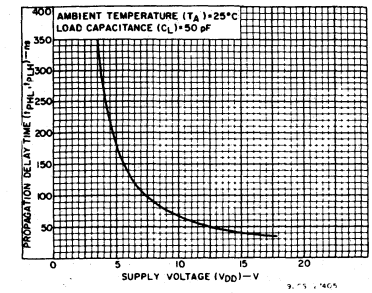


Fig. 8 – Typical propagation delay time vs. supply voltage.

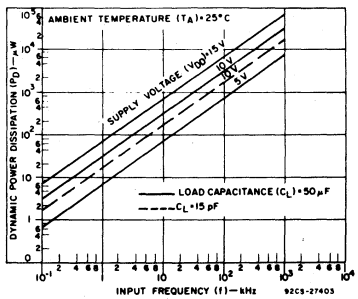


Fig. 9 – Typical dynamic power dissipation vs. input frequency.

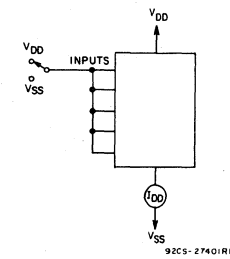


Fig. 10 – Quiescent device current.

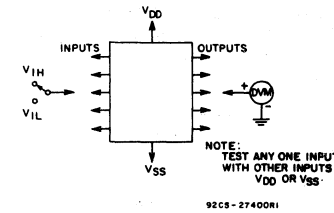


Fig. 11 – Input voltage.

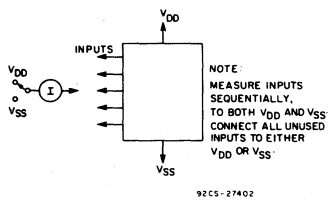
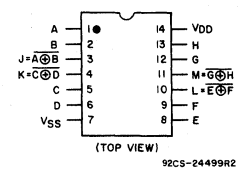
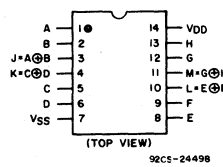


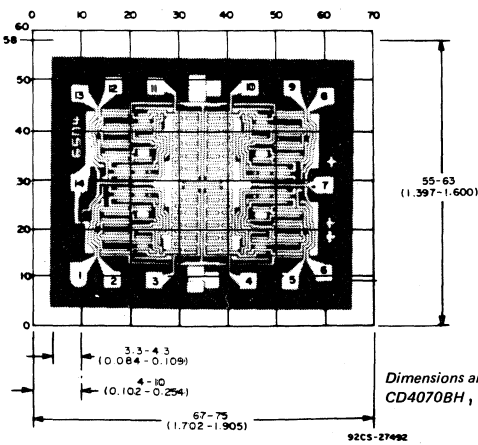
Fig. 12 – Input leakage.



TERMINAL ASSIGNMENT
CD4077B



TERMINAL ASSIGNMENT
CD4070B



Dimensions and pad layout for CD4070BH, CD4077BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS OR Gates

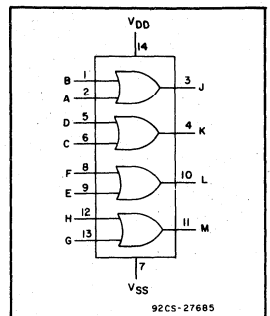
High-Voltage Types (20-Volt Rating)

CD4071B Quad 2-Input OR Gate
CD4072B Dual 4-Input OR Gate
CD4075B Triple 3-Input OR Gate

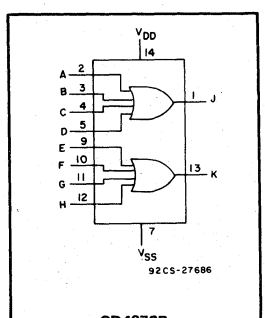
The RCA-CD4071B, CD4072B, and CD4075B OR gates provide the system designer with direct implementation of the positive-logic OR function and supplement the existing family of COS/MOS gates. The CD4071, CD4072, and CD4075 types are supplied in 14-lead dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

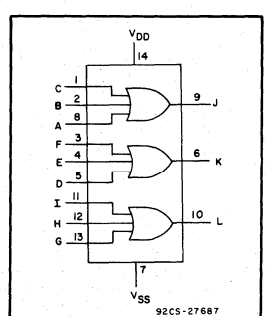
- Medium-Speed Operation-t_{PLH}, t_{PHL} = 60 ns (typ.) at V_{DD} = 10 V
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Standardized, symmetrical output characteristics
- Noise margin (over full package temperature range)
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13 A, "Standard Specifications for Description of 'B' Series CMOS Devices"



CD4071B
FUNCTIONAL DIAGRAM



CD4072B
FUNCTIONAL DIAGRAM



CD4075B
FUNCTIONAL DIAGRAM

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				–	—	4	
Input High Voltage, V_{IH} Min.	4.5	–	5	3.5				3.5	—	—	
	9	–	10	7				7	—	—	
	13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, and C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		ALL TYPES LIMITS		UNITS
		V_{DD} VOLTS	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH}		5	125	250	ns
		10	60	120	
		15	45	90	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input	—	5	7.5	pF

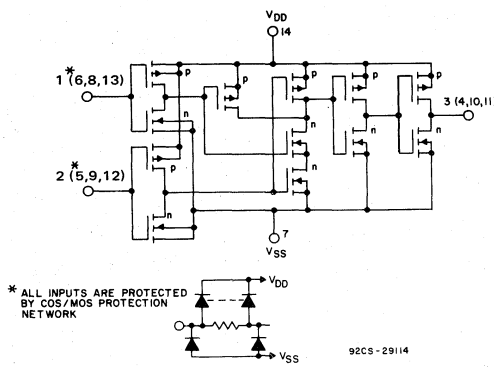


Fig. 3 — Schematic diagram for CD4071B (1 of 4 identical gates).

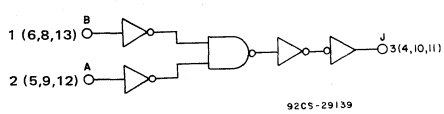


Fig. 5 — Logic diagram for CD4071B (1 of 4 identical gates).

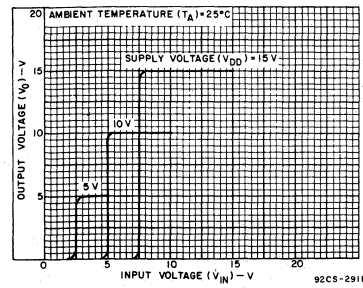


Fig. 1 — Typical voltage transfer characteristics.

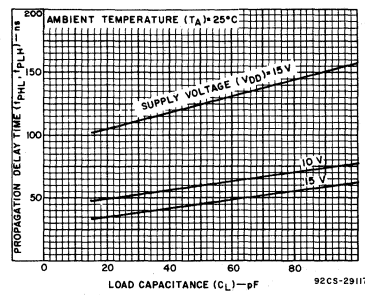


Fig. 2 — Typical propagation delay time as a function of load capacitance.

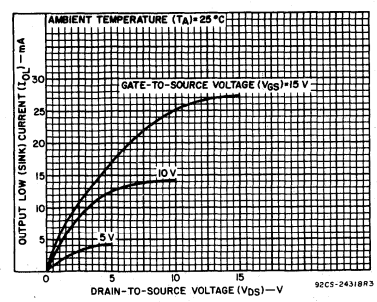


Fig. 4 — Typical output low (sink) current characteristics.

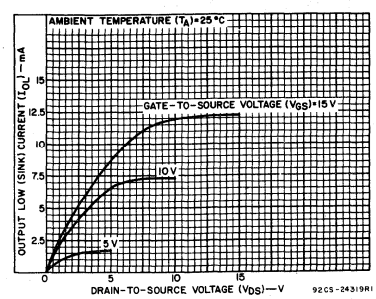


Fig. 6 — Minimum output low (sink) current characteristics.

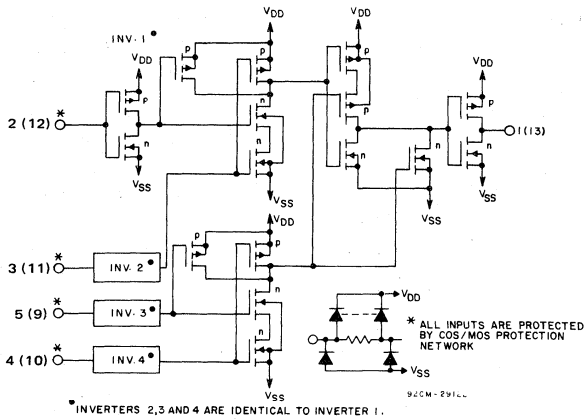


Fig. 7 – Schematic diagram for CD4072B (1 of 2 identical gates).

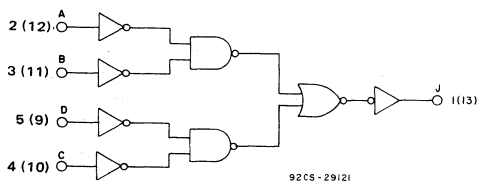


Fig. 9 – Logic diagram for CD4072B (1 of 2 identical gates).

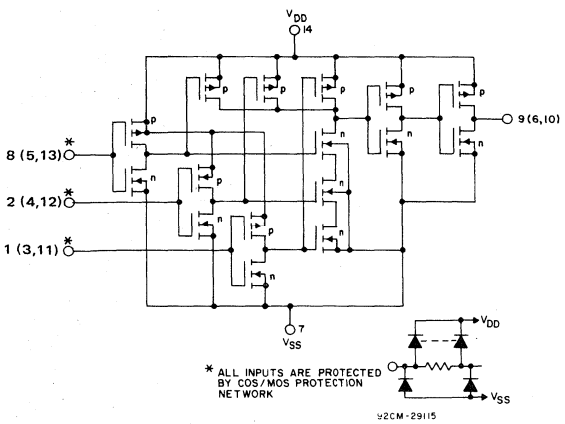


Fig. 11 – Schematic diagram for CD4075B (1 of 3 identical gates).

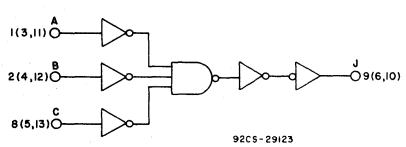


Fig. 13 – Logic diagram for CD4075B (1 of 3 identical gates).

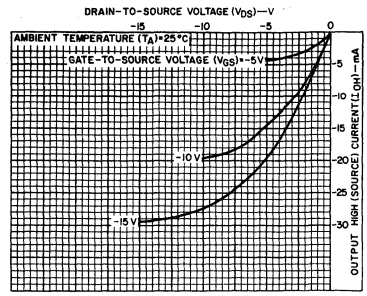


Fig. 8 – Typical output high (source) current characteristics.

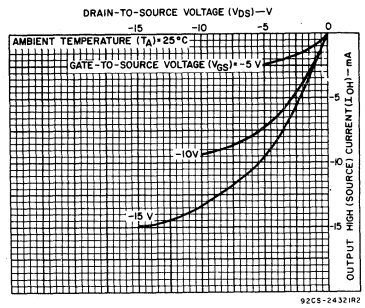


Fig. 10 – Minimum output high (source) current characteristics.

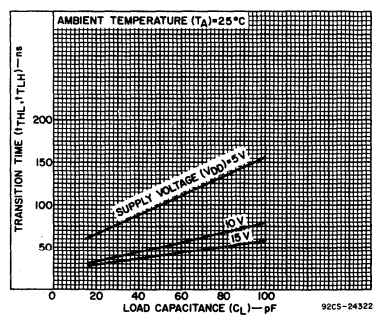


Fig. 12 – Typical transition time as a function of load capacitance.

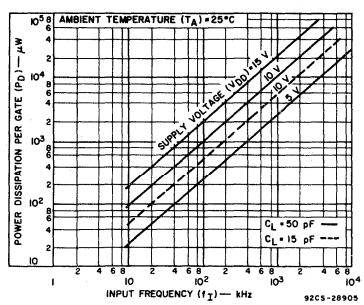
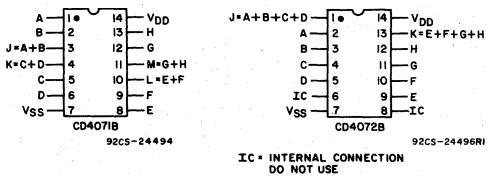
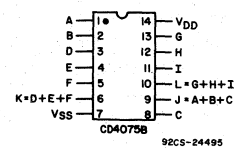


Fig. 14 – Typical dyanamic power dissipation as a function of frequency.

TERMINAL ASSIGNMENTS (TOP VIEW)





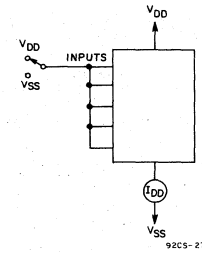


Fig. 15 — Quiescent device current test circuit.

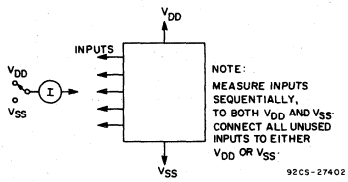


Fig. 16 — Input current test circuit.

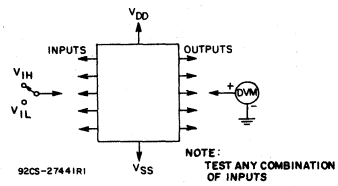
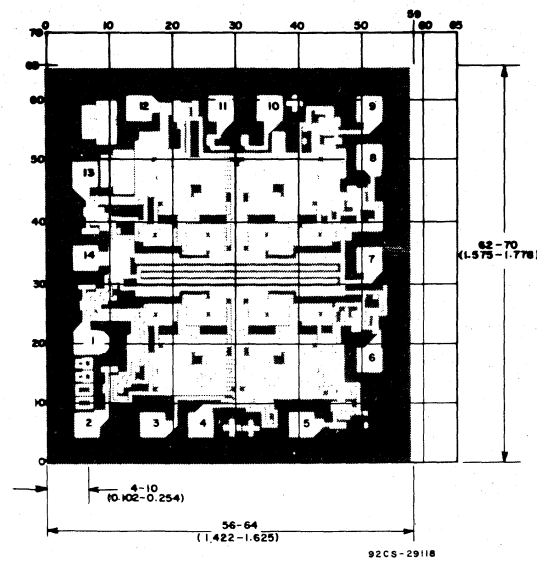


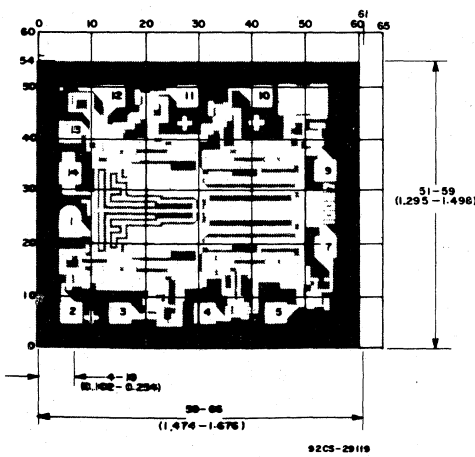
Fig. 17 — Input-voltage test circuit.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

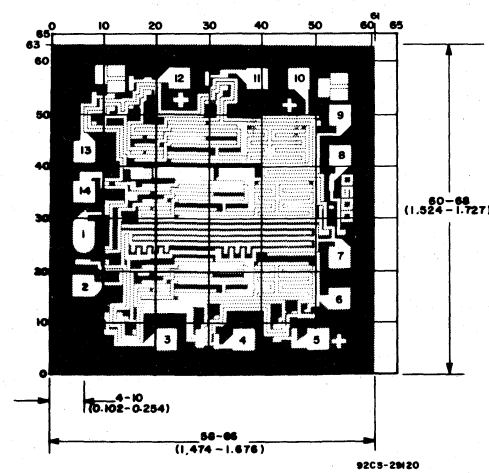
The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.



Dimensions and pad layout for CD4071B.



Dimensions and pad layout for CD4072B.



Dimensions and pad layout for CD4075B.

CD4081B, CD4082B, CD4073B Types

COS/MOS AND Gates

High-Voltage Types (20-Volt Rating)

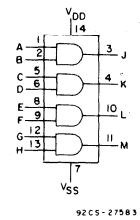
CD4081B Quad 2-Input AND Gate
CD4082B Dual 4-Input AND Gate
CD4073B Triple 3-Input AND Gate

The RCA-CD4081B, CD4082B, and CD-4073B AND gates provide the system designer with direct implementation of the AND function and supplement the existing family of COS/MOS gates.

The CD4081B, CD4082B, and CD4073B types are supplied in 14-lead dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

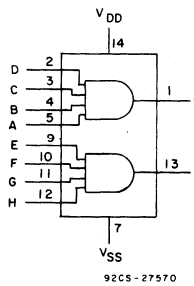
- **Medium-Speed Operation – t_{PLH}, t_{PHL} = 60 ns (typ.) at V_{DD} = 10 V**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (full package-temperature range) =**
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- **Standardized, symmetrical output characteristics**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**



CD4081B
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . –0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = –40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K). . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
PACKAGE TYPE E . . . . . –40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C



CD4082B
FUNCTIONAL DIAGRAM

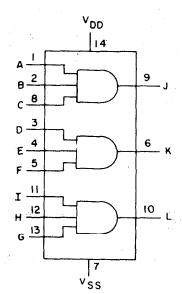
RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C, Input t_r,t_f=20 ns, and C_L=50 pF, R_L=200 kΩ

CHARACTERISTIC	TEST CONDITIONS		ALL TYPES LIMITS		UNITS
		V_{DD} Volts	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH}		5	125	250	ns
		10	60	120	
		15	45	90	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input	–	5	7.5	pF



CD4073B
FUNCTIONAL DIAGRAM

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5	–	5	1.5				–	–	1.5	V
	1	–	10	3				–	–	3	
	1.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

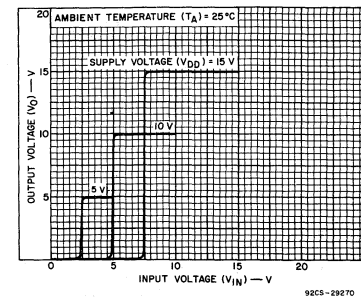


Fig. 1 — Typical voltage transfer characteristics.

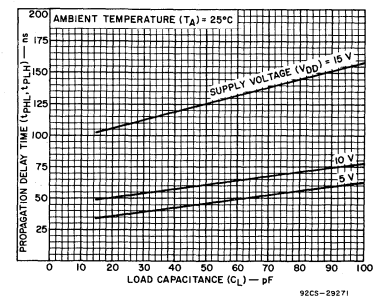


Fig. 2 — Typical propagation delay time as a function of load capacitance.

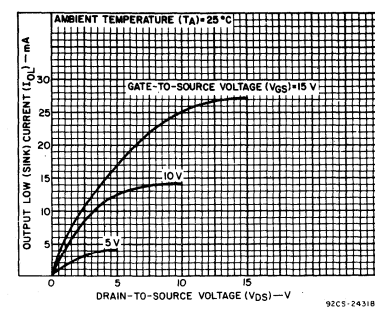


Fig. 3 — Typical output low (sink) current characteristics.

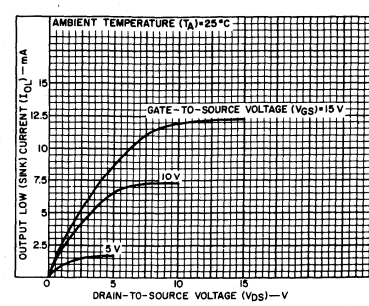


Fig. 6 — Minimum output low (sink) current characteristics.

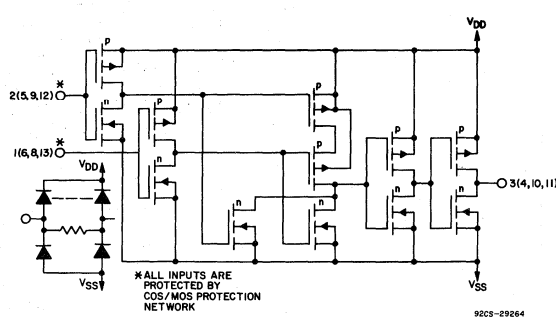


Fig. 4 — Schematic diagram for CD4081B (1 of 4 identical gates).

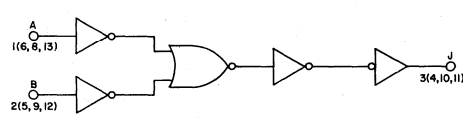


Fig. 5 — Logic diagram for CD4081B (1 of 4 identical gates).

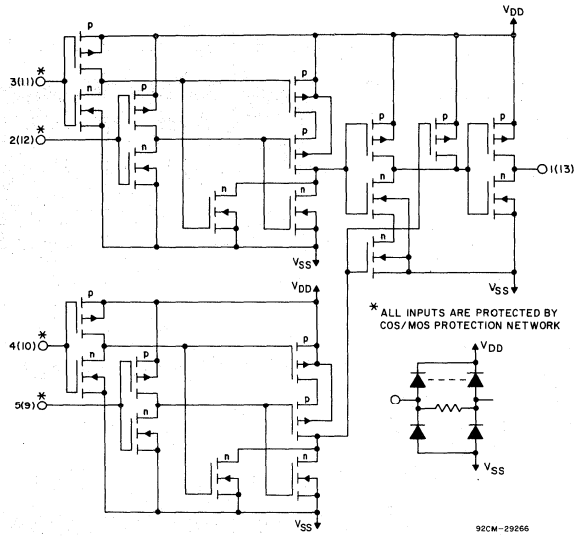


Fig. 8 – Schematic diagram for CD4082B (1 of 2 identical gates).

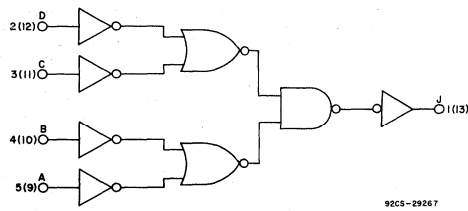


Fig. 9 – Logic diagram for CD4082B (1 of 2 identical gates).

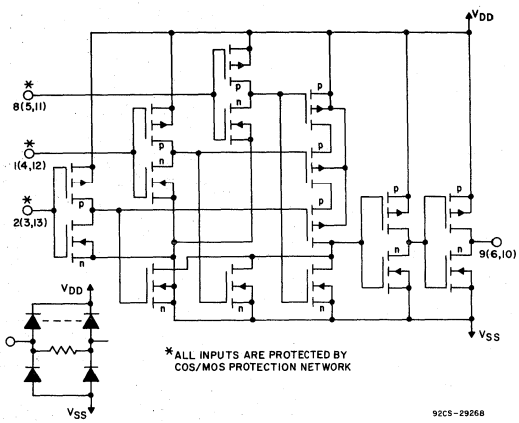


Fig. 12 – Schematic diagram for CD4073B (1 of 3 identical gates).

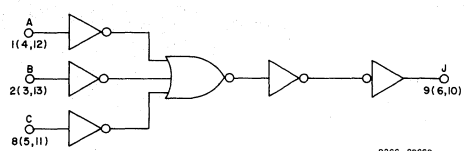


Fig. 13 – Logic diagram for CD4073B (1 of 3 identical gates).

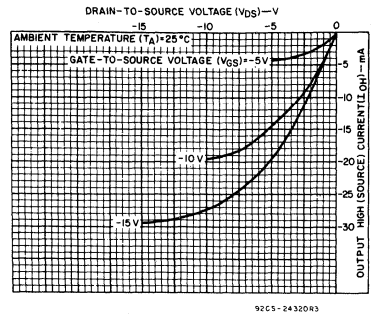


Fig. 7 – Typical output high (source) current characteristics.

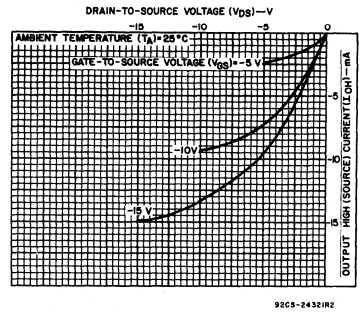


Fig. 10 – Minimum output high (source) current characteristics.

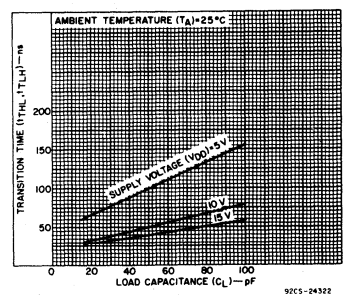


Fig. 11 – Typical transition time as a function of load capacitance.

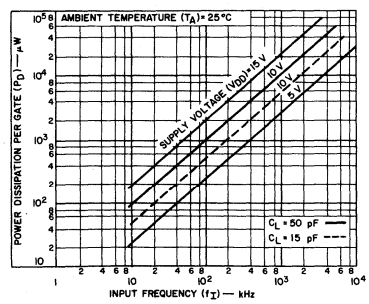


Fig. 14 – Typical dynamic power dissipation per gate as a function of frequency.

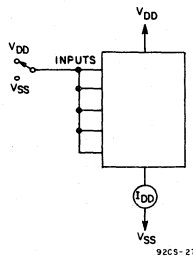


Fig. 15 – Quiescent device current test circuit.

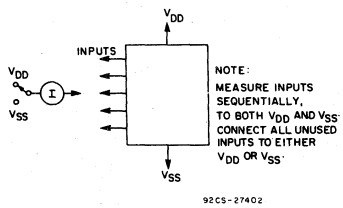


Fig. 16 – Input current test circuit.

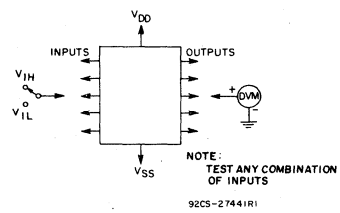
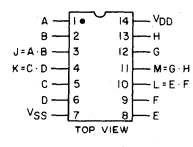
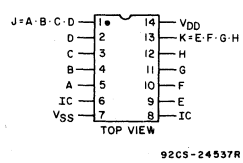


Fig. 17 – Input-voltage test circuit.

TERMINAL ASSIGNMENTS

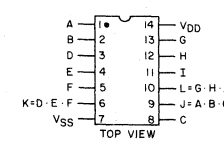


CD4081B

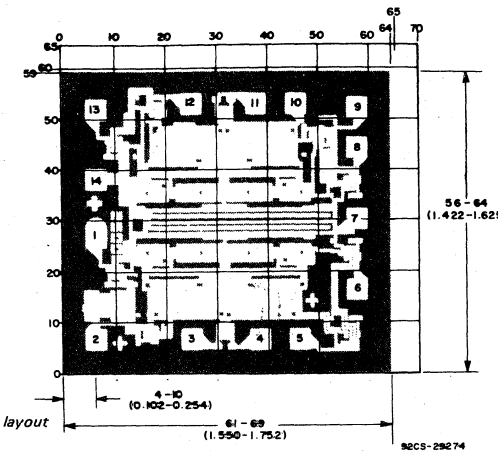


CD4082B

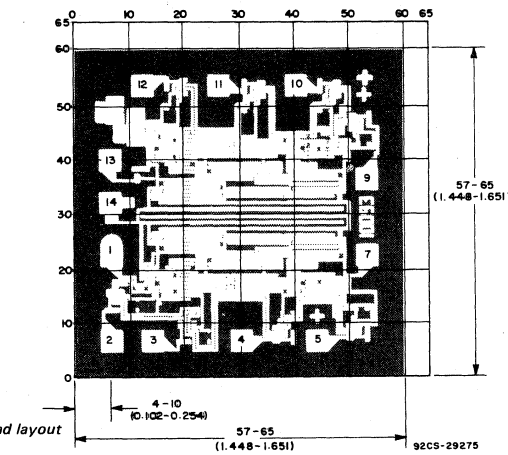
IC = INTERNAL CONNECTION - DO NOT USE



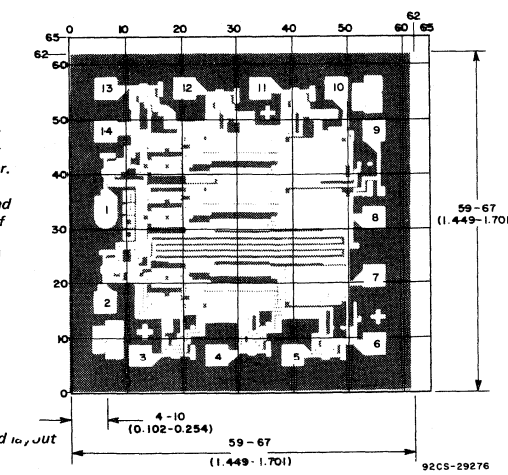
CD4073B



Dimensions and pad layout for CD4081B.



Dimensions and pad layout for CD4082B.



Dimensions and pad layout for CD4073B.

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

COS/MOS 4-Bit D-Type Registers

High-Voltage Types (20-Volt Rating)

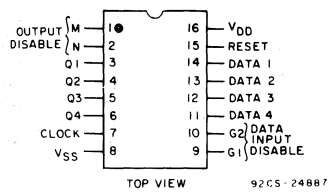
The CD4076B types are four-bit registers consisting of D-type flip-flops that feature three-state outputs. Data Disable inputs are provided to control the entry of data into the flip-flops. When both Data Disable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the clock input. Output Disable inputs are also provided. When the Output Disable inputs are both low, the normal logic states of the four outputs are available to the load. The outputs are disabled independently of the clock by a high logic level at either Output Disable input, and present a high impedance.

The CD4076B types are supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

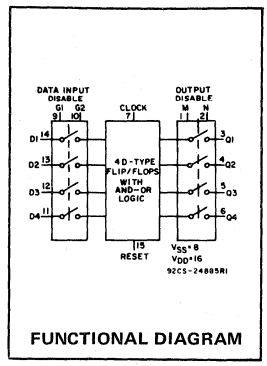
Features:

- **Three-state outputs**
- **Input disabled without gating the clock**
- **Gated output control lines for enabling or disabling the outputs**
- **Standardized, symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C**
- **Noise margin over full package temperature range:**

  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**



TERMINAL ASSIGNMENT



FUNCTIONAL DIAGRAM

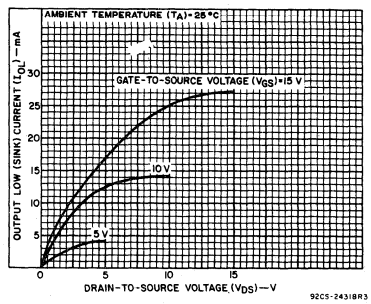


Fig.1 — Typical output low (sink) current characteristics.

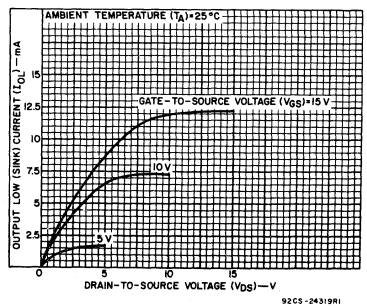


Fig.2 — Minimum output low (sink) current characteristics.

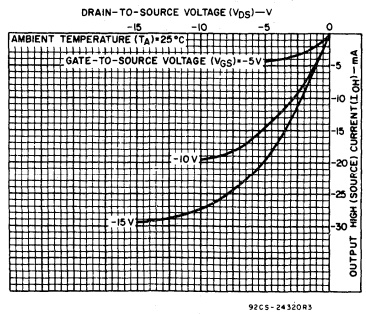


Fig.3 — Typical output high (source) current characteristics.

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)		3	18	V
Data Setup Time, t_S	5	200	–	ns
	10	80	–	
	15	60	–	
Clock Pulse Width, t_W	5	200	–	ns
	10	100	–	
	15	80	–	
Clock Input Frequency, f_{CL}	5		3	MHz
	10	dc	6	
	15		8	
Clock Input Rise or Fall Time, t_rCL, t_fCL	5	–	15	μs
	10	–	5	
	15	–	5	
Reset Pulse Width, t_W	5	120	–	ns
	10	50	–	
	15	40	–	
Data Input Disable Setup Time, t_S	5	180	–	ns
	10	100	–	
	15	70	–	

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

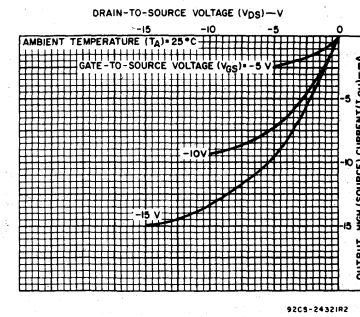


Fig.4 — Minimum output high (source) current characteristics.

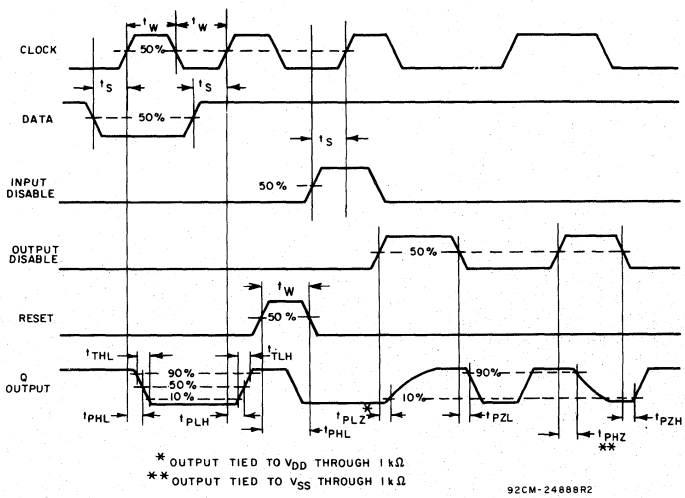


Fig.5 — Functional waveforms for CD4076B.

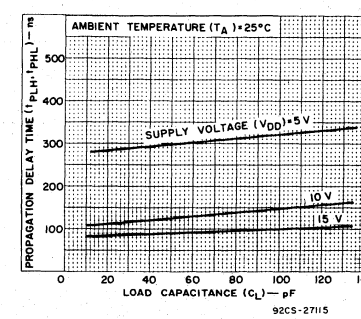


Fig.6 — Typical propagation delay time vs. load capacitance (clock to Q).

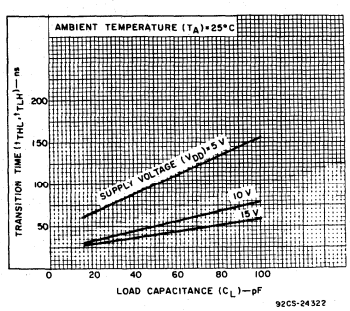


Fig.7 — Typical transition time vs. load capacitance.

Truth Table

Reset	Clock	Data Input Disable G1	Data Input Disable G2	Data D	Next State Output Q	
1	X	X	X	X	0	
0	0	X	X	X	Q	NC
0	↓	1	X	X	Q	NC
0	↓	X	1	X	Q	NC
0	↓	0	0	1	1	
0	↓	0	0	0	0	
0	1	X	X	X	Q	NC
0	↓	X	X	X	Q	NC

When either Output Disable M or N is high, the outputs are disabled (high impedance state); however sequential operation of the flip-flops is not affected.

1 ≡ High Level
0 ≡ Low Level
X = Don't Care
NC = No Change

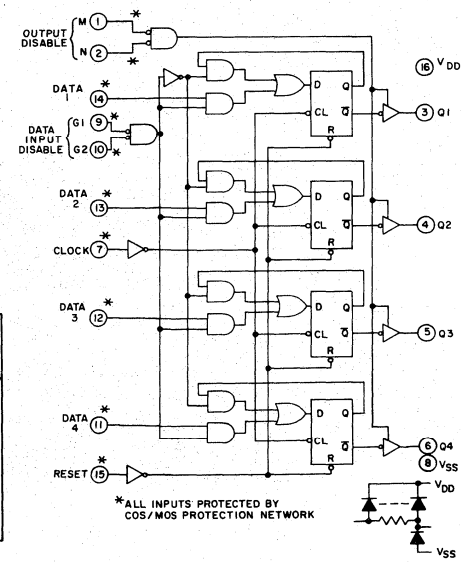


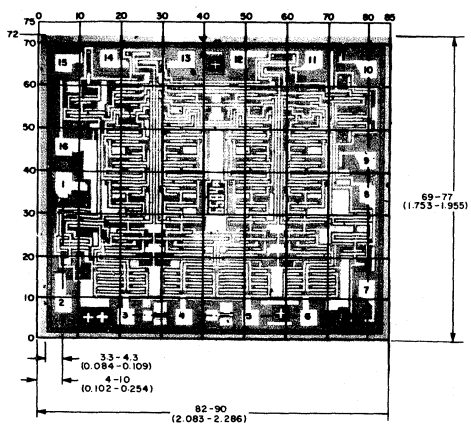
Fig.8 — CD4076B logic diagram.

CD4076B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA
3-State Output Leakage Current I_{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	–	$\pm 10^{-4}$	±0.4	μA

Dimensions and pad layout for CD4076BH



Dimensions and pad layout for CD4076BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r,t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ (Unless otherwise noted)

CHARACTERISTIC	TEST CONDITIONS	V_{DD} V	LIMITS Min.	Typ.	Max.	UNITS
Propagation Delay Time: Clock to Q Output, t_{PHL}, t_{PLH}		5	–	300	600	ns
		10	–	125	250	
		15	–	90	180	
Reset, t_{PHL}		5	–	230	460	
		10	–	100	200	
		15	–	75	150	
3-State Output 1 or 0 to High Impedance, t_{PHZ}, t_{PLZ}	R_L = 1 kΩ	5	–	150	300	
		10	–	75	150	
		15	–	60	120	
3-State High Impedance to 1 or 0 Output, t_{PZH}, t_{PZL}	R_L = 1 kΩ	5	–	150	300	
		10	–	75	150	
		15	–	60	120	
Transition Time, t_{THL}, t_{TLH}		5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Maximum Clock Input Frequency, f_{CL}		5	3	6	–	MHz
		10	6	12	–	
		15	8	16	–	
Minimum Clock Pulse Width, t_W		5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Maximum Clock Input Rise or Fall Time, t_{rcl}, t_{fcl}		5	15	–	–	μs
		10	5	–	–	
		15	5	–	–	
Minimum Reset Pulse With, t_W		5	–	60	120	ns
		10	–	25	50	
		15	–	20	40	
Minimum Data Setup Time, t_S		5	–	100	200	ns
		10	–	40	80	
		15	–	30	60	
Minimum Data Input Disable Setup Time, t_S		5	–	90	180	ns
		10	–	50	100	
		15	–	35	70	
Input Capacitance, C_{IN}	Any Input	–	–	5	7.5	pF

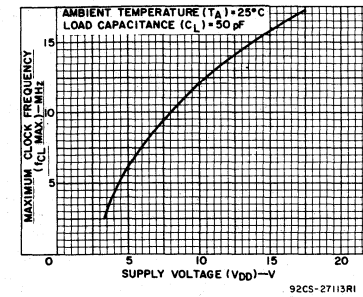


Fig.9 – Typical maximum clock input frequency vs. supply voltage.

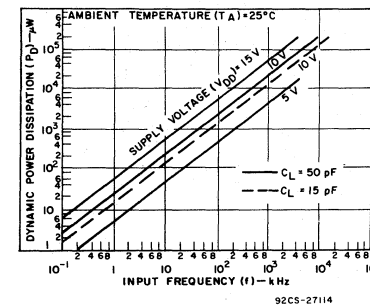


Fig.10 – Typical dynamic power dissipation vs. frequency.

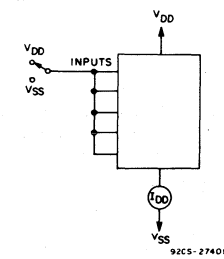


Fig.11 – Quiescent device current test circuit.

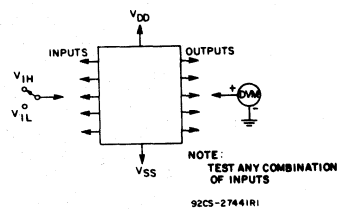


Fig.12 – Input voltage test circuit.

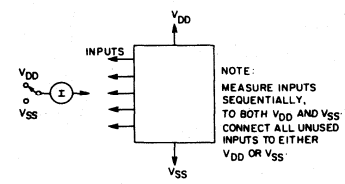


Fig. 13 – Input current test circuit.

COS/MOS 8-Input NOR/OR Gate

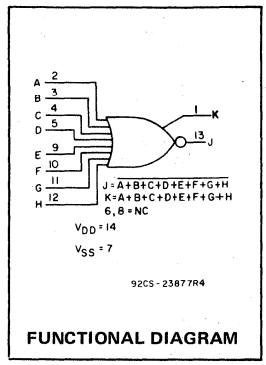
High-Voltage Types (20-Volt Rating)

The RCA-CD4078B NOR/OR Gate provides the system designer with direct implementation of the positive-logic 8-input NOR and OR functions and supplements the existing family of COS/MOS gates.

The CD4078B types are supplied in 14-lead dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Medium-Speed Operation: t_{PHL}, t_{PLH} = 75 ns (typ.) at V_{DD} = 10 V**
- **Buffered inputs and output**
- **5-V, 10-V, and 15-V parametric ratings**
- **Standardized symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range: 100 nA at 18 V and 25°C**
- **Noise margin (over full package-temperature range): 1 V at V_{DD} = 5 V; 2 V at V_{DD} = 10 V; 2.5 V at V_{DD} = 15 V**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**



FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	Min.	Max.	Units
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

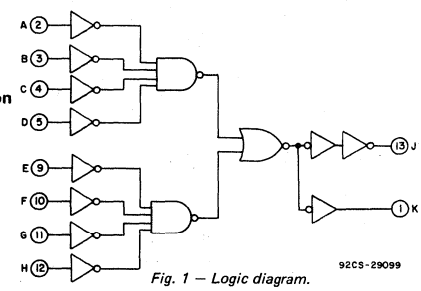


Fig. 1 — Logic diagram.

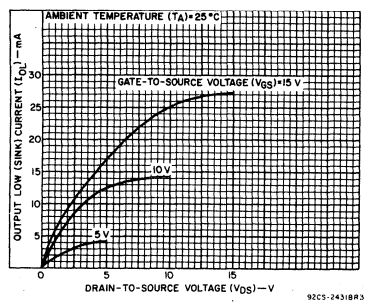


Fig. 2 — Typical output low (sink) current characteristics.

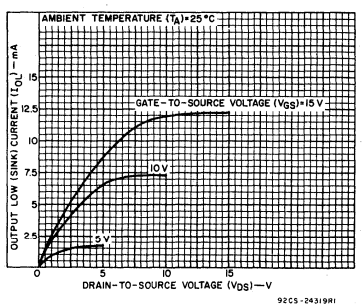


Fig. 3 — Minimum output low (sink) current characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200kΩ

CHARACTERISTIC	TEST CONDITIONS	ALL TYPES LIMITS			UNITS
		V_{DD} VOLTS	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH}		5	150	300	ns
		10	75	150	
		15	55	110	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input		5	7.5	pF

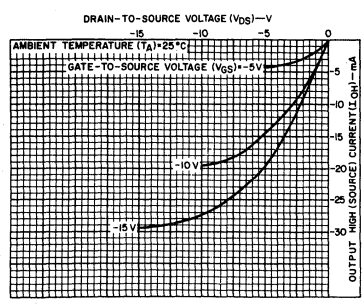


Fig. 4 — Typical output high (source) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1		mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6		
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8		
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1		
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2		
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6		
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8		
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05					0	0.05	V
	–	0,10	10	0.05					0	0.05	
	–	0,15	15	0.05					0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5		
	–	0,10	10	9.95				9.95	10		
	–	0,15	15	14.95				14.95	15		
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

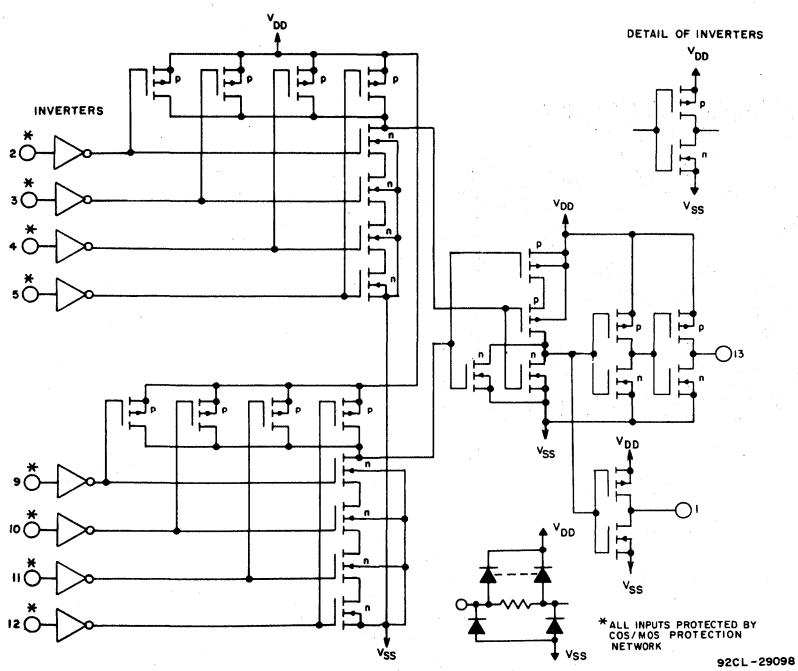


Fig. 8 — Schematic diagram.

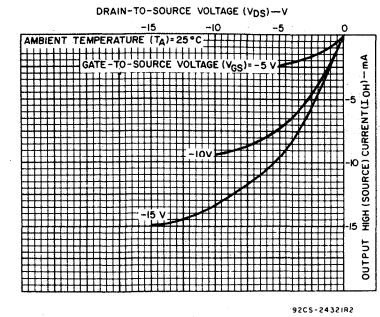


Fig. 5 — Minimum output high (source) current characteristics.

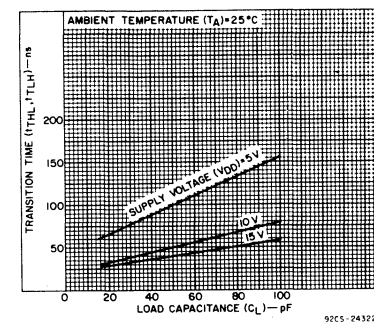


Fig. 6 — Typical transition time as a function of load capacitance.

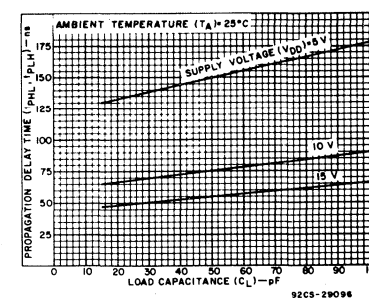


Fig. 7 — Typical propagation delay time as a function of load capacitance.

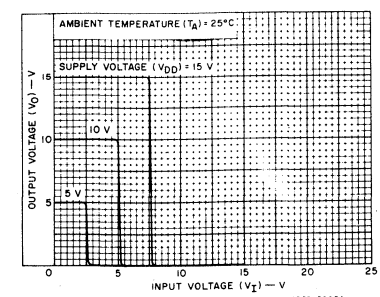


Fig. 9 — Typical voltage transfer characteristics (NOR output).

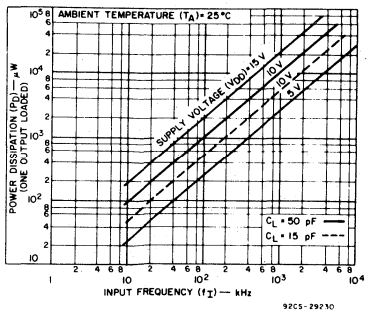


Fig. 10 — Typical dynamic power dissipation as a function of frequency.

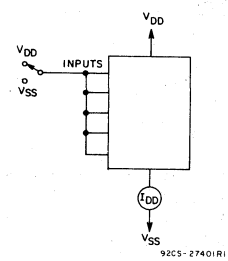


Fig. 11 — Quiescent-device-current test circuit.

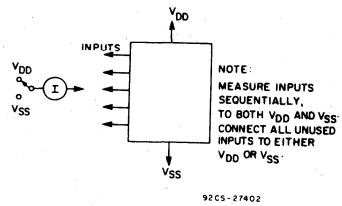


Fig. 12 — Input current test circuit.

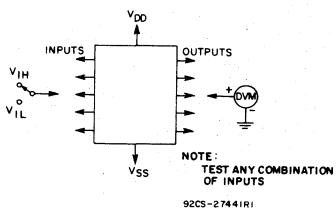


Fig. 13 — Input-voltage test circuit.

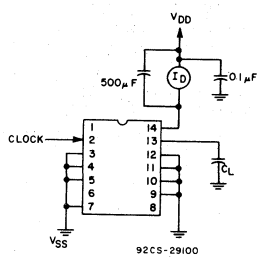
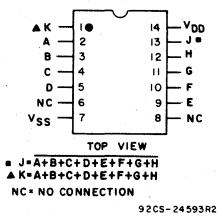
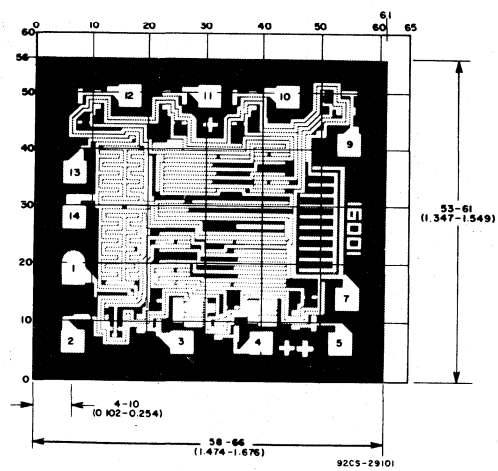


Fig. 14 — Dynamic power dissipation test circuit.



TERMINAL ASSIGNMENT



Dimensions and pad layout for CD4078BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS Dual 2-Wide 2-Input AND-OR-INVERT Gate

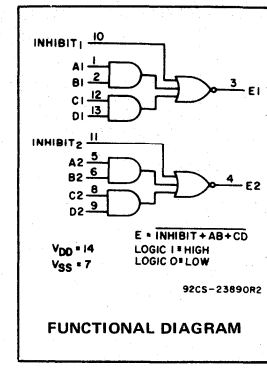
High-Voltage Types (20-Volt Rating)

The RCA-CD4085 contains a pair of AND-OR-INVERT gates, each consisting of two 2-input AND gates driving a 3-input NOR gate. Individual inhibit controls are provided for both A-O-I gates.

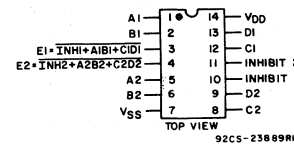
The CD4085B types are supplied in 14-lead dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packs (K suffix), and in chip form (H suffix).

Features:

- **Medium-speed operation – t_{PHL} = 90 ns; t_{PLH} = 125 ns (typ.) at 10 V**
- **Individual inhibit controls**
- **Standardized symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (over full package-temperature range):**
  - **1 V at V_{DD} = 5 V**
  - **2 V at V_{DD} = 10 V**
  - **2.5 V at V_{DD} = 15 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**



FUNCTIONAL DIAGRAM



TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)	3	18	V

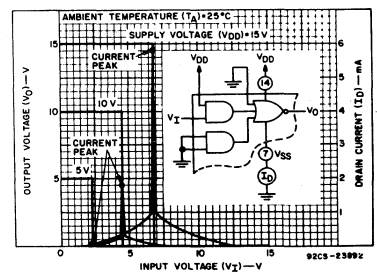


Fig. 1 – Typical voltage and current transfer characteristics.

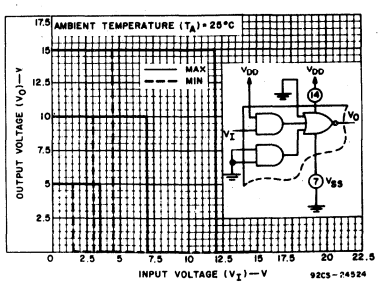


Fig. 2 – Min. and max. voltage transfer characteristics.

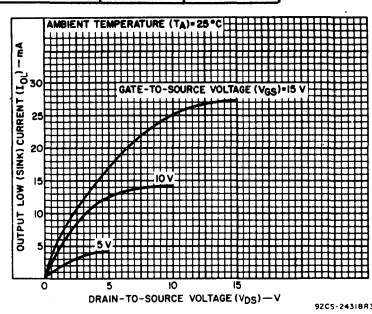


Fig. 3 – Typical output low (sink) current characteristics.

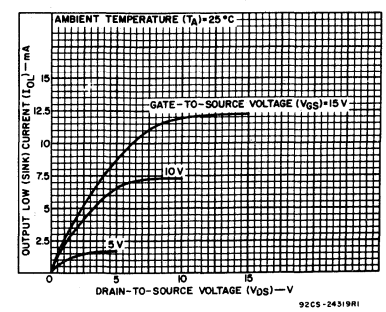


Fig. 4 – Minimum output low (sink) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at −55,+25,+125 Apply to D,K,F,H Pkgs. Values at −40,+25,+85 Apply to E Pkgs. −55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

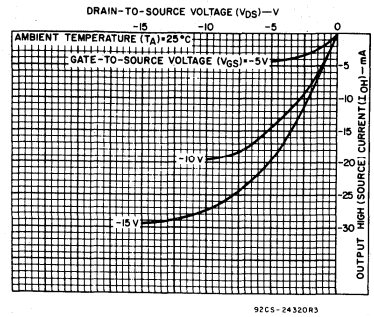


Fig. 5 – Typical output high (source) current characteristics.

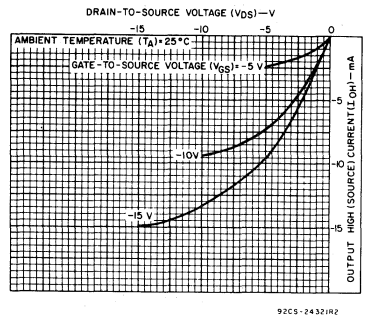


Fig. 6 – Minimum output high (source) current characteristics.

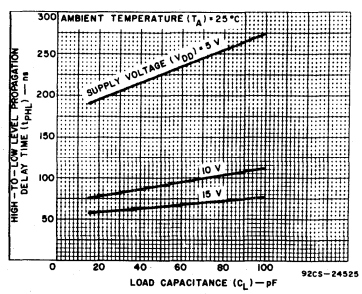


Fig. 7 – Typical data high-to-low level propagation delay time vs. load capacitance.

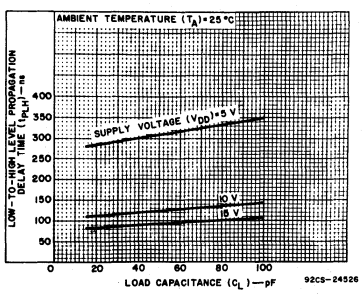


Fig. 8 – Typical data low-to-high level propagation delay time vs. load capacitance.

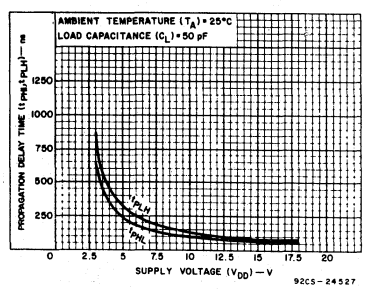


Fig. 9 – Typical data propagation delay time vs. supply voltage.

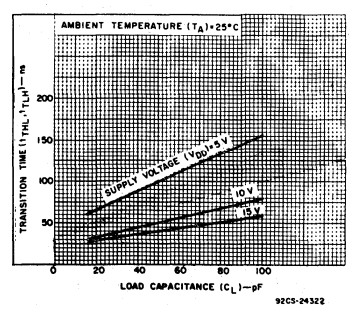


Fig. 10 – Typical transition time vs. load capacitance.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC		CONDITIONS V_{DD} V	LIMITS Typ.	LIMITS Max.	UNITS
Propagation Delay Time (Data): High-to-Low Level,	t_{PHL}	5	225	450	ns
		10	90	180	
		15	65	130	
Low-to-High Level,	t_{PLH}	5	310	620	ns
		10	125	250	
		15	90	180	
Propagation Delay Time (Inhibit): High-to-Low Level,	t_{PHL}	5	150	300	ns
		10	60	120	
		15	40	80	
Low-to-High Level,	t_{PLH}	5	250	500	ns
		10	100	200	
		15	70	140	
Transition Time,	t_{THL}, t_{TLH}	5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance,	C_{IN}	Any Input	5	7.5	pF

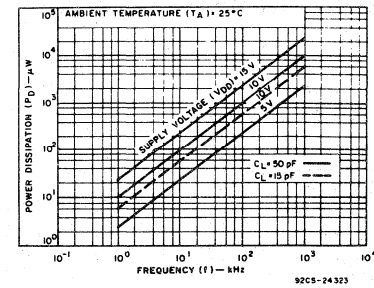


Fig. 11 — Typical power dissipation vs. frequency.

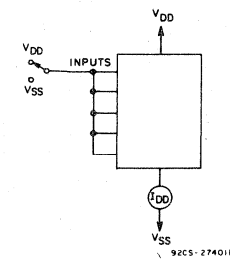


Fig. 12 — Quiescent device current test circuit.

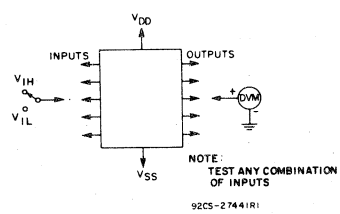


Fig. 13 — Input voltage test circuit.

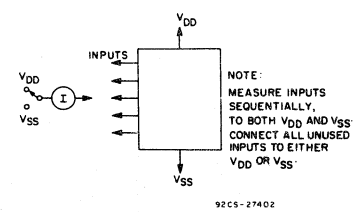


Fig. 14 — Input current test circuit.

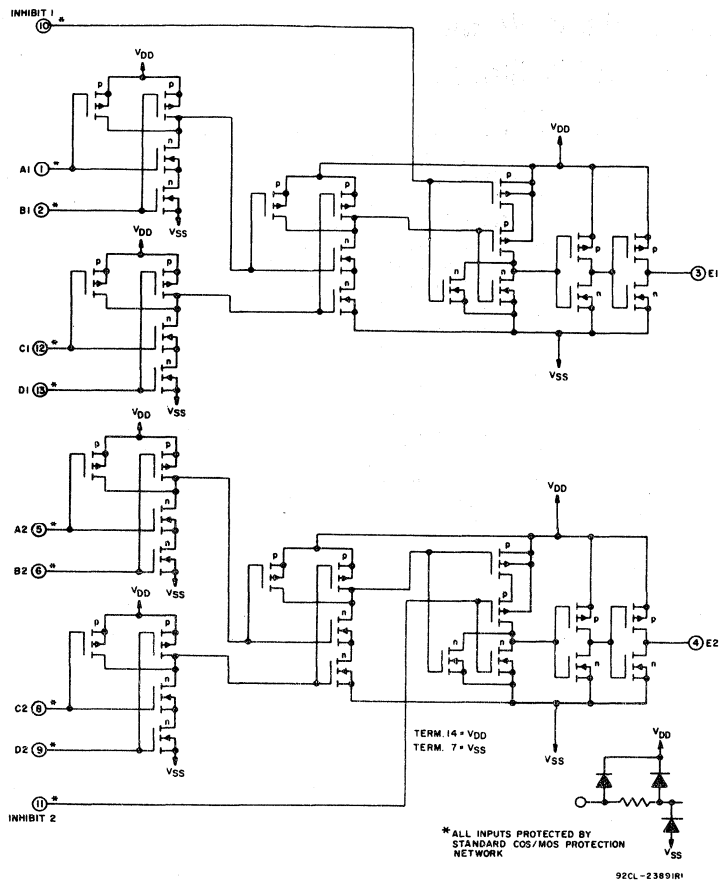
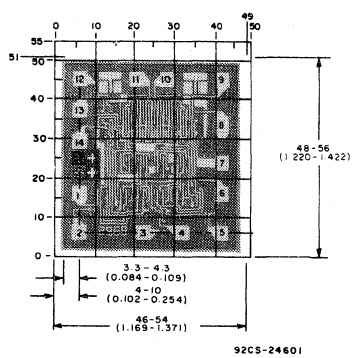


Fig. 15 – CD4085 schematic diagram.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions and Pad Layout for CD4085BH.

COS/MOS Expandable 4-Wide 2-Input AND-OR-INVERT Gate

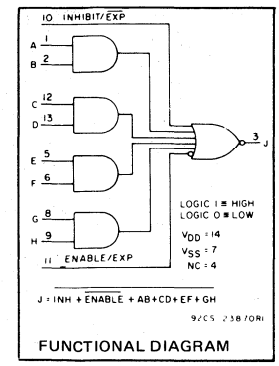
High-Voltage Types (20-Volt Rating)

The RCA-CD4086B contains one 4-wide 2-input AND-OR-INVERT gate with an INHIBIT/$\overline{EXP}$ input and an ENABLE/EXP input. For a 4-wide A-O-I function INHIBIT/$\overline{EXP}$ is tied to V_{SS} and ENABLE/EXP to V_{DD}. See Fig. 2 and its associated explanation for applications where a capability greater than 4-wide is required.

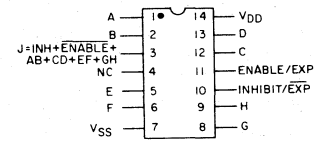
The CD4086B is supplied in 14-lead dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packs (K suffix), and in chip form (H suffix).

Features:

- **Medium-speed operation – t_{PHL} = 90 ns; t_{PLH} = 140 ns (typ.) at 10 V**
- **INHIBIT and ENABLE inputs**
- **Buffered outputs**
- **100% tested for quiescent current at 20 V**
- **Maximum input leakage current of 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (over full package temperature range):**
  - **1 V at V_{DD} = 5 V**
  - **2 V at V_{DD} = 10 V**
  - **2.5 V at V_{DD} = 15 V**
- **Standardized, symmetrical output characteristics**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**



FUNCTIONAL DIAGRAM



Top View

TERMINAL ASSIGNMENT

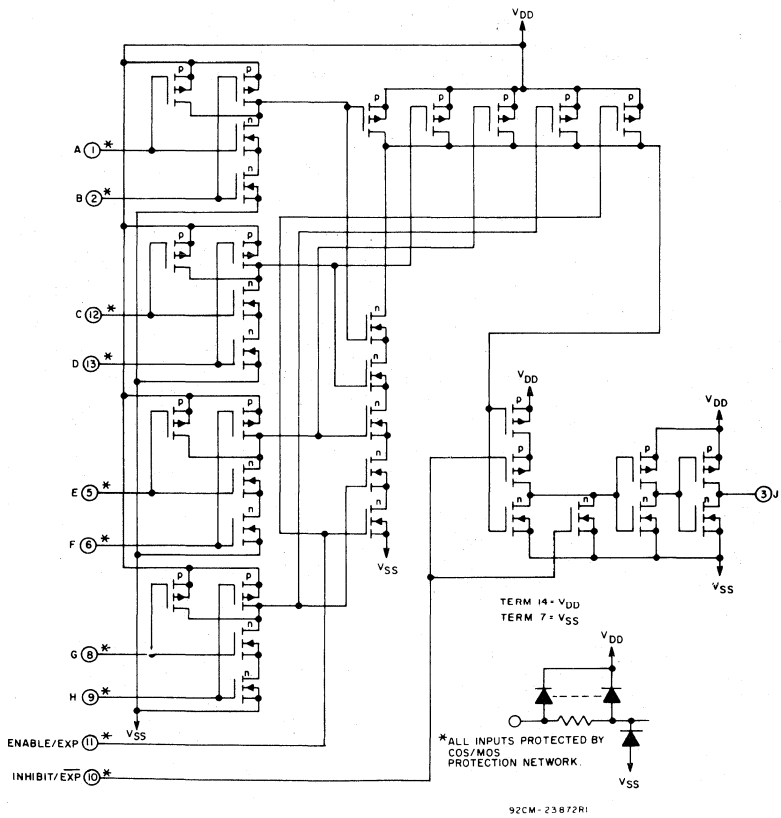


Fig. 1 – CD4086B schematic diagram.

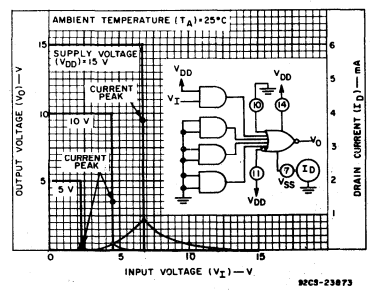


Fig. 2 – Typical voltage and current transfer characteristics.

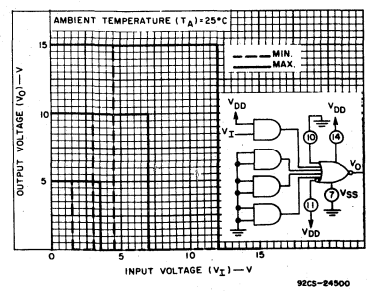


Fig. 3 – Minimum and maximum voltage transfer characteristics.

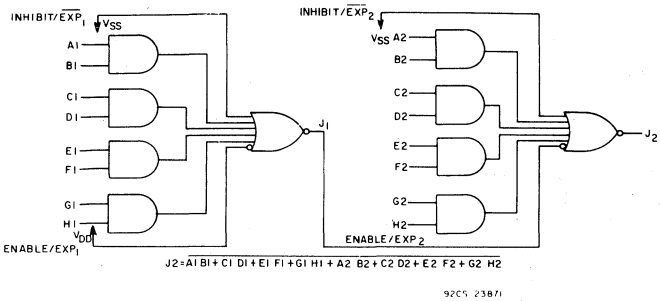


Fig. 4 – Two CD4086B's connected as an 8-wide 2-input A-O-I gate.

Fig. 4 above shows two CD4086's utilized to obtain an 8-wide 2-input A-O-I function. The output (J1) of one CD4086 is fed directly to the ENABLE/EXP2 line of the second CD4086. In a similar fashion, any NAND gate output can be fed directly into the ENABLE/EXP input to obtain a 5-wide A-O-I function. In addition, any AND gate output can be fed directly into the INHIBIT/$\overline{EXP}$ input with the same result.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

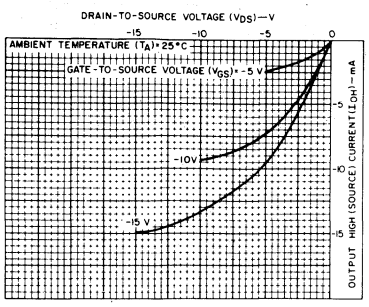


Fig.8 – Minimum output high (source) current characteristics.

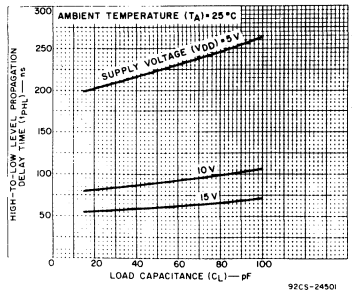


Fig. 9 – Typical DATA or ENABLE high-to-low level propagation delay time vs. load capacitance.

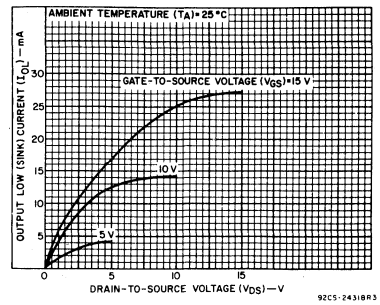


Fig.5 – Typical output low (sink) current characteristics.

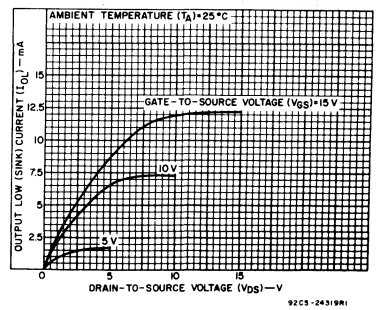


Fig.6 – Minimum output low (sink) current characteristics.

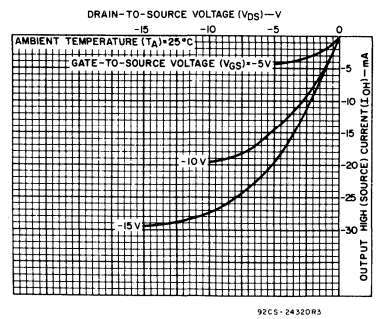


Fig.7 – Typical output high (source) current characteristics.

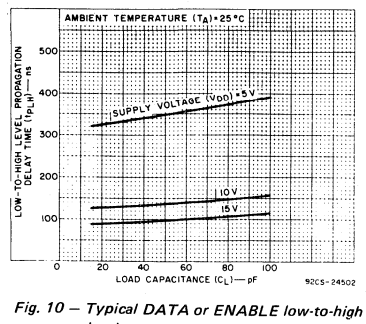


Fig. 10 – Typical DATA or ENABLE low-to-high level propagation delay time vs. load capacitance.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55,+25,+125 Apply to D,K,F,H Pkgs. Values at −40,+25,+85 Apply to E Pkgs.							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

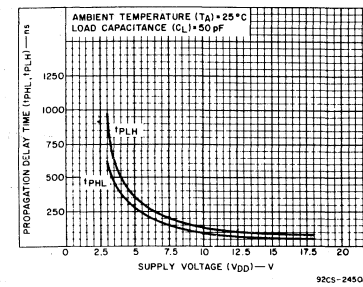


Fig. 11 – Typical DATA or ENABLE propagation delay time vs. supply voltage.

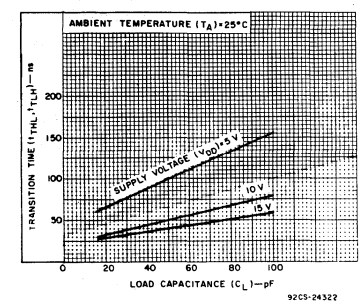


Fig. 12 – Typical transition time vs. load capacitance.

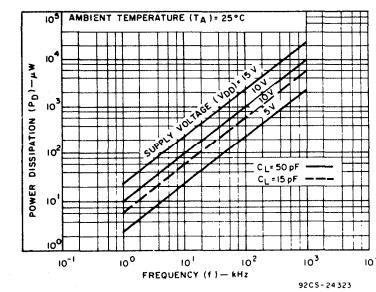


Fig. 13 – Typical power dissipation vs. frequency.

TEST CIRCUITS

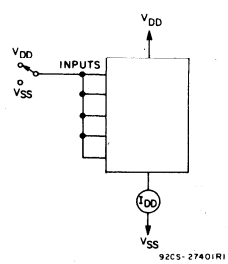


Fig. 14 – Quiescent device current.

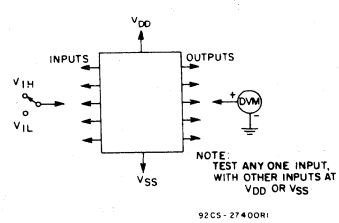


Fig. 15 – Input voltage.

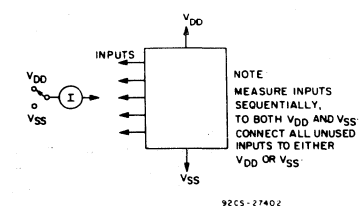


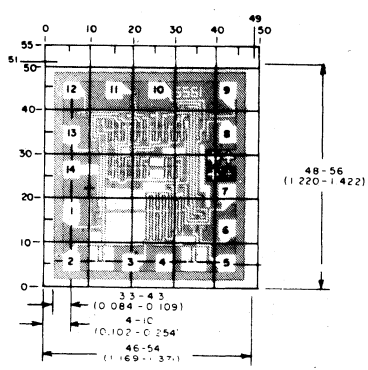
Fig. 16 – Input leakage current.

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	CONDITIONS	LIMITS		UNITS
	V_{DD} (V)	TYP.	MAX.	
Propagation Delay Time (Data): High-to-Low Level, t_{PHL}	5	225	450	ns
	10	90	180	
	15	60	120	
Low-to-High Level, t_{PLH}	5	350	700	ns
	10	140	280	
	15	100	200	
Propagation Delay Time (Inhibit): High-to-Low Level, $t_{PHL(INH)}$	5	150	300	ns
	10	60	120	
	15	40	80	
Low-to-High Level, $t_{PLH(INH)}$	5	250	500	ns
	10	100	200	
	15	70	140	
Transition Time, t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Input Capacitance C_{IN}	Any Input	5	7.5	pF

Dimensions and Pad Layout for the CD4086BH



92CS-24602

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS
Binary Rate Multiplier

High-Voltage Types (20-Volt Rating)

The RCA-CD4089B is a low-power 4-bit digital rate multiplier that provides an output pulse rate that is the clock-input-pulse rate multiplied by 1/16 times the binary input. For example, when the binary input number is 13, there will be 13 output pulses for every 16 input pulses. This device may be used to perform arithmetic operations (add, subtract, divide, raise to a power), solve algebraic and differential equations, generate natural logarithms and trigonometric functions, A/D and D/A conversions, and frequency division.

For words of more than 4 bits, CD4089B devices may be cascaded in two different modes: an Add mode and a Multiply mode (see Figs. 12 and 13). In the Add mode some of the gaps left by the more significant unit at the count of 15 are filled in by the less significant units. For example, when two units are cascaded in the Add mode and programmed to 11 and 13, respectively, the more significant unit will have 11 output pulses for every 16 input pulses and the other unit will have 13 output pulses for every 256 input pulses for a total of

$$\frac{11}{16}+\frac{13}{256}=\frac{189}{256}$$

In the Multiply mode the fraction programmed into the first rate multiplier is multiplied by the fraction programmed into the second multiplier. Thus the output rate will be

$$\frac{11}{16}\times\frac{13}{16}=\frac{143}{256}$$

Features:

- **Cascadable in multiples of 4-bits**
- **Set to "15" input and "15" detect output**
- **100% tested for quiescent current at 20 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Standardized, symmetrical output characteristics**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (full package-temperature range) =**
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

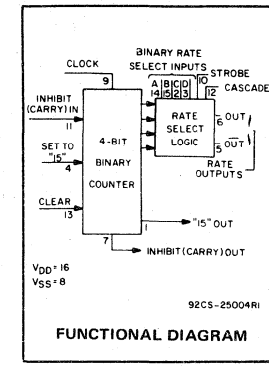
Applications:

- **Numerical control**
- **Instrumentation**
- **Digital filtering**
- **Frequency synthesis**

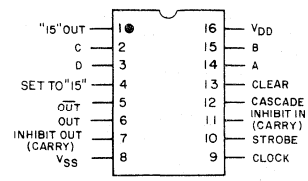
The CD4089B has an internal synchronous 4-bit counter which, together with one of the four binary input bits, produces pulse trains as shown in Fig. 15.

If more than one binary input bit is high, the resulting pulse train is a combination of the separate pulse trains as shown in Fig. 15.

The CD4089B types are supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).



FUNCTIONAL DIAGRAM



TOP VIEW

TERMINAL ASSIGNMENT

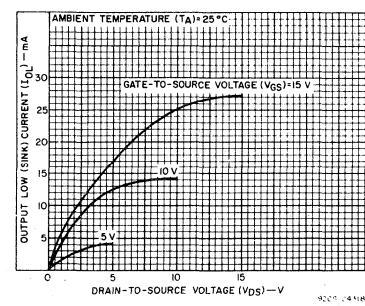


Fig. 1 – Typical output low (sink) current characteristics.

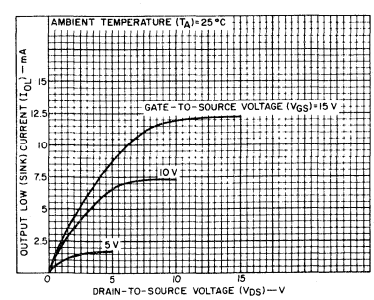


Fig. 2 – Minimum output low (sink) current characteristics.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)			3	18	V
Set or Clear Pulse Width,	t_W	5 10 15	160 90 60	– – –	ns
Clock Pulse Width,	t_W	5 10 15	330 170 100	– – –	ns
Clock Frequency,	f_{CL}	5 10 15	dc	1.2 2.5 3.5	MHz
Clock Rise or Fall Time,	t_{rCL} or t_{fCL}	5, 10,15	–	15	μs
Inhibit In Setup Time,	t_{SU}	5 10 15	100 40 20	– – –	ns
Inhibit In Removal Time,	t_{REM}	5 10 15	240 130 110	– – –	ns
Set Removal Time,	t_{REM}	5 10 15	150 80 50	– – –	ns
Clear Removal Time,	t_{REM}	5 10 15	60 40 30	– – –	ns

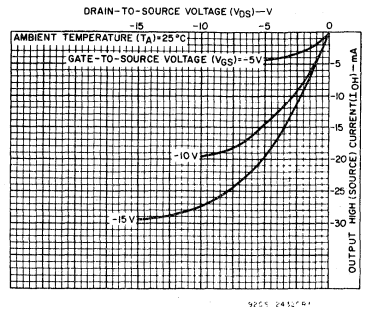


Fig. 3 – Typical output high (source) current characteristics.

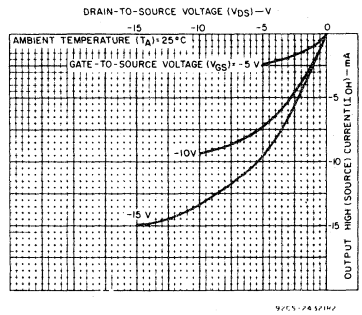


Fig. 4 – Minimum output high (source) current characteristics.

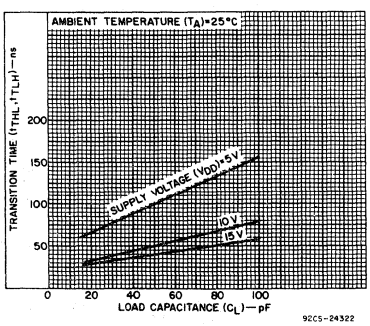


Fig. 5 – Typical transition time as a function of load capacitance.

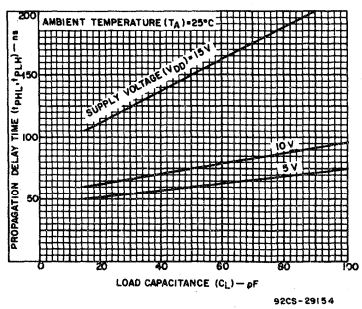


Fig. 6 – Typical propagation delay time as a function of load capacitance (Clock or Strobe to Out).

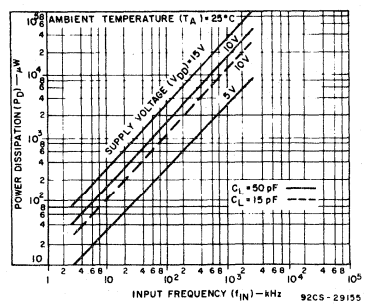


Fig. 7 – Typical dynamic power dissipation as a function of input frequency.

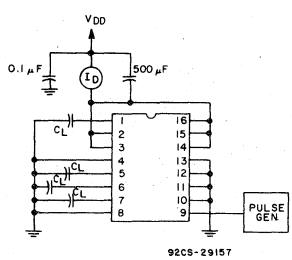


Fig. 8 – Dynamic power dissipation test circuit.

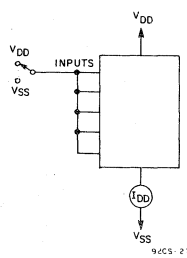


Fig. 9 – Quiescent device current test circuit.

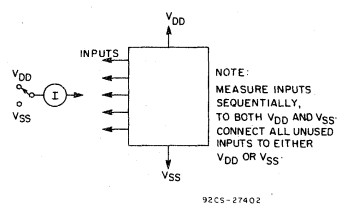


Fig. 10 – Input-current test circuit.

TRUTH TABLE

INPUTS										OUTPUTS			
Number of Pulses or Input Logic Level (0 = Low; 1 = High; X = Don't Care)										Number of Pulses or Output Logic Level (L = Low; H = High)			
D	C	B	A	CLK	INH IN	STR	CAS	CLR ⇂	SET ⇂	OUT	$\overline{OUT}$	INH OUT	"15" OUT
0	0	0	0	16	0	0	0	0	0	L	H	1	1
0	0	0	1	16	0	0	0	0	0	1	1	1	1
0	0	1	0	16	0	0	0	0	0	2	2	1	1
0	0	1	1	16	0	0	0	0	0	3	3	1	1
0	1	0	0	16	0	0	0	0	0	4	4	1	1
0	1	0	1	16	0	0	0	0	0	5	5	1	1
0	1	1	0	16	0	0	0	0	0	6	6	1	1
0	1	1	1	16	0	0	0	0	0	7	7	1	1
1	0	0	0	16	0	0	0	0	0	8	8	1	1
1	0	0	1	16	0	0	0	0	0	9	9	1	1
1	0	1	0	16	0	0	0	0	0	10	10	1	1
1	0	1	1	16	0	0	0	0	0	11	11	1	1
1	1	0	0	16	0	0	0	0	0	12	12	1	1
1	1	0	1	16	0	0	0	0	0	13	13	1	1
1	1	1	0	16	0	0	0	0	0	14	14	1	1
1	1	1	1	16	0	0	0	0	0	15	15	1	1
X	X	X	X	16	1	0	0	0	0	†	†	H	†
X	X	X	X	16	0	1	0	0	0	L	H	1	1
X	X	X	X	16	0	0	1	0	0	H	*	1	1
1	X	X	X	16	0	0	0	1	0	16	16	H	L
0	X	X	X	16	0	0	0	0	1	L	H	H	L
X	X	X	X	16	0	0	0	0	1	L	H	L	H

* Output same as the first 16 lines of this truth table (depending on values of A, B, C, D).

† Depends on internal state of counter.

Clear and Set Inputs should not be high at the same time; device draws increased quiescent current when in this non-valid state.

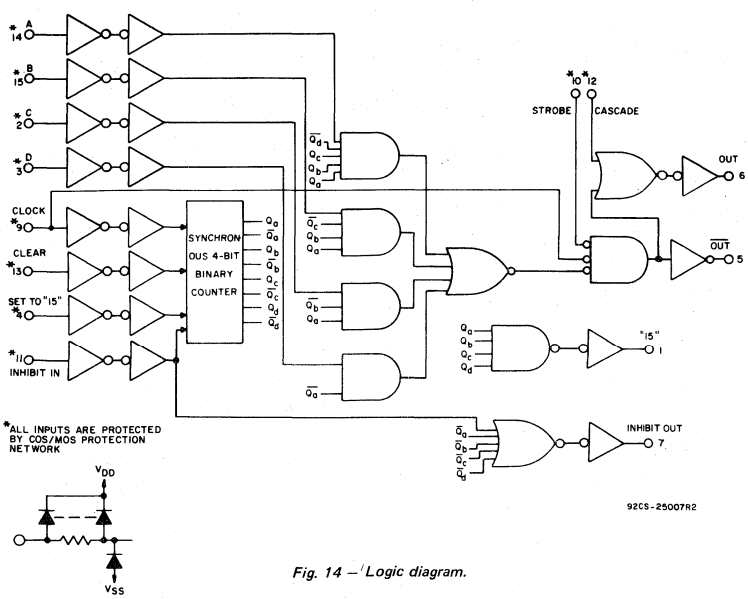


Fig. 14 – Logic diagram.

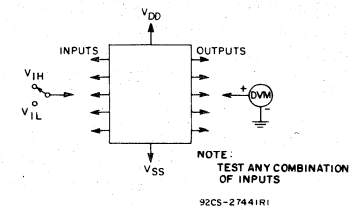


Fig. 11 – Input-voltage test circuit.

APPLICATIONS

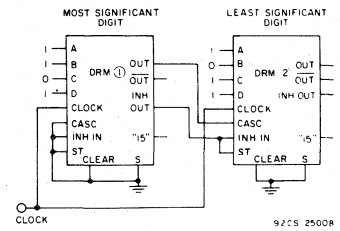


Fig. 12 – Two CD4089B's cascaded in the "Add" mode with a preset number of 189 $\left(\frac{11}{16}+\frac{13}{256}=\frac{189}{256}\right)$.

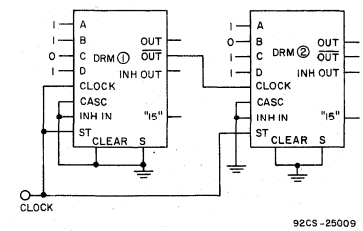


Fig. 13 – Two CS4089B's cascaded in the "Multiply" mode with a preset number of 143 $\left(\frac{11}{16}\times\frac{13}{16}=\frac{143}{256}\right)$.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
									+25		
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

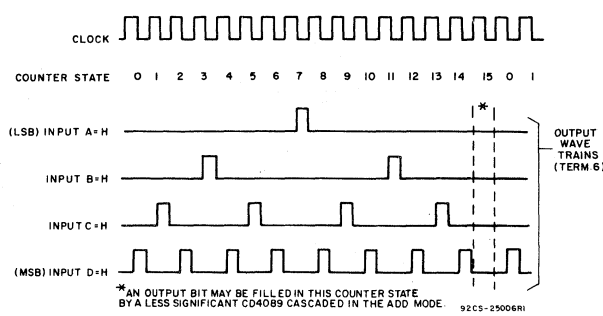


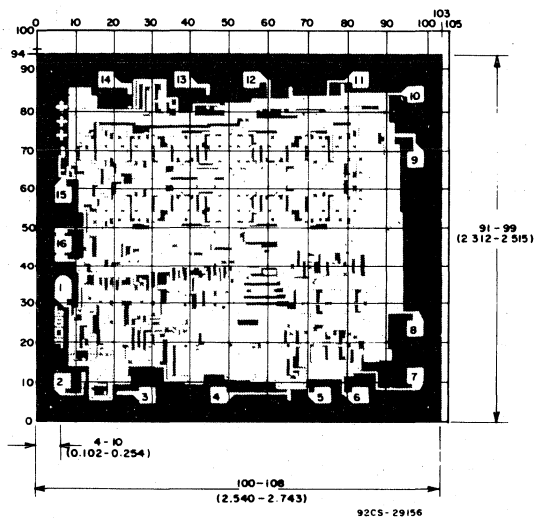
Fig. 15 – Timing diagram.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$;
Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} V	LIMITS Min.	Typ.	Max.	UNITS
Propagation Delay Time, t_{PHL}, t_{PLH} Clock to Out	5	–	110	220	ns
	10	–	55	110	
	15	–	45	90	
Clock or Strobe to Out	5	–	150	300	ns
	10	–	75	150	
	15	–	60	120	
Clock to Inhibit Out High Level to Low Level	5	–	360	720	ns
	10	–	160	320	
	15	–	110	220	
Low Level to High Level	5	–	250	500	ns
	10	–	100	200	
	15	–	75	150	
Clear to Out	5	–	380	760	ns
	10	–	175	350	
	15	–	130	260	
Clock to "9" or "15" Out	5	–	300	600	ns
	10	–	125	250	
	15	–	90	180	
Cascade to Out	5	–	90	180	ns
	10	–	45	90	
	15	–	35	70	
Inhibit In to Inhibit Out	5	–	160	320	ns
	10	–	75	150	
	15	–	55	110	
Set to Out	5	–	330	660	ns
	10	–	150	300	
	15	–	110	220	
Transition Time, t_{THL}, t_{TLH}	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Maximum Clock Frequency, f_{CL}	5	1.2	2.4	–	MHz
	10	2.5	5	–	
	15	3.5	7	–	
Minimum Clock Pulse Width, t_W	5	–	165	330	ns
	10	–	85	170	
	15	–	50	100	
Clock Rise or Fall Time, t_{rCL}, t_{fCL}	5	–	–	15	μs
	10	–	–	15	
	15	–	–	15	
Minimum Set or Clear Pulse Width, t_W	5	–	80	160	ns
	10	–	45	90	
	15	–	30	60	
Minimum Inhibit In Setup Time, t_{SU} High Level to Low Level	5	–	50	100	ns
	10	–	20	40	
	15	–	10	20	
Minimum Inhibit In Removal Time, t_{REM}	5	–	120	240	ns
	10	–	65	130	
	15	–	55	110	

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$ (cont'd)
Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS			UNITS
		V_{DD} V	Min.	Typ.	Max.	
Minimum Set Removal Time, t_{REM}		5	–	75	150	ns
		10	–	40	80	
		15	–	25	50	
Minimum Clear Removal Time, t_{REM}		5	–	30	60	ns
		10	–	20	40	
		15	–	15	30	
Input Capacitance, C_{IN}	Any Input	–	–	5	7.5	pF



Dimensions and Pad Layout for CD4089BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS Quad 2-Input NAND Schmitt Triggers

High-Voltage Types (20 Volt Rating)

The RCA-CD4093B consists of four Schmitt-trigger circuits. Each circuit functions as a two-input NAND gate with Schmitt-trigger action on both inputs. The gate switches at different points for positive- and negative-going signals. The difference between the positive voltage (V_P) and the negative voltage (V_N) is defined as hysteresis voltage (V_H) (see Fig. 2).

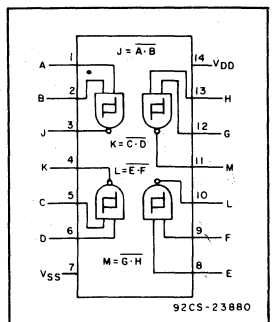
The CD4093B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- Schmitt-trigger action on each input with no external components
- Hysteresis voltage typically 0.9 V at V_{DD} = 5 V and 2.3 V at V_{DD} = 10 V
- Noise immunity greater than 50%
- No limit on input rise and fall times
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range, 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Wave and pulse shapers
- High-noise-environment systems
- Monostable multivibrators
- Astable multivibrators
- NAND logic



FUNCTIONAL DIAGRAM

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	MIN.	MAX.	UNITS
Supply-Voltage Range (T_A = Full Package-Temp. Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

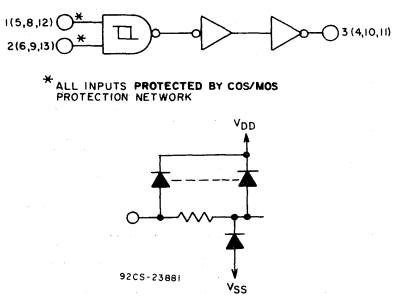


Fig. 1 – Logic diagram—1 of 4 Schmitt triggers.

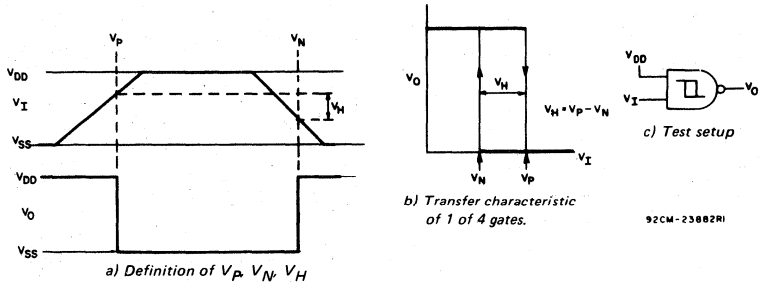


Fig. 2 – Hysteresis definition, characteristic, and test setup.

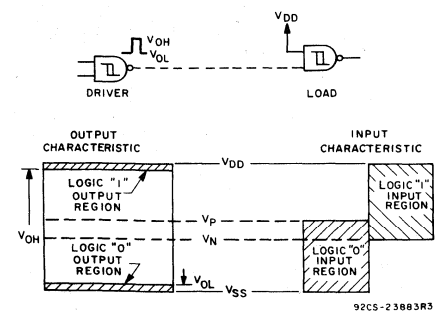


Fig. 3 – Input and output characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D, K, F, H Packages Values at −40, +25, +85 Apply to E Packages							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	MIN.	TYP.	MAX.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Positive Trigger Threshold Voltage V_P Min.	–	a	5	2.2	2.2	2.2	2.2	2.2	2.9	–	V
	–	a	10	4.6	4.6	4.6	4.6	4.6	5.9	–	
	–	a	15	6.8	6.8	6.8	6.8	6.8	8.8	–	
	–	b	5	2.6	2.6	2.6	2.6	2.6	3.3	–	
	–	b	10	5.6	5.6	5.6	5.6	5.6	7	–	
	–	b	15	6.3	6.3	6.3	6.3	6.3	9.4	–	
V_P Max.	–	a	5	3.6	3.6	3.6	3.6	–	2.9	3.6	V
	–	a	10	7.1	7.1	7.1	7.1	–	5.9	7.1	
	–	a	15	10.8	10.8	10.8	10.8	–	8.8	10.8	
	–	b	5	4	4	4	4	–	3.3	4	
	–	b	10	8.2	8.2	8.2	8.2	–	7	8.2	
	–	b	15	12.7	12.7	12.7	12.7	–	9.4	12.7	
Negative Trigger Threshold Voltage V_N Min.	–	a	5	0.9	0.9	0.9	0.9	0.9	1.9	–	V
	–	a	10	2.5	2.5	2.5	2.5	2.5	3.9	–	
	–	a	15	4	4	4	4	4	5.8	–	
	–	b	5	1.4	1.4	1.4	1.4	1.4	2.3	–	
	–	b	10	3.4	3.4	3.4	3.4	3.4	5.1	–	
	–	b	15	4.8	4.8	4.8	4.8	4.8	7.3	–	
V_N Max.	–	a	5	2.8	2.8	2.8	2.8	–	1.9	2.8	V
	–	a	10	5.2	5.2	5.2	5.2	–	3.9	5.2	
	–	a	15	7.4	7.4	7.4	7.4	–	5.8	7.4	
	–	b	5	3.2	3.2	3.2	3.2	–	2.3	3.2	
	–	b	10	6.6	6.6	6.6	6.6	–	5.1	6.6	
	–	b	15	9.6	9.6	9.6	9.6	–	7.3	9.6	
Hysteresis Voltage V_H Min.	–	a	5	0.3	0.3	0.3	0.3	0.3	0.9	–	V
	–	a	10	1.2	1.2	1.2	1.2	1.2	2.3	–	
	–	a	15	1.6	1.6	1.6	1.6	1.6	3.5	–	
	–	b	5	0.3	0.3	0.3	0.3	0.3	0.9	–	
	–	b	10	1.2	1.2	1.2	1.2	1.2	2.3	–	
	–	b	15	1.6	1.6	1.6	1.6	1.6	3.5	–	
V_H Max.	–	a	5	1.6	1.6	1.6	1.6	–	0.9	1.6	V
	–	a	10	3.4	3.4	3.4	3.4	–	2.3	3.4	
	–	a	15	5	5	5	5	–	3.5	5	
	–	b	5	1.6	1.6	1.6	1.6	–	0.9	1.6	
	–	b	10	3.4	3.4	3.4	3.4	–	2.3	3.4	
	–	b	15	5	5	5	5	–	3.5	5	

[a] Input on terminals 1,5,8,12 or 2,6,9,13; other inputs to V_{DD}.

[b] Input on terminals 1 and 2, 5 and 6,8 and 9, or 12 and 13; other inputs to V_{DD}.

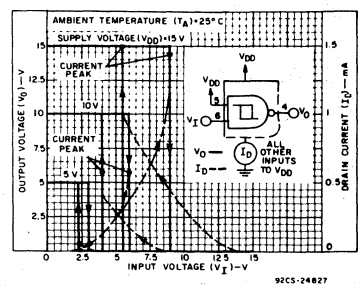


Fig. 4 – Typical current and voltage transfer characteristics.

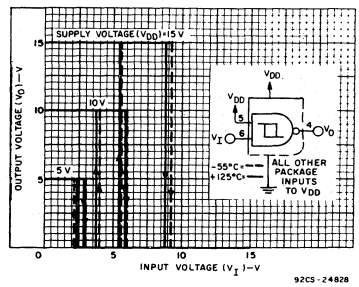


Fig. 5 – Typical voltage transfer characteristics as a function of temperature.

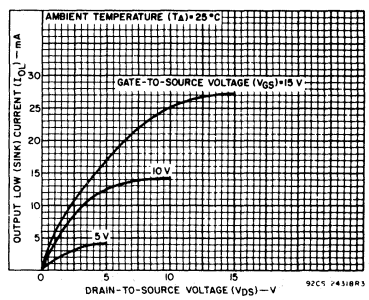


Fig. 6 – Typical output low (sink) current characteristics.

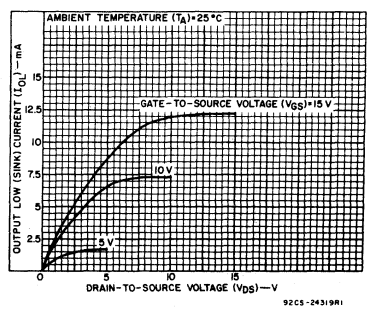


Fig. 7 – Minimum output low (sink) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS (CONT'D)

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURE (°C) Values at −55, +25, +125 Apply to D, K, F, H Packages Values at −40, +25, +85 Apply to E Packages							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 MIN.	+25 TYP.	+25 MAX.	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95		–	
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

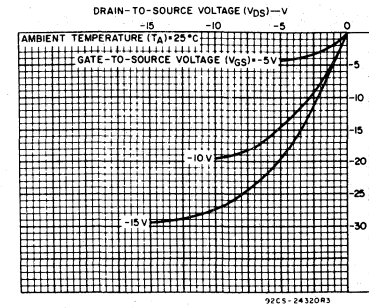


Fig. 8 – Typical output high (source) current characteristics.

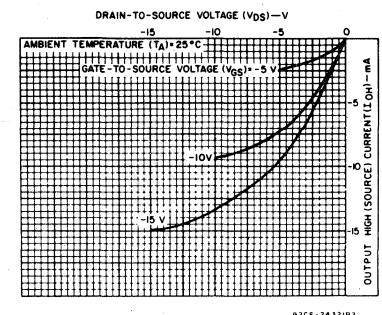


Fig. 9 – Minimum output high (source) current characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		V_{DD} VOLTS	TYP.	MAX.	
Propagation Delay Time: t_{PHL}, t_{PLH}		5	300	600	ns
		10	150	300	
		15	120	240	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input		5	7.5	pF

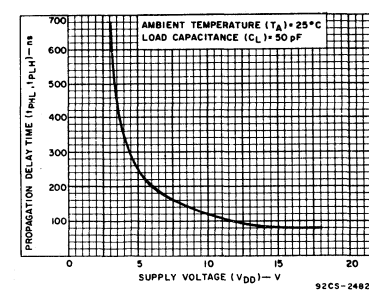


Fig. 10 – Typical propagation delay time vs. supply voltage.

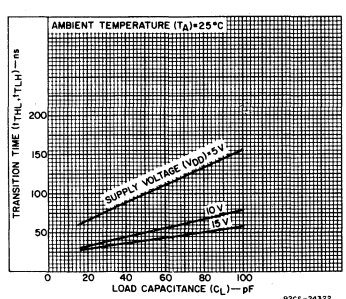


Fig. 11 – Typical transition time vs. load capacitance.

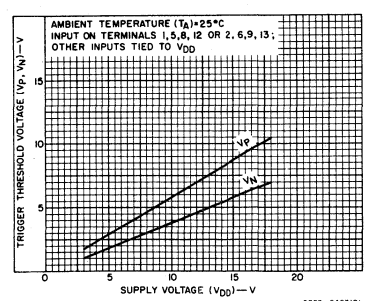


Fig. 12 – Typical trigger threshold voltage vs. V_{DD}.

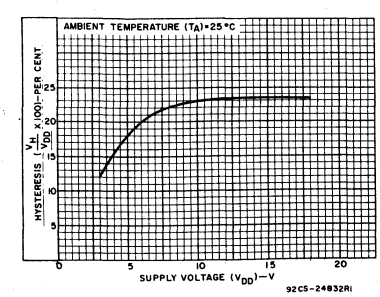


Fig. 13 – Typical per cent hysteresis vs. supply voltage.

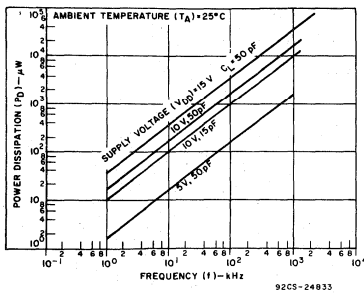


Fig. 14 – Typical power dissipation vs. frequency characteristics.

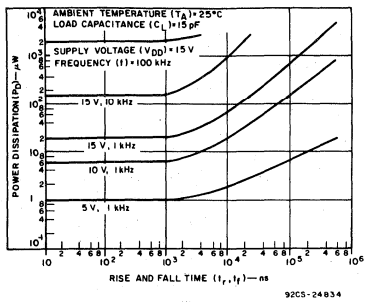


Fig. 15 – Typical power dissipation vs. rise and fall times.

APPLICATIONS

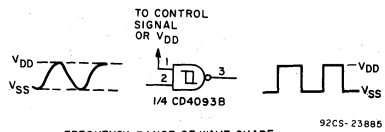


Fig. 16 – Wave shaper.

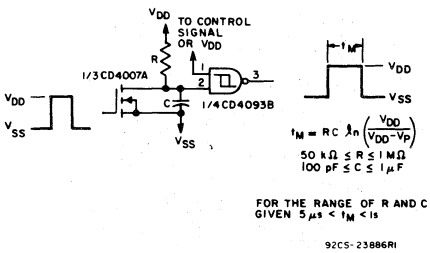


Fig. 17 – Monostable multivibrator.

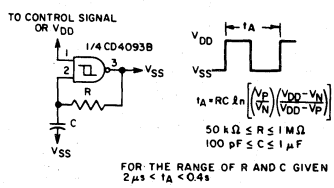


Fig. 18 – Astable multivibrator.

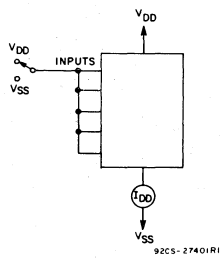


Fig. 19 – Quiescent device current test circuit.

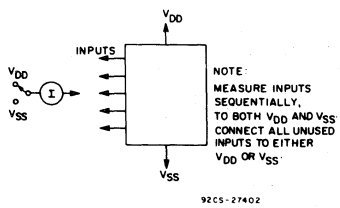
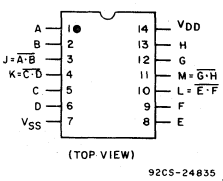
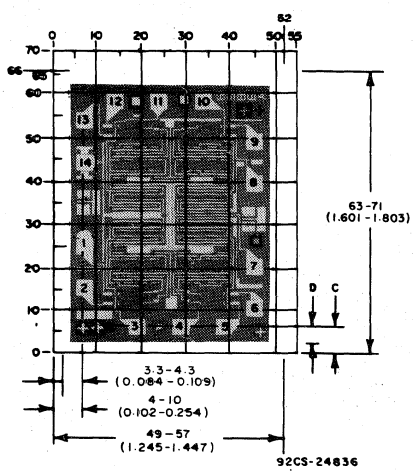


Fig. 20 – Input current test circuit.



TERMINAL ASSIGNMENT



Dimensions and Pad Layout for CD4093BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS 8-Stage Shift-and-Store Bus Register

High-Voltage Types (20-Volt Rating)

The RCA-CD4094B is an 8-stage serial shift register having a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive clock transitions. The data in each shift register stage is transferred to the storage register when the STROBE input is high. Data in the storage register appears at the outputs whenever the OUTPUT-ENABLE signal is high.

Two serial outputs are available for cascading a number of CD4094B devices. Data is available at the Q_S serial output terminal on positive clock edges to allow for high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information, available at the Q'_S terminal on the next negative clock edge, provides a means for cascading CD4094B devices when the clock rise time is slow.

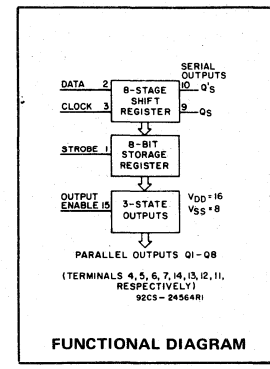
The CD4094B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- 3-state parallel outputs for connection to common bus
- Separate serial outputs synchronous to both positive and negative clock edges for cascading
- Medium speed operation – 5 MHz at 10 V (typ.)
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package temperature range): 1 V at V_{DD} = 5 V, 2 V at V_{DD} = 10 V, 2.5 V at V_{DD} = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Serial-to-parallel data conversion
- Remote control holding register
- Dual-rank shift, hold, and bus applications



FUNCTIONAL DIAGRAM

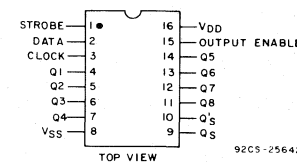


Fig. 1 – Terminal assignment.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . –0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = –40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
PACKAGE TYPE E . . . . . –40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

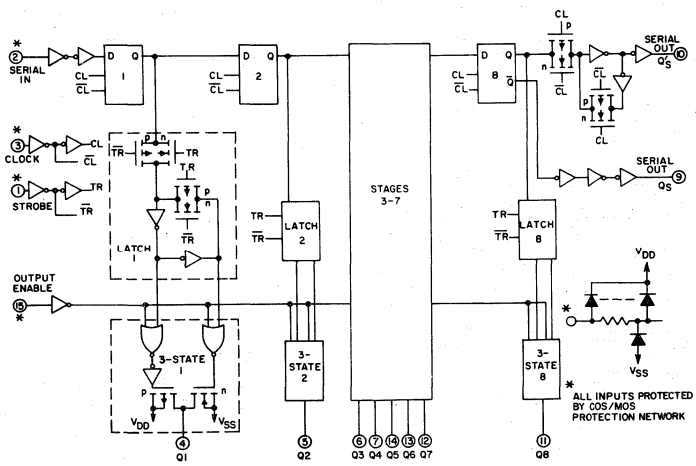


Fig. 2 – CD4094B Logic diagram.

TRUTH TABLE

CL▲	Output Enable	Strobe	Data	Parallel Outputs Q1	Parallel Outputs QN	Serial Outputs QS*	Serial Outputs Q'S
⌐	0	X	X	OC	OC	Q7	NC
⌐	0	X	X	OC	OC	NC	Q7
⌐	1	0	X	NC	NC	Q7	NC
⌐	1	1	0	0	Q_{N-1}	Q7	NC
⌐	1	1	1	1	Q_{N-1}	Q7	NC
⌐	1	1	1	NC	NC	NC	Q7

▲ = Level Change
X = Don't Care
NC = No Change
OC = Open Circuit
Logic 1 ≡ High
Logic 0 ≡ Low

* At the positive clock edge information in the 7th shift register stage is transferred to the 8th register stage and the Q_S output.

CD4094B Types

RECOMMENDED OPERATING CONDITIONS *at T_A = 25°C, Except as Noted.*
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)		3	18	V
Data Setup Time, t_S	5 10 15	125 55 35	– – –	ns
Clock Pulse Width, t_W	5 10 15	200 100 83	– – –	ns
Clock Input Frequency, f_{CL}	5 10 15	dc	1.25 2.5 3	MHz
Clock Input Rise or Fall time, t_rCL, t_fCL:*	5 10 15	–	15 5 5	μs
Strobe Pulse Width, t_W	5 10 15	200 80 70	– – –	ns

*If more than one unit is cascaded t_fCL (for Q_S only) should be made less than or equal to the sum of the fixed propagation delay at 50 pF and the transition time of the output driving stage for the estimated capacitive load.

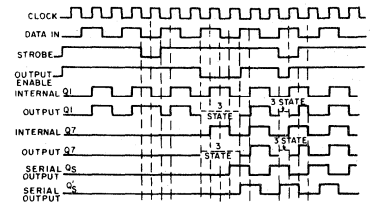


Fig. 3 – Timing diagram.

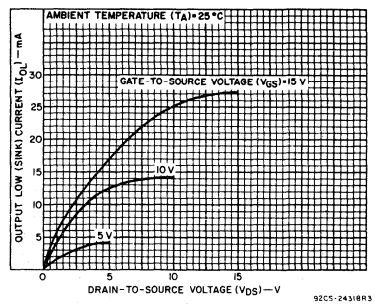


Fig. 4 – Typical output low (sink) current characteristics.

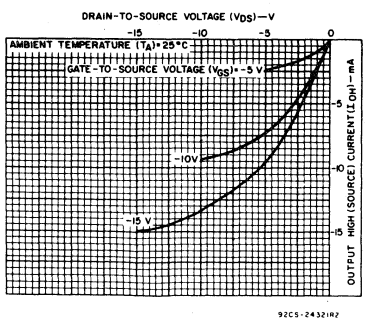


Fig. 5 – Minimum output low (sink) current characteristics.

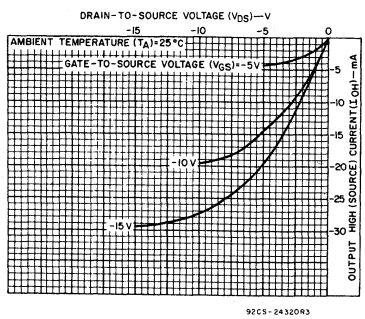


Fig. 6 – Typical output high (source) current characteristics.

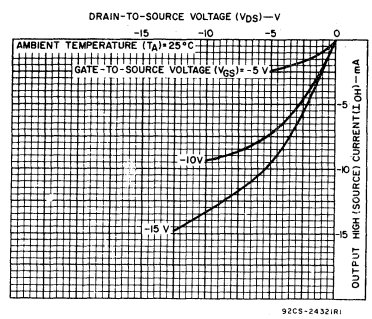


Fig. 7 – Minimum output high (source) current characteristics.

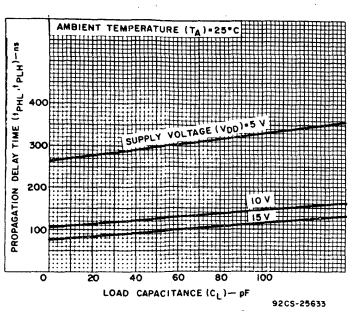


Fig. 8 – Clock-to-serial output Q_S propagation delay vs C_L.

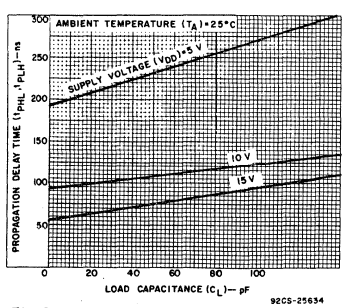


Fig. 9 – Clock-to-serial output Q'_S propagation delay vs C_L.

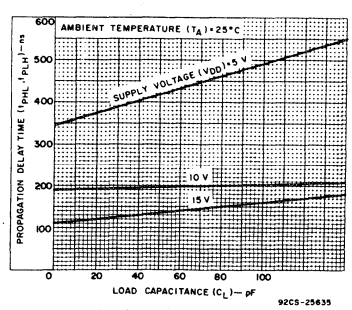


Fig. 10 – Clock-to-parallel output propagation delay vs C_L.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
									+25		
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	-	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA
3-State Output Leakage Current I_{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	–	$\pm 10^{-4}$	±0.4	μA

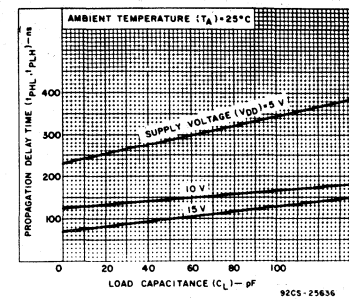


Fig. 11 – Strobe-to-parallel output propagation delay vs C_L.

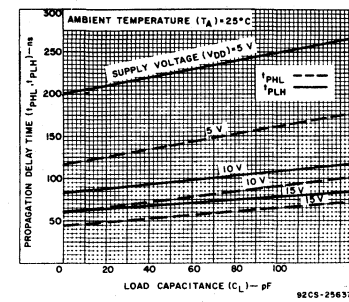


Fig. 12 – Output enable-to-parallel output propagation delay vs C_L.

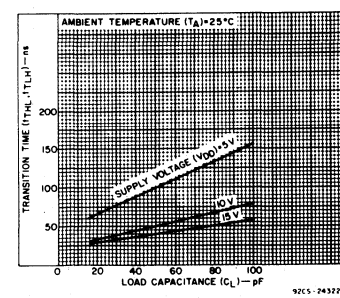


Fig. 13 – Typical transition time vs. load capacitance.

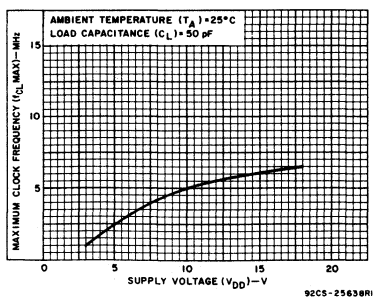


Fig. 14 – Typical maximum-clock-frequency vs. supply voltage.

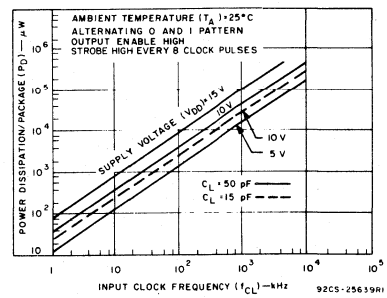


Fig. 15 – Dynamic power dissipation vs input clock frequency.

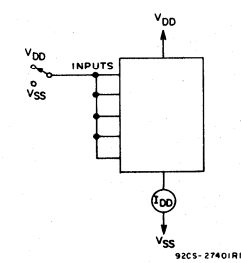


Fig. 16 – Quiescent device current test circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A=25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS			UNITS
		MIN.	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH} Clock to Serial Output Q_S	5	–	300	600	ns
	10	–	125	250	
	15	–	95	190	
Clock to Serial Output Q'_S	5	–	230	460	ns
	10	–	110	220	
	15	–	75	150	
Clock to Parallel Output	5	–	420	840	ns
	10	–	195	390	
	15	–	135	270	
Strobe to Parallel Output	5	–	290	580	ns
	10	–	145	290	
	15	–	100	200	
Output Enable to Parallel Output: High-to-Low, t_{PHL}	5	–	140	280	ns
	10	–	75	150	
	15	–	55	110	
Low-to-High, t_{PLH}	5	–	225	450	ns
	10	–	95	190	
	15	–	70	140	
Minimum Strobe Pulse Width, t_W	5	–	100	200	ns
	10	–	40	80	
	15	–	35	70	
Minimum Clock Pulse Width, t_W	5	–	100	200	ns
	10	–	50	100	
	15	–	40	83	
Minimum Data Setup Time, t_S	5	–	60	125	ns
	10	–	30	55	
	15	–	20	35	
Transition Time; t_{THL}, t_{TLH}	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Maximum Clock Input Rise or Fall Time, t_rCL, t_fCL	5	15	–	–	μs
	10	5	–	–	
	15	5	–	–	
Maximum Clock Input Frequency, f_{CL}	5	1.25	2.5	–	MHz
	10	2.5	5	–	
	15	3	6	–	
Input Capacitance C_{IN} (Any Input)	–	–	5	7.5	pF

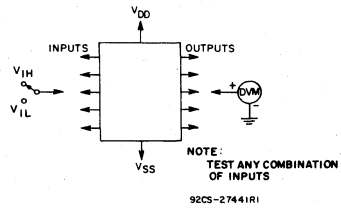


Fig. 17 – Input voltage test circuit.

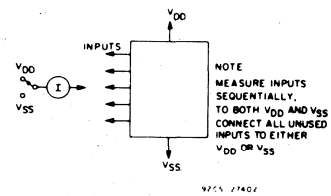


Fig. 18 – Input current test circuit.

TYPICAL APPLICATION

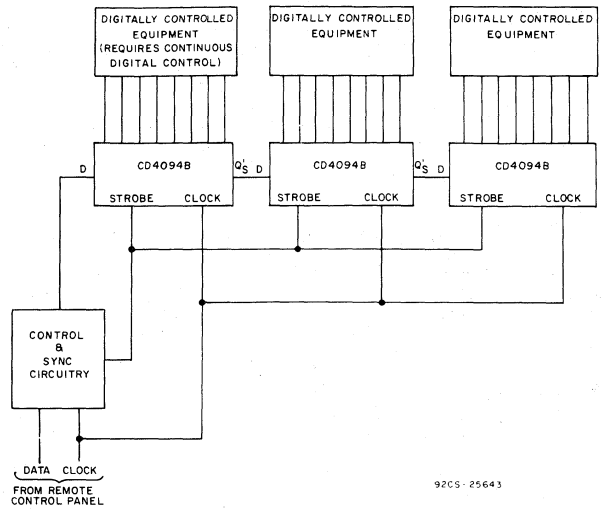
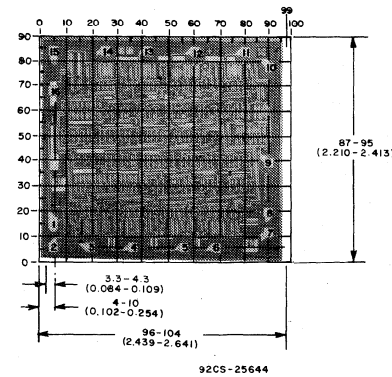


Fig. 19 – Remote control holding register.

Dimensions and Pad Layout for CD4094B Chip.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

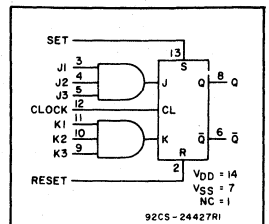
The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.



COS/MOS Gated J-K Master-Slave Flip-Flops

With Set-Reset Capability
High-Voltage Types (20-Volt Rating)

CD4095B Non-Inverting J and K Inputs
CD4096B Inverting and Non-Inverting J and K Inputs



CD4095B
Functional Diagram

The RCA-CD4095B and CD4096B are J-K Master-Slave Flip-Flops featuring separate AND gating of multiple J and K inputs. The gated J-K inputs control transfer of information into the master section during clocked operation. Information on the J-K inputs is transferred to the Q and $\overline{Q}$ outputs on the positive edge of the clock pulse. SET and RESET inputs (active high) are provided for asynchronous operation.

The CD4095B and CD4096B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- **16 MHz toggle rate (typ.) at $V_{DD} - V_{SS} = 10$ V**
- **Gated inputs**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin over full package-temperature range: 1 V at V_{DD} = 5 V, 2 V at V_{DD} = 10 V, 2.5 V at V_{DD} = 15 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Standardized, symmetrical output characteristics**

Applications:

- **Registers**
- **Counters**
- **Control circuits**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

TRUTH TABLES
SYNCHRONOUS OPERATION (S=0 R=0)

Inputs Before Positive Clock Transition		Outputs After Positive Clock Transition	
J*	K*	Q	$\overline{Q}$
0	0	No Change	
0	1	0	1
1	0	1	0
1	1	Toggles	

* For CD4095B: J = J1 · J2 · J3; K = K1 · K2 · K3
For CD4096B: J = J1 · J2 · $\overline{J3}$; K = K1 · K2 · $\overline{K3}$

ASYNCHRONOUS OPERATION (J and K - DON'T CARE)

S	R	Q	$\overline{Q}$
0	0	No Change	
0	1	0	1
1	0	1	0
1	1	0	0

0 = V_{SS}, 1 = V_{DD}

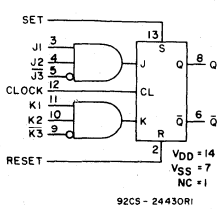


Fig. 1 – CD4096B Functional Diagram.

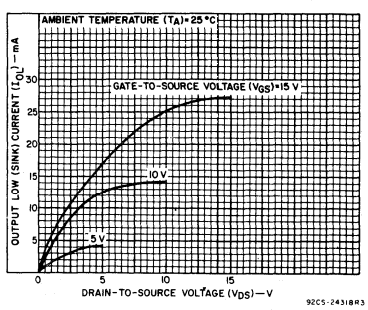


Fig.2 – Typical output low (sink) current characteristics.

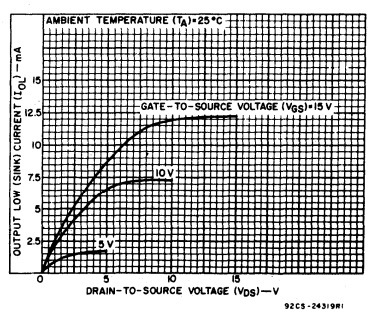


Fig.3 – Minimum output low (sink) current characteristics.

RECOMMENDED OPERATING CONDITIONS at T_A = 25° C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	18	V
Data Setup Time, t_S	5	400	–	ns
	10	160	–	
	15	100	–	
Clock Pulse Width, t_W	5	140	–	ns
	10	60	–	
	15	40	–	
Clock Input Frequency, f_{CL}	5	dc	3.5	MHz
	10		8	
	15		12	
Clock Rise and Fall Time, t_rCL, t_fCL:	5	–	15	μs
	10	–	5	
	15	–	5	
Set or Reset Pulse Width, t_W	5	200	–	ns
	10	100	–	
	15	50	–	

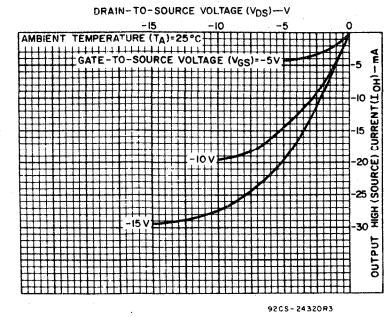


Fig.4 – Typical output high (source) current characteristics.

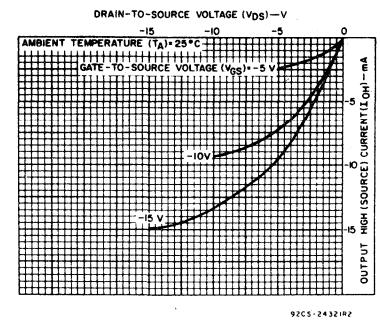


Fig.5 – Minimum output high (source) current characteristics.

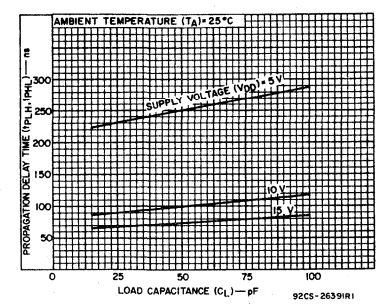


Fig.6 – Typical propagation delay time vs. load capacitance.

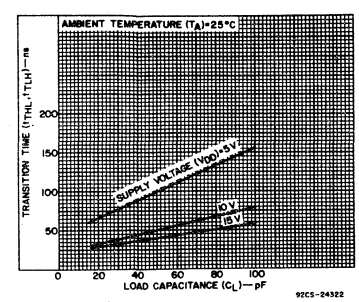


Fig.7 – Typical transition time vs. load capacitance.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	CONDITIONS V_{IN} (V)	CONDITIONS V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D,K,F,H Packages Values at –40, +25, +85 Apply to E Package –55	–40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current, I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5, 13.5	–	15	4				–	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5, 13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		V_{DD} (V)	MIN.	TYP.	MAX.	
Propagation Delay Time: t_{PHL}, t_{PLH}		5	–	250	500	ns
		10	–	100	200	
		15	–	75	150	
Set or Reset		5	–	150	300	
		10	–	75	150	
		15	–	50	100	
Transition Time, t_{THL}, t_{TLH}		5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Maximum Clock Input Frequency, (f_{CL})		5	3.5	7	–	MHz
		10	8	16	–	
		15	12	24	–	
Minimum Clock Pulse Width, t_W		5	–	70	140	ns
		10	–	30	60	
		15	–	20	40	
Clock Input Rise or Fall Time, t_{rcl}, t_{rcf}		5	–	–	15	μs
		10	–	–	5	
		15	–	–	5	
Minimum Set or Reset Pulse Width, t_W		5	–	100	200	ns
		10	–	50	100	
		15	–	25	50	
Minimum Data Setup Time, t_S		5	–	200	400	ns
		10	–	80	160	
		15	–	50	100	
Input Capacitance, C_{IN}	Any Input	–	–	5	7.5	pF

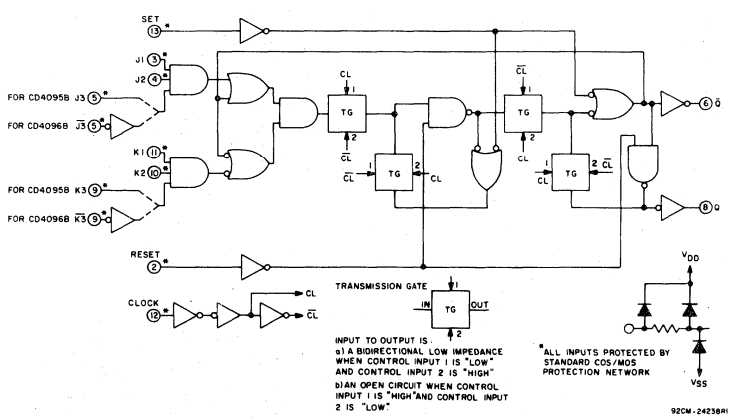


Fig.11 – CD4095B and CD4096B logic diagram.

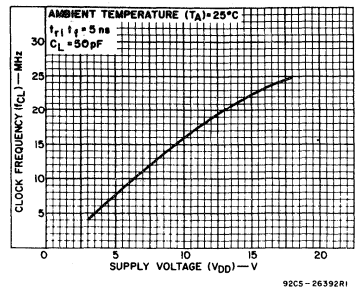


Fig.8 – Typical clock frequency vs. supply voltage (toggle mode–see Fig. 16).

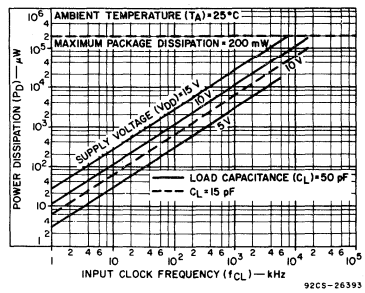


Fig. 9 – Typical power dissipation vs. input clock frequency.

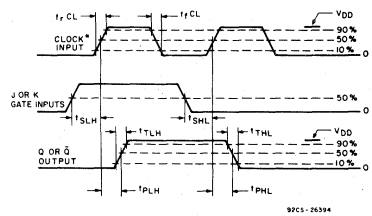


Fig.10 – Propagation delay, transition, and setup-time waveforms.

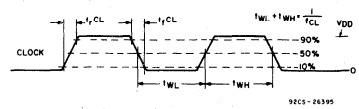


Fig.12 – Clock pulse rise and fall time waveforms.

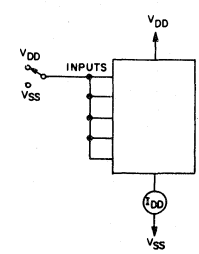


Fig.13 – Quiescent device current test circuit.

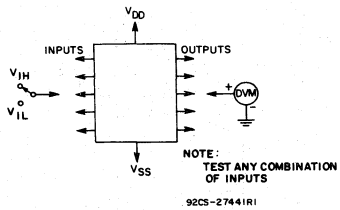


Fig. 14 – Input voltage test circuit.

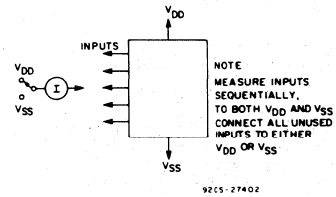


Fig. 15 – Input leakage current test circuit.

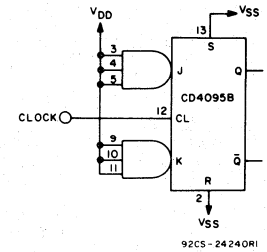


Fig. 16 – CD4095B connected in toggle mode.

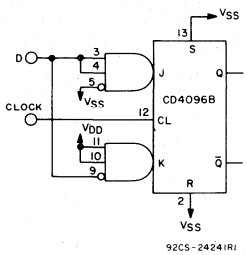


Fig. 17 – CD4096B connected as a "D" type flip-flop.

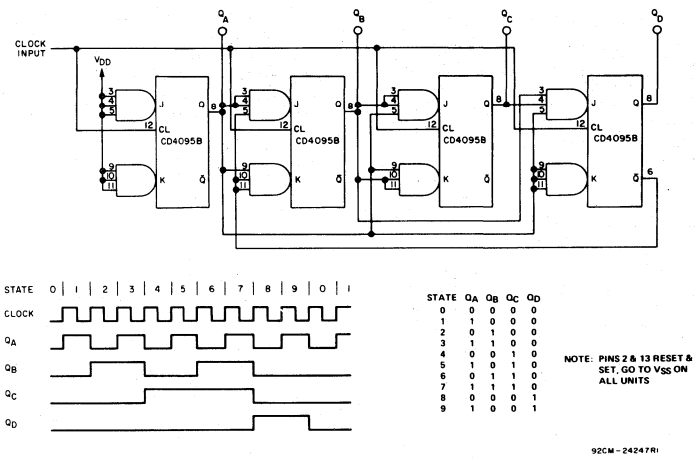
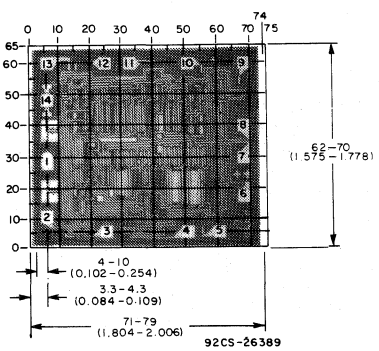


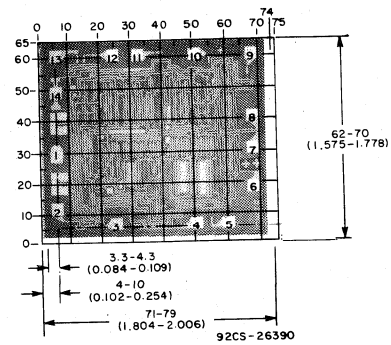
Fig. 18 – Synchronous binary divide-by-ten counter.

DIMENSIONS AND PAD LAYOUT FOR CD4095B AND CD4096B



CD4095BH

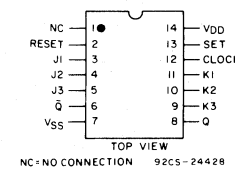
The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.



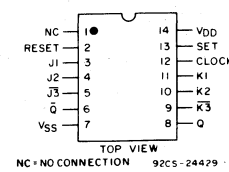
CD4096BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

TERMINAL ASSIGNMENTS



CD4095B



CD4096B

COS/MOS Dual Monostable Multivibrator

High-Voltage Types (20-Volt Rating)

The RCA-CD4098B dual monostable multivibrator provides stable retriggerable/resettable one-shot operation for any fixed-voltage timing application.

An external resistor (R_X) and an external capacitor (C_X) control the timing for the circuit. Adjustment of R_X and C_X provides a wide range of output pulse widths from the Q and $\overline{Q}$ terminals. The time delay from trigger input to output transition (trigger propagation delay) and the time delay from reset input to output transition (reset propagation delay) are independent of R_X and C_X.

Leading-edge-triggering (+TR) and trailing-edge-triggering (−TR) inputs are provided for triggering from either edge of an input pulse. An unused +TR input should be tied to V_{SS}. An unused −TR input should be tied to V_{DD}. A RESET (on low level) is provided for immediate termination of the output pulse or to prevent output pulses when power is turned on. An unused RESET input should be tied to V_{DD}. However, if an entire section of the CD4098B is not used, its RESET should be tied to V_{SS}. See Table I.

In normal operation the circuit triggers (extends the output pulse one period) on the application of each new trigger pulse. For operation in the non-retriggerable mode, $\overline{Q}$ is connected to −TR when leading-edge triggering (+TR) is used or Q is connected to +TR when trailing-edge triggering (−TR) is used.

The time period (T) for this multivibrator can be approximated by: $T_X = \frac{1}{2} R_X C_X$ for $C_X \geq 0.01\ \mu F$. Time periods as a function of R_X for values of C_X and V_{DD} are given in Fig. 8. Values of T vary from unit to unit and as a function of voltage, temperature, and $R_X C_X$.

The minimum value of external resistance, R_X, is 5 kΩ. The maximum value of external capacitance, C_X, is 100 μF. Fig. 9 shows time periods as a function of C_X for values of R_X and V_{DD}.

The output pulse width has variations of ±2.5% typically, over the temperature range of −55°C to 125°C for C_X=1000 pF and R_X=100 kΩ.

For power supply variations of ±5%, the output pulse width has variations of ±0.5% typically, for V_{DD}=10 V and 15 V and ±1% typically, for V_{DD}=5 V at C_X=1000 pF and R_X=5 kΩ.

The CD4098B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

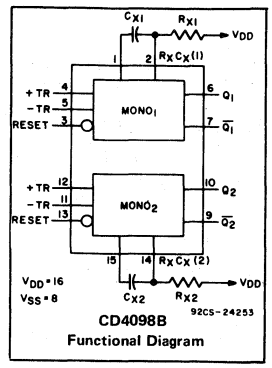
The CD4098B is similar to type MC14528.

Features:

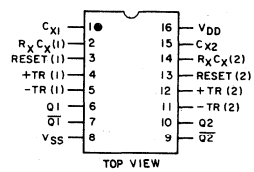
- **Retriggerable/resettable capability**
- **Trigger and reset propagation delays independent of R_X, C_X**
- **Triggering from leading or trailing edge**
- **Q and $\overline{Q}$ buffered outputs available**
- **Separate resets**
- **Wide range of output-pulse widths**
- **100% tested for maximum quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (full package-temperature range): 1 V at V_{DD}= 5 V; 2 V at V_{DD}=10 V; 2.5 V at V_{DD}=15 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Standardized, symmetrical output characteristics**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices."**

Applications:

- **Pulse delay and timing**
- **Pulse shaping**
- **Astable multivibrator**



CD4098B
Functional Diagram



TERMINALS 1, 8, 15 ARE ELECTRICALLY CONNECTED INTERNALLY

92CS-24848RI

TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} V	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	–	3	18	V
Trigger Pulse Width t_W(TR)	5 10 15	140 60 40	– – –	ns
Reset Pulse Width t_W(R) (This is a function of C_X)	–	See Dynamic Char. Chart and Fig. 11		–
Trigger Rise or Fall Time t_r(TR), t_f(TR)	5 - 15	–	100	μs

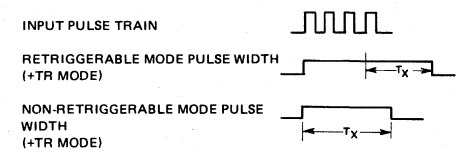
TABLE I

CD4098B FUNCTIONAL TERMINAL CONNECTIONS

FUNCTION	V_{DD} TO TERM. NO.		V_{SS} TO TERM. NO.		INPUT PULSE TO TERM. NO.		OTHER CONNECTIONS	
	$MONO_1$	$MONO_2$	$MONO_1$	$MONO_2$	$MONO_1$	$MONO_2$	$MONO_1$	$MONO_2$
Leading-Edge Trigger/ Retriggerable	3, 5	11, 13			4	12		
Leading-Edge Trigger/ Non-retriggerable	3	13			4	12	5-7	11-9
Trailing-Edge Trigger/ Retriggerable	3	13	4	12	5	11		
Trailing-Edge Trigger/ Non-retriggerable	3	13			5	11	4-6	12-10
Unused Section	5	11	3, 4	12, 13				

NOTES:

1. A RETRIGGERABLE ONE-SHOT MULTIVIBRATOR HAS AN OUTPUT PULSE WIDTH WHICH IS EXTENDED ONE FULL TIME PERIOD (T_X) AFTER APPLICATION OF THE LAST TRIGGER PULSE.
2. A NON-RETRIGGERABLE ONE-SHOT MULTIVIBRATOR HAS A TIME PERIOD T_X REFERENCED FROM THE APPLICATION OF THE FIRST TRIGGER PULSE.



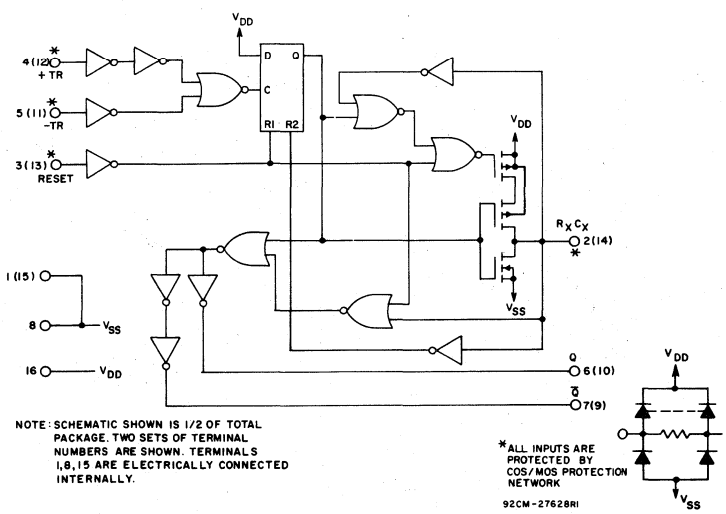


Fig. 4 – CD4098B logic diagram.

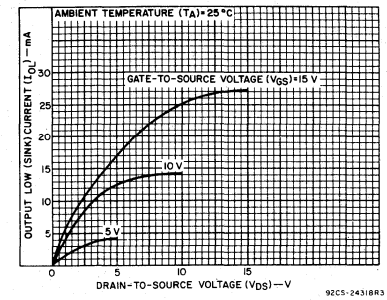


Fig. 1 – Typical output low (sink) current characteristics.

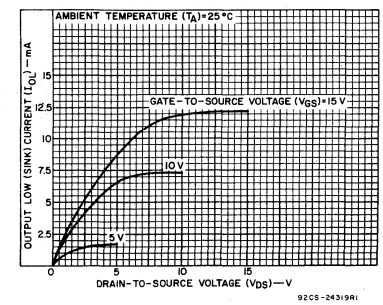


Fig. 2 – Minimum output low (sink) current characteristics.

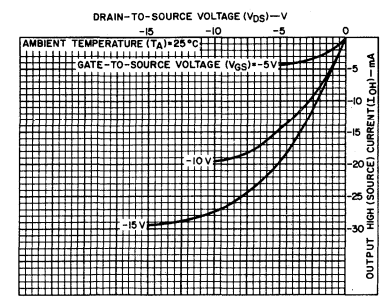


Fig. 3 – Typical output high (source) current characteristics.

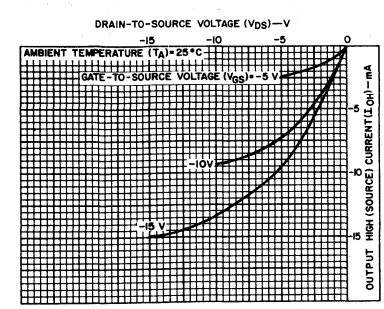


Fig. 5 – Minimum output high (source) current characteristics.

CD4098B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55,+25,+125 Apply to D,K,F,H Pkgs. Values at −40,+25,+85 Apply to E Pkgs.							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

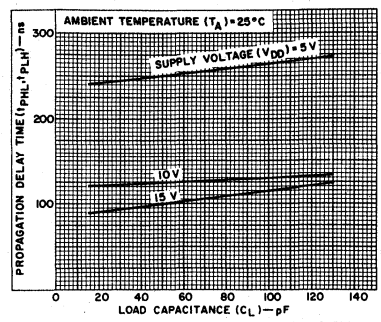


Fig. 6 – Typical propagation delay time vs. load capacitance, trigger into Q out. (All values of C_X and R_X.)

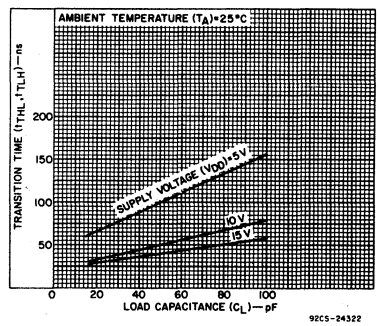


Fig. 7 – Transition time vs. load capacitance for R_X = 5 kΩ-10000 kΩ and C_X = 15 pF-10000 pF.

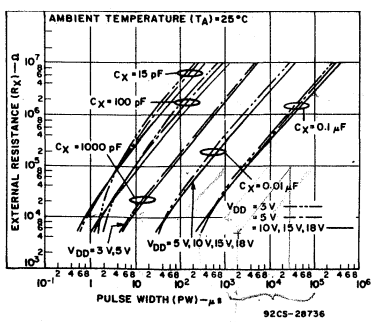


Fig. 8 – Typical external resistance vs. pulse width.

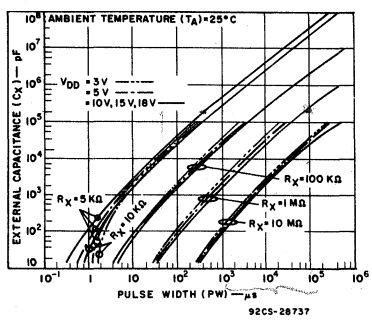


Fig. 9 – Typical external capacitance vs. pulse width.

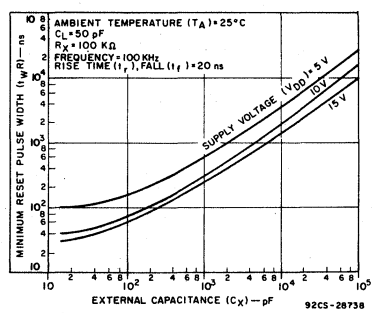
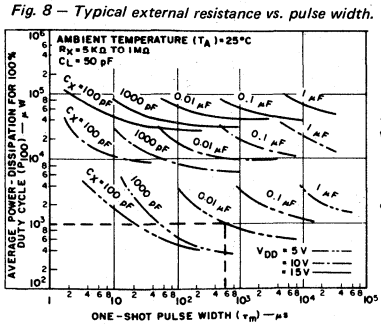


Fig. 10 – Typical minimum reset pulse width vs. external capacitance.



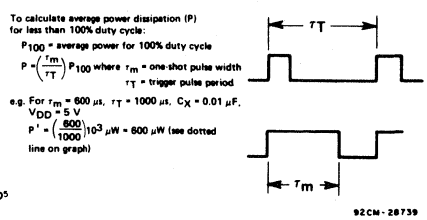


Fig. 11 – Average power dissipation vs. one-shot pulse width.

TEST CIRCUITS

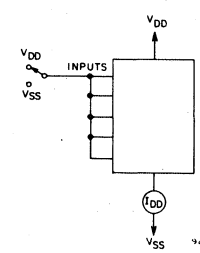


Fig. 12 – Quiescent-device-current test circuits.

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25°C$; Input $t_r, t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200$ kΩ

CHARACTERISTIC	TEST CONDITIONS			LIMITS		UNITS
	R_X (kΩ)	C_X (pF)	V_{DD} (V)	Typ.	Max.	
Trigger Propagation Delay Time +TR, −TR to Q, $\overline{Q}$ t_{PHL}, t_{PLH}	5 to 10,000	≥15	5	250	500	ns
			10	125	250	
			15	100	200	
Minimum Trigger Pulse Width, t_{WH}, t_{WL}	5 to 10,000	≥15	5	70	140	ns
			10	30	60	
			15	20	40	
Transition Time, t_{TLH}	5 to 10,000	≥15	5	100	200	ns
			10	50	100	
			15	40	80	
t_{THL}	5 to 10,000	15 to 10,000	5	100	200	
			10	50	100	
			15	40	80	
	5 to 10,000	0.01 μF to 0.1 μF	5	150	300	
			10	75	150	
			15	65	130	
	5 to 10,000	0.1 μF to 1 μF	5	250	500	
			10	150	300	
			15	80	160	
Reset Propagation Delay Time, T_{PHL}, T_{PLH}	5 to 10,000	≥15	5	225	450	ns
			10	125	250	
			15	75	150	
Minimum Reset Pulse Width, t_{WR}	100	15	5	100	200	ns
			10	40	80	
			15	30	60	
		1000	5	600	1200	
			10	300	600	
			15	250	500	
		0.1 μF	5	25	50	μs
			10	15	30	
			15	10	20	
Trigger Rise or Fall Time t_r(TR), t_f(TR)	–	–	5 to 15	–	100	μs
Pulse Width Match Between Circuits in Same Package	10	10,000	5	5	10	%
			10	7.5	15	
			15	7.5	15	
Input Capacitance, C_{IN}	Any Input			5	7.5	pF

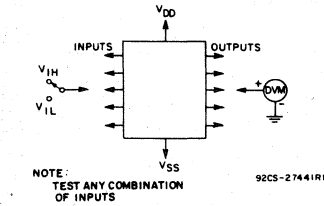


Fig. 13 – Input-voltage test circuit.

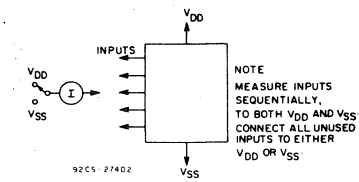


Fig. 14 – Input leakage current test circuit.

APPLICATIONS

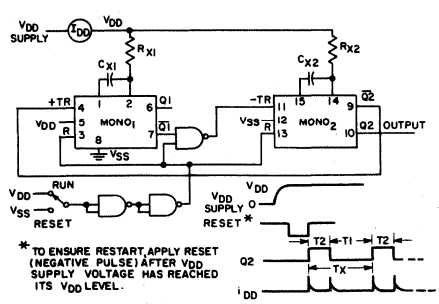


Fig. 15 – Astable multivibrator with restart after reset capability.

I_{DD}, T_X vs. R_X

R_X	I_{DD} (Avg.)	T_X (T1 + T2)	V_{DD}
10 kΩ	1 mA	3.8 μs	5 V
↓	↓ 0.05 mA	↓ 0.5 s	
	2.5 mA	3.2 μs	10 V
	↓ 0.5 mA	↓ 0.5 s	
	5 mA	3 μs	15 V
10 MΩ	↓ 1 mA	↓ 0.5 s	

Note:
All values are typical.
C_X range: 0.0001 μF to 0.1 μF.

92CM-28740

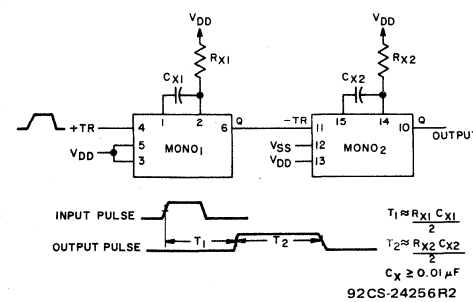
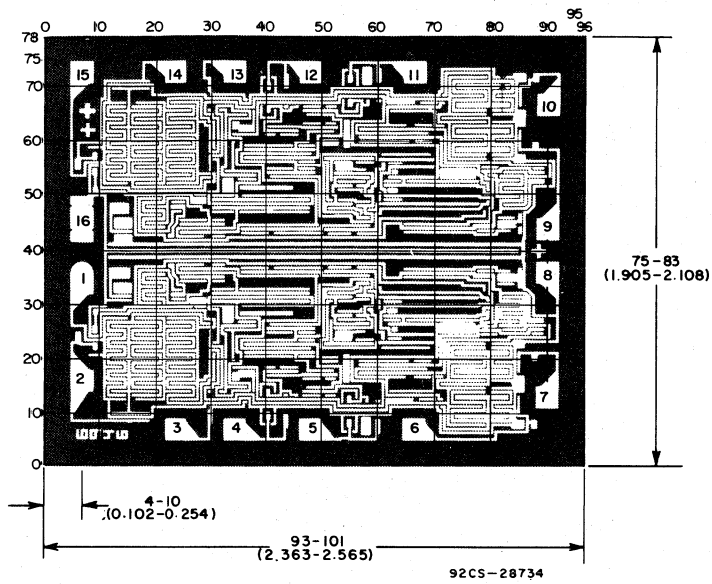


Fig. 16 – Pulse delay.



Dimensions and Pad Layout for CD4098B

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photograph and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips the cleavage angles are 57^{o} instead of 90^{o} with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS
8-Bit Addressable Latch

High-Voltage Types (20-Volt Rating)

The RCA-CD4099B 8-bit addressable latch is a serial-input, parallel-output storage register that can perform a variety of functions.

Data are inputted to a particular bit in the latch when that bit is addressed (by means of inputs A0, A1, A2) and when WRITE DISABLE is at a low level. When WRITE DISABLE is high, data entry is inhibited; however, all 8 outputs can be continuously read independent of WRITE DISABLE and address inputs.

A master RESET input is available, which resets all bits to a logic "0" level when RESET and WRITE DISABLE are at a high level. When RESET is at a high level, and WRITE DISABLE is at a low level, the latch acts as a 1-of-8 demultiplexer; the bit that is addressed has an active output which follows the data input, while all unaddressed bits are held to a logic "0" level.

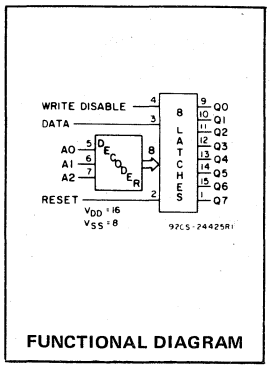
The CD4099B types are supplied in 16-lead hermetic ceramic dual-in-line packages (D and F suffixes), 16-lead plastic dual-in-line packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

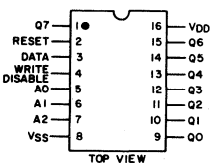
- **Serial data input** ■ **Active parallel output**
- **Storage register capability** ■ **Master clear**
- **Can function as demultiplexer**
- **Standardized, symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V (full package-temperature range), 100 nA at 18 V and 25°C**
- **Noise margin (full package-temperature range) = 1 V at V_{DD} = 5 V, 2 V at V_{DD} = 10 V, 2.5 V at V_{DD} = 15 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

- **Multi-line decoders**
- **A/D converters**



FUNCTIONAL DIAGRAM



TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

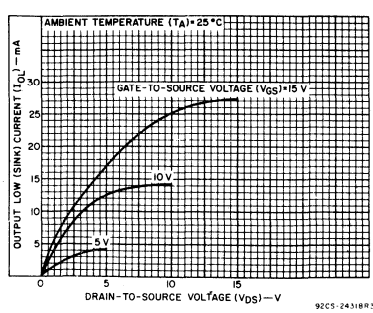


Fig.1 — Typical output low (sink) current characteristics.

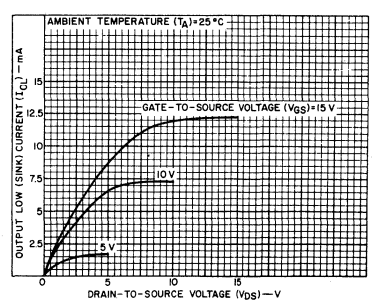


Fig.2 — Minimum output low (sink) current characteristics.

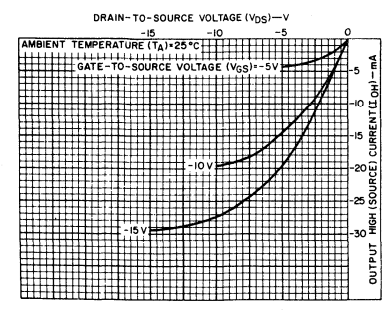


Fig.3 — Typical output high (source) current characteristics.

RECOMMENDED OPERATING CONDITIONS *at T_A = 25° C (Unless otherwise specified)*
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	SEE FIG. 2*	V_{DD} (V)	LIMITS MIN.	LIMITS MAX.	UNITS
Supply Voltage Range: (At T_A = Full Package Temperature Range)			3	18	V
Minimum Pulse Width, t_W Data	4	5	200	–	ns
		10	100	–	
		15	80		
Address	8	5	400	–	
		10	200	–	
		15	125	–	
Reset	5	5	150	–	
		10	75	–	
		15	50	–	
Setup Time, t_S Data to WRITE DISABLE	6	5	100	–	ns
		10	50	–	
		15	35	–	
Hold Time, t_H Data to WRITE DISABLE	7	5	150	–	ns
		10	75	–	
		15	50	–	

* Circled numbers refer to times indicated on master timing diagram.

Note: In addition to the above characteristics, a WRITE DISABLE ON time (the time that WRITE DISABLE is at a high level) must be observed during an address change for the total time that the external address lines A0, A1, and A2 are settling to a stable level, to prevent a wrong cell from being addressed (see Fig. 6).

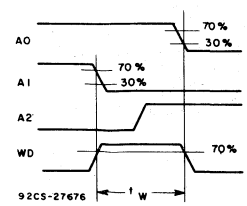


Fig.6 — Definition of WRITE DISABLE ON time.

MODE SELECTION			
WD	R	ADDRESSED LATCH	UNADDRESSED LATCH
0	0	Follows Data	Holds Previous State
0	1	Follows Data (Active High 8-Channel Demultiplexer)	Reset to "0"
1	0	Holds Previous State	
1	1	Reset to "0"	Reset to "0"

WD = WRITE DISABLE R = RESET

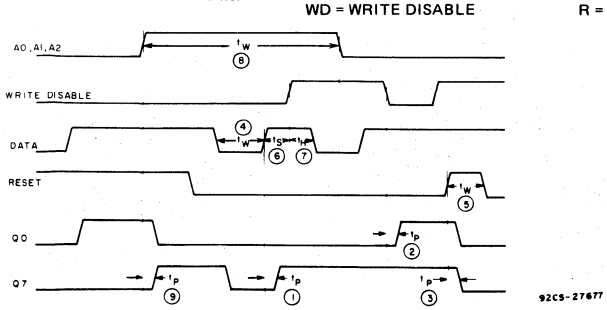


Fig.8 — Master timing diagram.

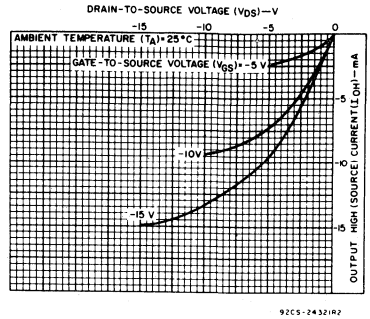


Fig.4 — Minimum output high (source) current characteristics.

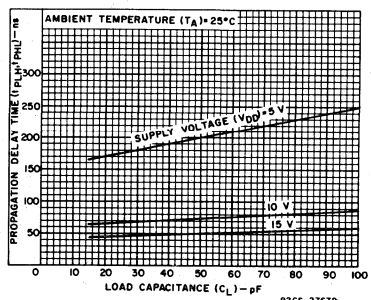


Fig.5 — Typical propagation delay time (data to Qn) vs. load capacitance.

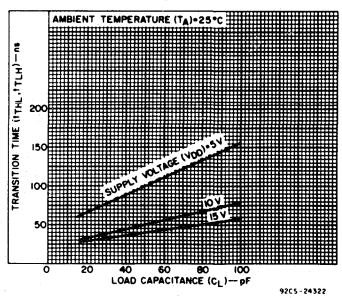


Fig.7 — Typical transition time vs. load capacitance.

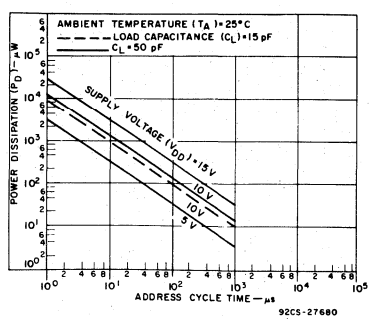


Fig.9 — Typical dynamic power dissipation vs. address cycle time.

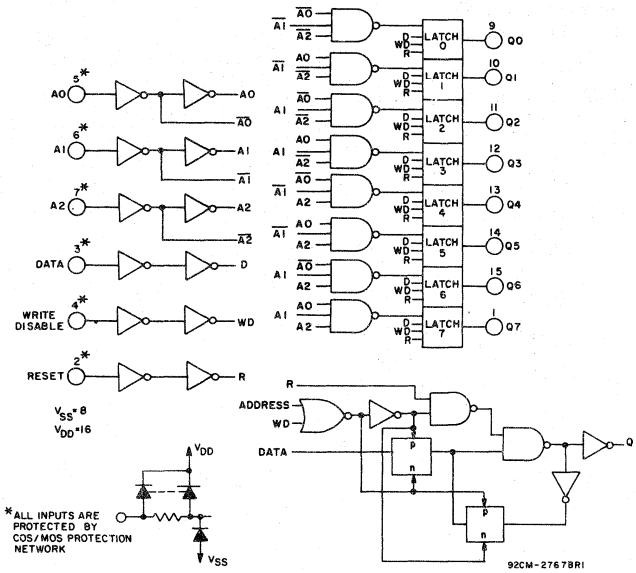


Fig. 10 — Logic diagram of CD4099B and detail of 1 of 8 latches.

TEST CIRCUITS

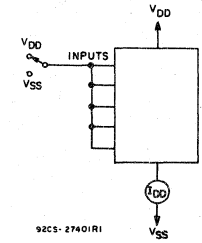


Fig. 11 — Quiescent device current test circuit.

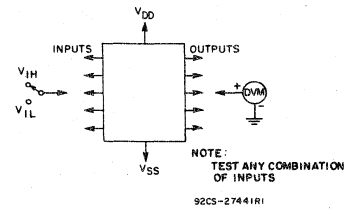


Fig. 12 — Input voltage test circuit.

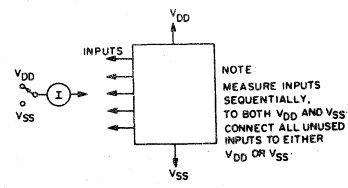


Fig. 13 — Input current test circuit.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	-	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

APPLICATIONS

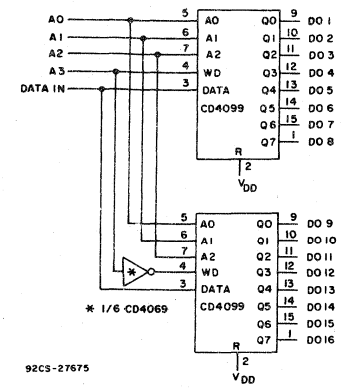


Fig. 14 — 1 of 16 decoder/demultiplexer.

DYNAMIC ELECTRICAL CHARACTERISTICS *at $T_A = 25°C$, $C_L = 50\,pF$, Input t_r, $t_f = 20\,ns$, $R_L = 200\,K\Omega$*

CHARACTERISTIC	CONDITIONS SEE FIG. 2*	V_{DD} (V)	LIMITS ALL PACKAGE TYPES TYP.	MAX.	UNITS
Propagation Delay: t_{PLH}, t_{PHL} Data to Output,	①	5	200	400	ns
		10	75	150	
		15	50	100	
WRITE DISABLE to Output, t_{PLH}, t_{PHL}	②	5	200	400	
		10	80	160	
		15	60	120	
Reset to Output, t_{PHL}	③	5	175	350	
		10	80	160	
		15	65	130	
Address to Output, t_{PLH}, t_{PHL}	⑨	5	225	450	
		10	100	200	
		15	75	150	
Transition Time, t_{THL}, t_{TLH} (Any Output)		5	100	200	ns
		10	50	100	
		15	40	80	
Minimum Pulse Width, t_W Data	④	5	100	200	ns
		10	50	100	
		15	40	80	
Address	⑧	5	200	400	ns
		10	100	200	
		15	65	125	
Reset	⑤	5	75	150	ns
		10	40	75	
		15	25	50	
Minimum Setup Time, t_S Data to WRITE DISABLE	⑥	5	50	100	ns
		10	25	50	
		15	20	35	
Minimum Hold Time, t_H Data to WRITE DISABLE	⑦	5	75	150	ns
		10	40	75	
		15	25	50	
Input Capacitance, C_{IN}	Any Input		5	7.5	pF

*Circled numbers refer to times indicated on master timing diagram.

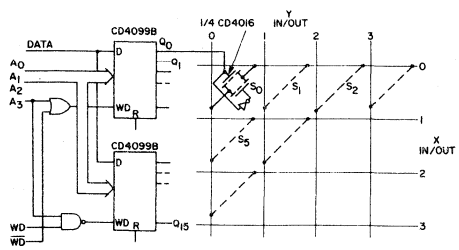


Fig. 15 — Multiple selection decoding — 4 x 4 crosspoint switch.

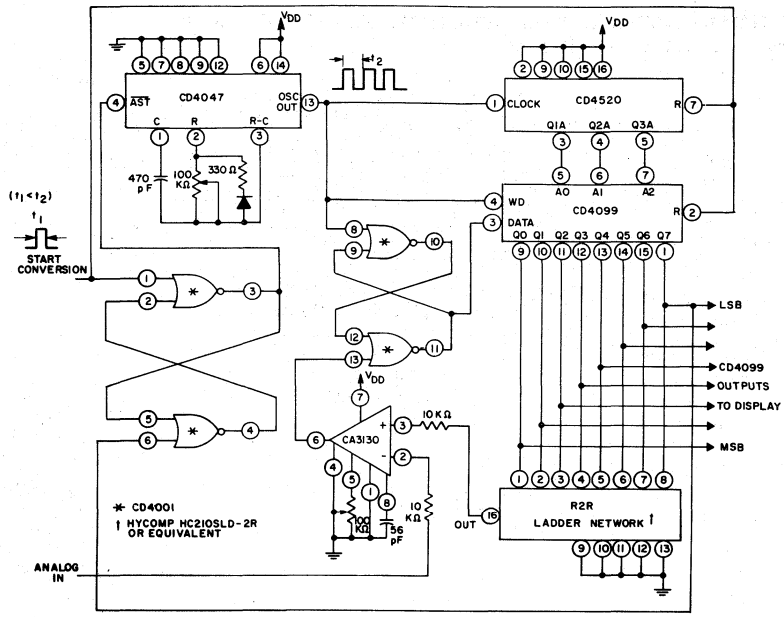
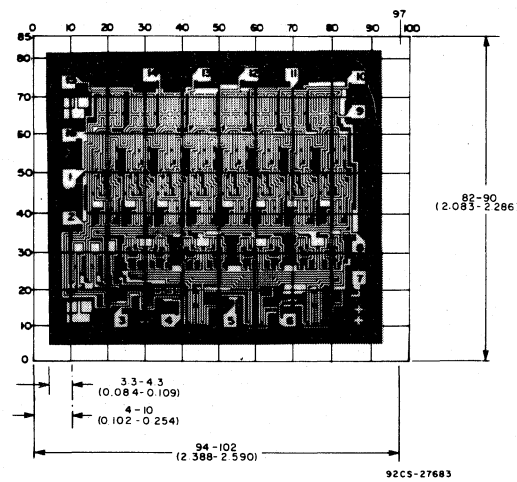


Fig. 16 — A/D converter 92CL-27681



CD4099BH
DIMENSIONS AND PAD LAYOUT

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS Strobed Hex Inverter/Buffer

High-Voltage Types (20-Volt Rating)

The RCA-CD4502B consists of six inverter/buffers with 3-state outputs. A logic "1" on the OUTPUT DISABLE input produces a high-impedance state in all six outputs. This feature permits common busing of the outputs, thus simplifying system design. A Logic "1" on the INHIBIT input switches all six outputs to logic "0" if the OUTPUT DISABLE input is a logic "0". This device is capable of driving two standard TTL loads, which is equivalent to six times the JEDEC "B"-series I_{OL} standard.

The CD4502B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

This device is similar to the MC14502.

Features:

- 2 TTL-load output drive capability
- 3-state outputs
- Common output-disable control
- Inhibit control
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**
- **Noise margin (full package-temperature range) =**

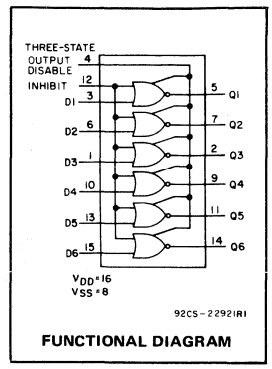
  1 V at V_{DD} = 5 V

  2 V at V_{DD} = 10 V

  2.5 V at V_{DD} = 15 V

Applications:

- **3-state hex inverter for interfacing IC's with data buses**
- **COS/MOS to TTL hex buffer**



FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

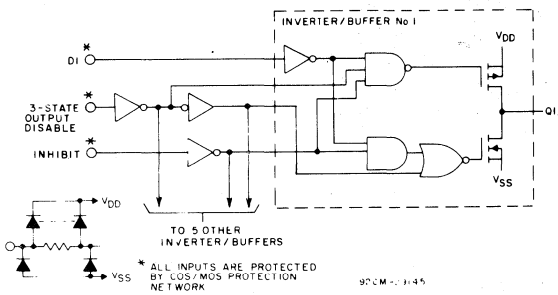


Fig.1 – Logic diagram of 1 of 6 identical inverter/buffers.

TRUTH TABLE

DISABLE	INHIBIT	Dn	Qn
0	0	0	1
0	0	1	0
0	1	X	0
1	X	X	Z

Logic 0 = Low
Z = High Impedance
X = Don't Care
Logic 1 = High

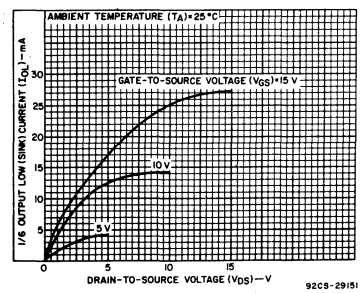


Fig.2 – Typical output low (sink) current characteristics.

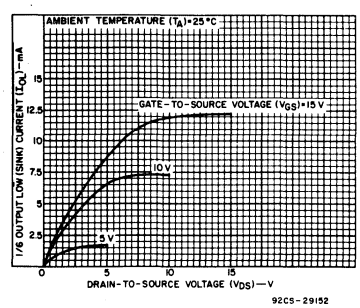


Fig.3 – Minimum output low (sink) current characteristics.

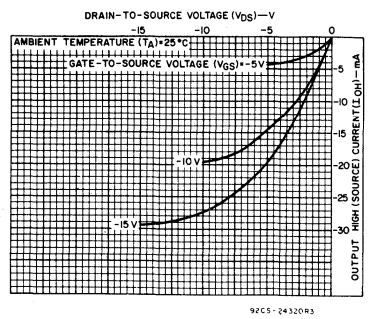


Fig.4 – Typical output high (source) current characteristics.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	3.84	3.66	2.52	2.16	3.06	6	–	mA
	0.5	0,10	10	9.6	9	6.6	5.4	7.8	15.6	–	
	1.5	0,15	15	25.2	24	16.8	14.4	20.4	40.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5, 13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	4.5	–	5	3.5				3.5	—	—	
	9	–	10	7				7	—	—	
	13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA
3-State Output Leakage Current I_{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	–	$\pm 10^{-4}$	±0.4	μA

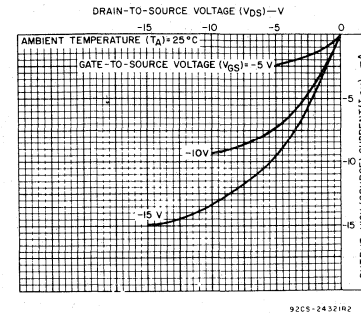


Fig.5 – Minimum output high (source) current characteristics.

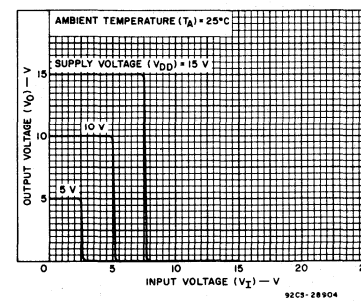


Fig.6 – Typical voltage transfer characteristics.

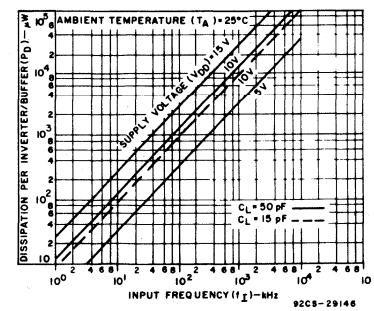


Fig.7 – Typical power dissipation as a function of input frequency.

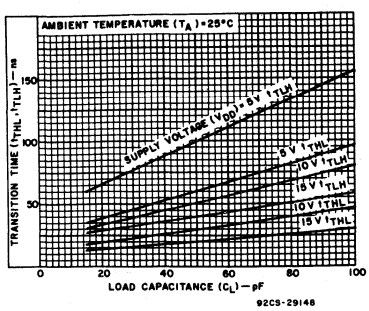


Fig.8 – Typical transition time as a function of load capacitance.

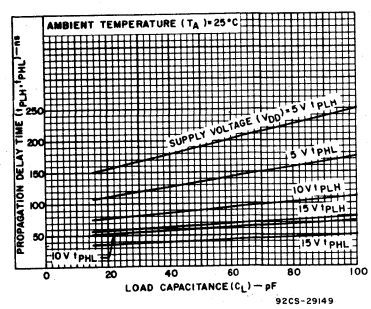


Fig.9 – Typical propagation-delay time as a function of load capacitance.

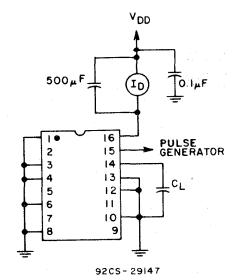


Fig. 10 – Power-dissipation test circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	LIMITS TYP	LIMITS MAX	UNITS
Data or Inhibit Delay Times: High to Low, t_{PHL}		5	135	270	ns
		10	60	120	
		15	40	80	
Low to High, t_{PLH}		5	190	380	
		10	90	180	
		15	65	130	
Disable Delay Times: Output High to High Impedance, t_{PHZ}		5	60	120	ns
		10	40	80	
		15	30	60	
High-Impedance to Output High, t_{PZH}	See Fig. 14	5	110	220	
		10	50	100	
		15	40	80	
Output Low to High Impedance, t_{PLZ}		5	125	250	
		10	65	130	
		15	55	110	
High Impedance to Output Low, t_{PZL}		5	125	250	
		10	55	110	
		15	40	80	
Transition Times: Low to High, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
High to Low, t_{THL}		5	60	120	
		10	30	60	
		15	20	40	
Input Capacitance, C_{IN}	Any Input		5	7.5	pF

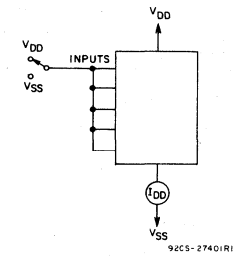


Fig. 11 — Quiescent-device-current test circuit.

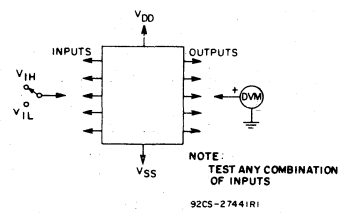


Fig. 12 — Input-voltage test circuit.

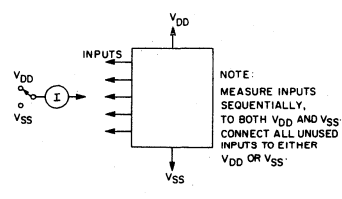
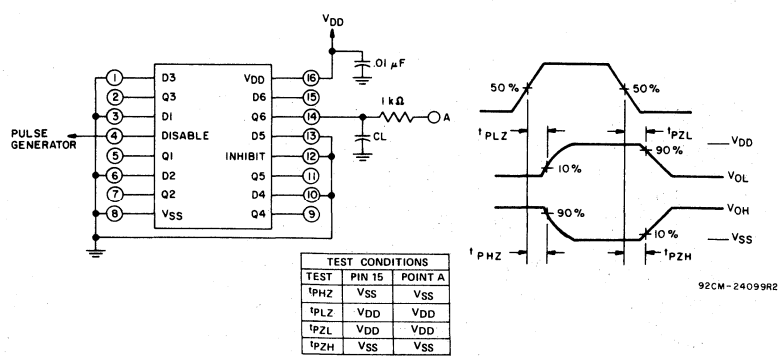
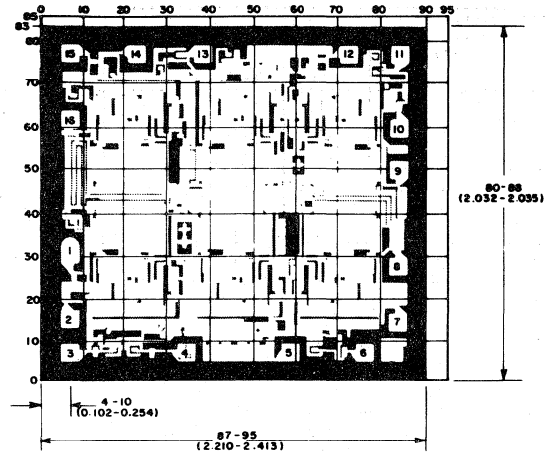


Fig. 13 — Input leakage current test circuit.



TEST CONDITIONS		
TEST	PIN 15	POINT A
t_{PHZ}	V_{SS}	V_{SS}
t_{PLZ}	V_{DD}	V_{DD}
t_{PZL}	V_{DD}	V_{DD}
t_{PZH}	V_{SS}	V_{SS}

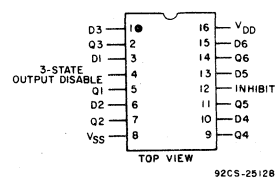
Fig. 14 — Disable delay times test circuit and waveforms.



Dimensions and Pad Layout for CD4502BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch.)

The photograph and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.



TERMINAL ASSIGNMENT

CD4508B Types

COS/MOS Dual 4-Bit Latch

High-Voltage Types (20-Volt Rating)

The RCA-CD4508B dual 4-bit latch contains two identical 4-bit latches with separate STROBE, RESET, and OUTPUT DISABLE controls. With the STROBE line in the high state, the data on the "D" inputs appear at the corresponding "Q" outputs provided the DISABLE line is in the low state. Changing the STROBE line to the low state locks the data into the latch. A high on the reset line forces the outputs to a low level regardless of the state of the STROBE input. The outputs are forced to the high-impedance state for bus line applications by a high level on the DISABLE input.

The CD4508B types are supplied in the 24-lead dual in-line ceramic packages (D and F suffixes), 24-lead dual-in-line plastic packages (E suffix), 24-lead ceramic flat packages (K suffix), and in chip form (H suffix).

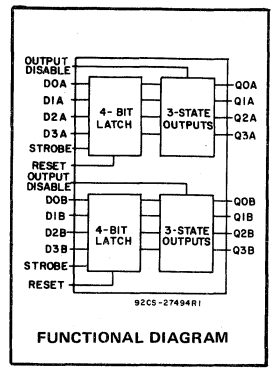
The CD4508B is similar to industry type MC14508.

Features:

- **Two independent 4-bit latches**
- **Individual master reset for each 4-bit latch**
- **3-state outputs with high-impedance state for bus line applications**
- **Medium-speed operation: $t_{PHL} = t_{PLH} = 70$ ns (typ.) at $V_{DD} = 10$ V and $C_L = 50$ pF**
- **100% tested for quiescent current at 20 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Standardized, symmetrical output characteristics**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (full package-temperature range) =**
  1 V at $V_{DD} = 5$ V
  2 V at $V_{DD} = 10$ V
  2.5 V at $V_{DD} = 15$ V
- **Meets all requirements of JEDEC Tentative Standard No.13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

- **Buffer storage**
- **Holding registers**
- **Data storage and multiplexing**



FUNCTIONAL DIAGRAM

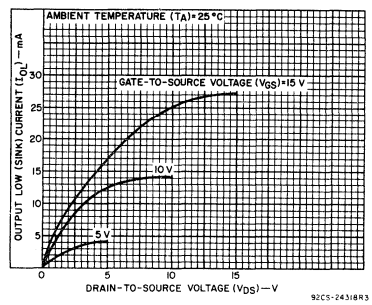


Fig.2 – Typical output low (sink) current characteristics.

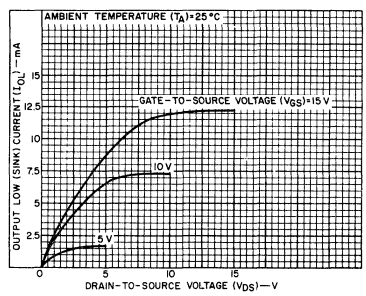


Fig.3 – Minimum output low (sink) current characteristics.

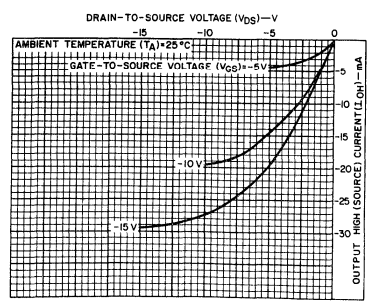


Fig.4 – Typical output high (source) current characteristics.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

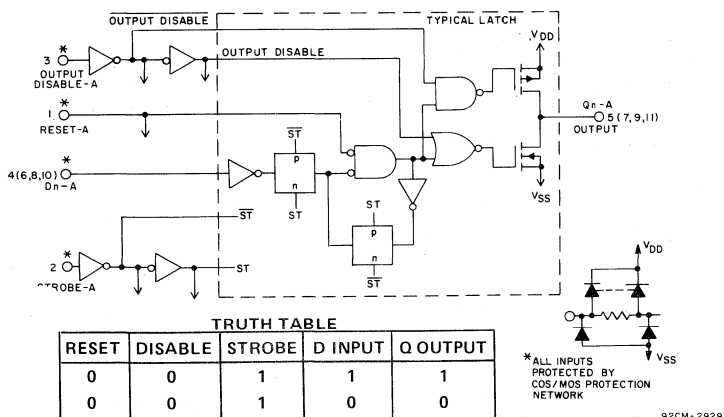
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	18	V
Reset Pulse Width, $t_{W(R)}$	5	200	–	ns
	10	140	–	
	15	100	–	
Strobe Pulse Width, $t_{W(st)}$	5	140	–	
	10	80	–	
	15	70	–	
Setup Time, t_{SU}	5	50	–	
	10	30	–	
	15	20	–	
Hold Time, t_H	5	0	–	
	10	0	–	
	15	0	–	

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA
3-State Output Leakage Current I_{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	–	$±10^{-4}$	±0.4	μA



TRUTH TABLE

RESET	DISABLE	STROBE	D INPUT	Q OUTPUT
0	0	1	1	1
0	0	1	0	0
0	0	0	X	LATCHED
1	0	X	X	0
X	1	X	X	Z

1 = HIGH LEVEL X = DON'T CARE

0 = LOW LEVEL Z = HIGH IMPEDANCE

Fig. 7 — Logic diagram (A-Section), 1 of 4 identical latches with common output disable, reset, and strobe.

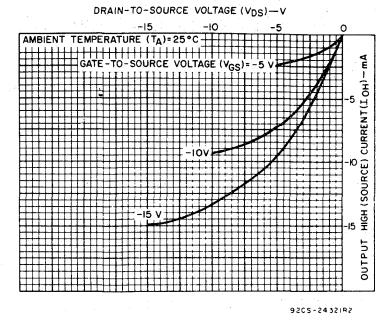


Fig. 4 — Minimum output high (source) current characteristics.

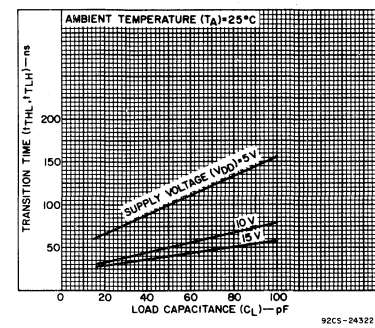


Fig. 5 — Typical transition time as a function of load capacitance.

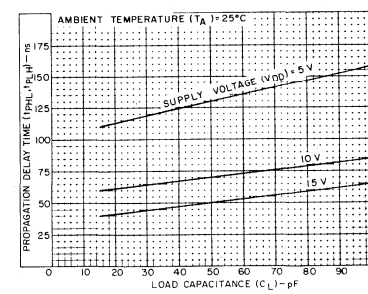


Fig. 6 — Typical propagation delay time as a function of load capacitance (strobe to data out).

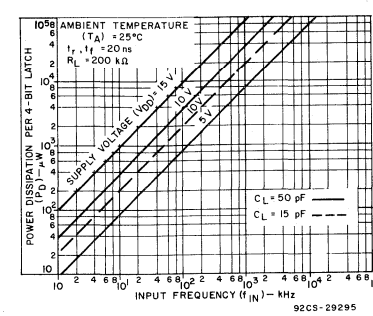


Fig. 8 — Typical power dissipation as a function of frequency.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ, unless otherwise specified.

CHARACTERISTIC	TEST CONDITIONS	V_{DD}	LIMITS Typ.	LIMITS Max.	UNITS
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Minimum Reset Pulse Width, $t_{W(R)}$		5	100	200	
		10	70	140	
		15	50	100	
Minimum Strobe Pulse Width, $t_{W(st)}$		5	70	140	
		10	40	80	
		15	35	70	
Minimum Setup Time, t_{SU}		5	25	50	
		10	15	30	
		15	10	20	
Minimum Hold Time, t_H		5	0	0	
		10	0	0	
		15	0	0	
Propagation Delay Times: t_{PHL}, t_{PLH} Strobe to Data Out		5	130	260	
		10	70	140	
		15	50	100	
Data In to Data Out		5	105	210	
		10	60	120	
		15	45	90	
Reset to Data Out		5	90	180	
		10	50	100	
		15	40	80	
3-State Propagation Delay Times: Output High to High Impedance, t_{PHZ}		5	110	220	
		10	60	120	
		15	40	80	
High Impedance to Output High, t_{PZH}		5	90	180	
		10	50	100	
		15	35	70	
Output Low to High Impedance, t_{PLZ}		5	90	180	
		10	50	100	
		15	35	70	
High Impedance to Output Low, t_{PZL}		5	90	180	
		10	50	100	
		15	35	70	
Input Capacitance, C_{IN}	Any Input	–	5	7.5	pF

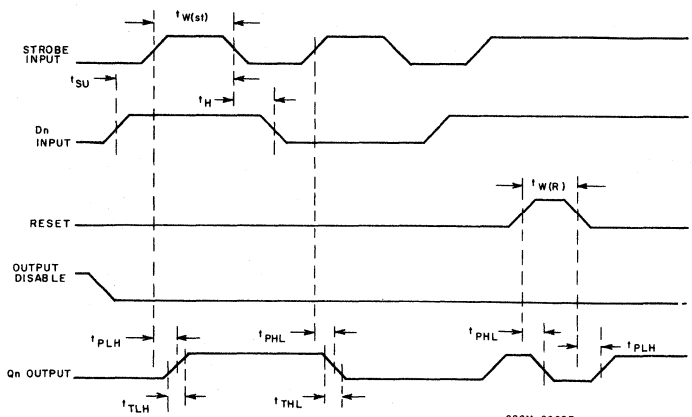


Fig. 12 – Test waveforms.

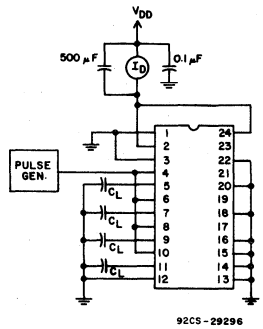


Fig.9 – Power dissipation test circuit.

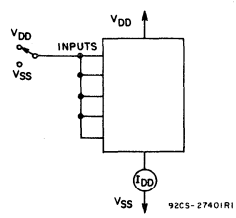


Fig.10 – Quiescent device current test circuit.

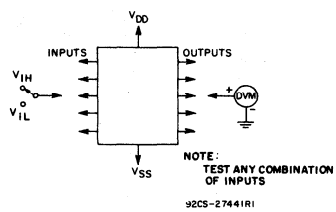


Fig.11 – Input voltage test circuit.

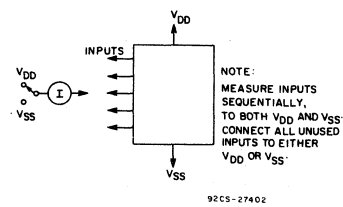


Fig. 13 – Input current test circuit.

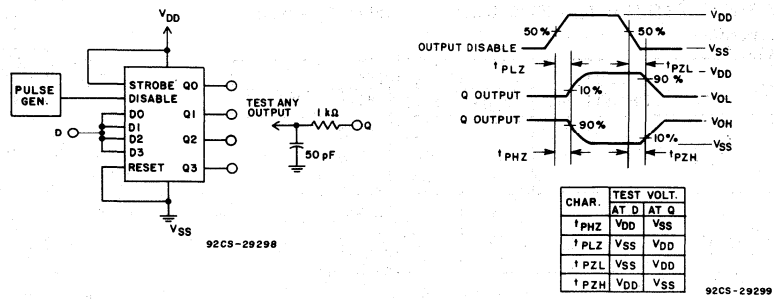


Fig. 14 – Output disable test circuit and waveforms.

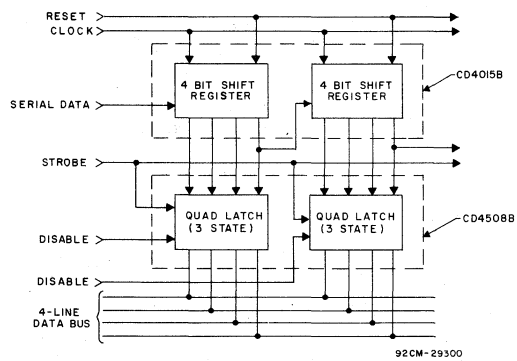


Fig. 15 – Bus register.

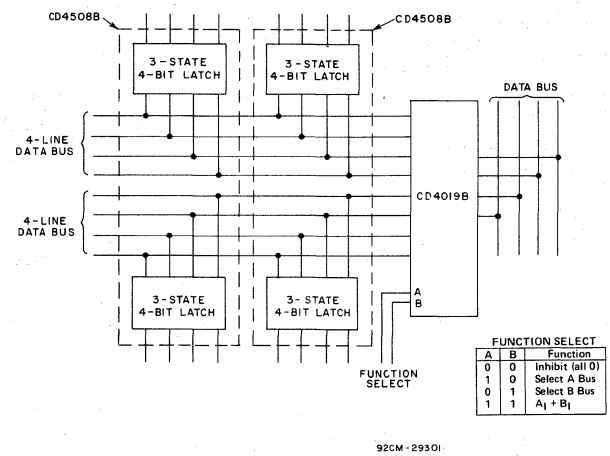
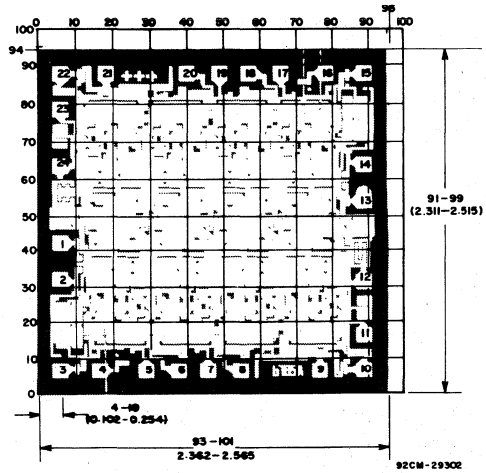


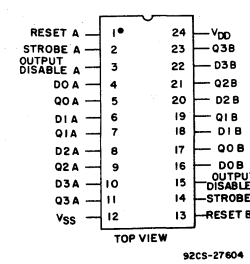
Fig. 16 – Dual multiplexed bus register with function select.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions and pad layout for CD4508B.



TERMINAL ASSIGNMENT

COS/MOS Presettable Up/Down Counters

High-Voltage Types (20-Volt Rating)

CD4510B – – – BCD Type

CD4516B – – – Binary Type

The RCA-CD4510B Presettable BCD Up/Down Counter and the CD4516 Presettable Binary Up/Down Counter consist of four synchronously clocked D-type flip-flops (with a gating structure to provide T-type flip-flop capability) connected as counters. These counters can be cleared by a high level on the RESET line, and can be preset to any binary number present on the jam inputs by a high level on the PRESET ENABLE line. The CD4510B will count out of non-BCD counter states in a maximum of two clock pulses in the up mode, and a maximum of four clock pulses in the down mode.

If the CARRY-IN input is held low, the counter advances up or down on each positive-going clock transition. Synchronous cascading is accomplished by connecting all clock inputs in parallel and connecting the CARRY-OUT of a less significant stage to the CARRY-IN of a more significant stage.

The CD4510B and CD4516B can be cascaded in the ripple mode by connecting the CARRY-OUT to the clock of the next stage. If the UP/DOWN input changes during a terminal count, the CARRY-OUT must be gated with the clock, and the UP/DOWN input must change while the clock is high. This method provides a clean clock signal to the subsequent counting stage. (See Fig. 17).

These devices are similar to types MC14510 and MC14516.

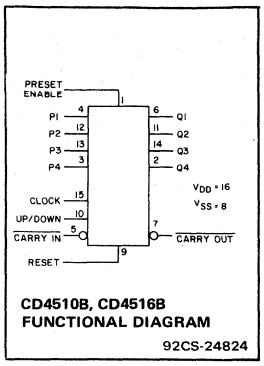
The CD4510B and CD4516B Series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- Medium-speed operation -- f_{CL} = 8 MHz typ. at 10 V
- Synchronous internal carry propagation
- Reset and Preset capability
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Standardized symmetrical output characteristics
- Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range): 1 V at V_{DD} = 5 V; 2 V at V_{DD} = 10 V; 2.5 V at V_{DD} = 15 V

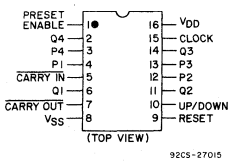
Applications:

- Up/Down difference counting
- Multistage synchronous counting
- Multistage ripple counting
- Synchronous frequency dividers



CD4510B, CD4516B
FUNCTIONAL DIAGRAM

92CS-24824



92CS-27015

CD4510B, CD4516B
TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . –0.5 to +20 V

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V

DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA

POWER DISSIPATION PER PACKAGE (P_D):
For T_A = –40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW

OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
PACKAGE TYPE E . . . . . –40 to +85°C

STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

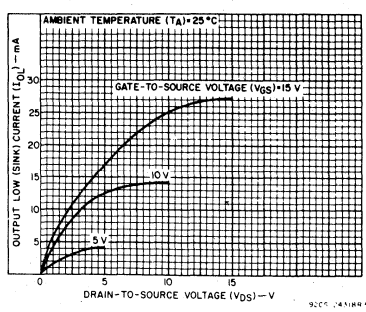


Fig. 1 – Typical output low (sink) current characteristics.

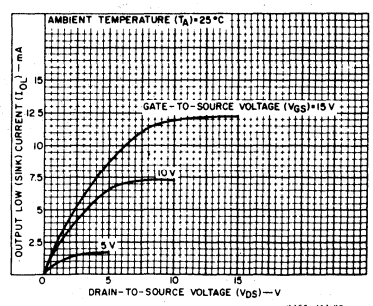


Fig. 2 – Minimum output low (sink) current characteristics.

OPERATING CONDITIONS AT T_A = 25°C, Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V_{DD}	Min.	Max.	Units
Supply Voltage Range (At T_A = Full Package-Temperature Range)		3	18	V
Clock Pulse Width, t_W	5	150	–	ns
	10	75	–	
	15	60	–	
Clock Input Frequency, f_{CL}	5	–	2	MHz
	10	–	4	
	15	–	5.5	
Preset Enable or Reset Removal Time●	5	150	–	ns
	10	80	–	
	15	60	–	
Clock Rise and Fall Time, t_rCL, t_fCL *	5	–	15	μs
	10	–	5	
	15	–	5	
Carry-In Setup Time, t_S	5	130	–	ns
	10	60	–	
	15	45	–	
Up-Down Setup Time, t_S	5	360	–	ns
	10	160	–	
	15	110	–	
Preset Enable or Reset Pulse Width, t_W	5	220	–	ns
	10	100	–	
	15	75	–	

●Time required after the falling edge of the reset or preset enable inputs before the rising edge of the clock will trigger the counter (similar to setup time).

*If more than one unit is cascaded in the parallel clocked application, t_rCL should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transition time of the carry output driving stage for the estimated capacitive load.

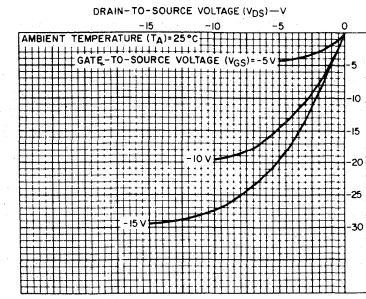


Fig. 3 – Typical output high (source) current characteristics.

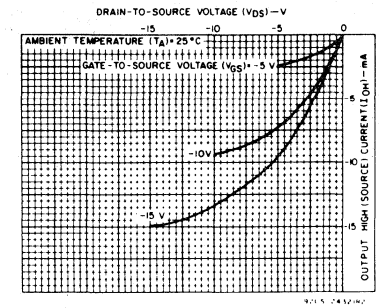


Fig. 4 – Minimum output high (source) current characteristics.

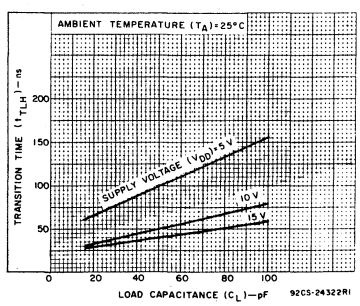


Fig. 5 – Typical transition time vs. load capacitance.

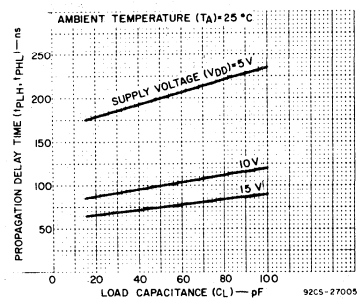


Fig. 6 – Typical propagation delay time vs. load capacitance for clock-to-Q outputs.

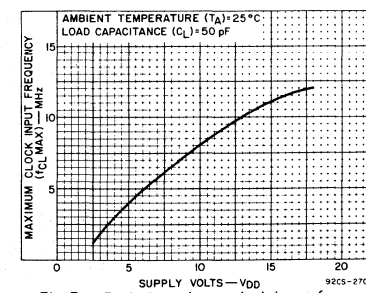


Fig. 7 – Typical maximum clock input frequency vs. supply voltage.

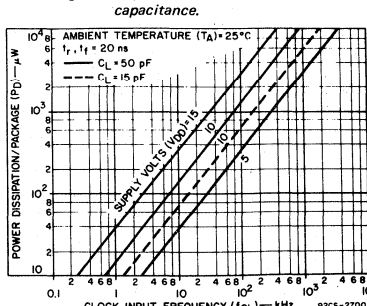


Fig. 8 – Typical dynamic power dissipation vs. frequency.

TEST CIRCUITS

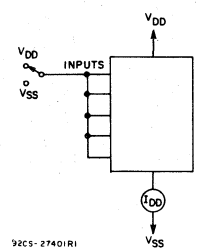


Fig. 9 – Quiescent device current.

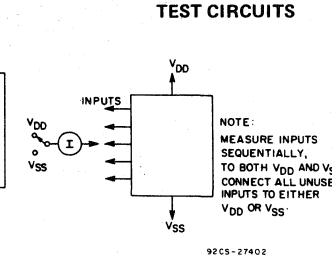


Fig. 10 – Input current.

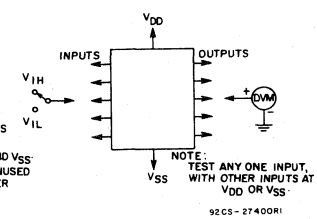


Fig. 11 – Input voltage.

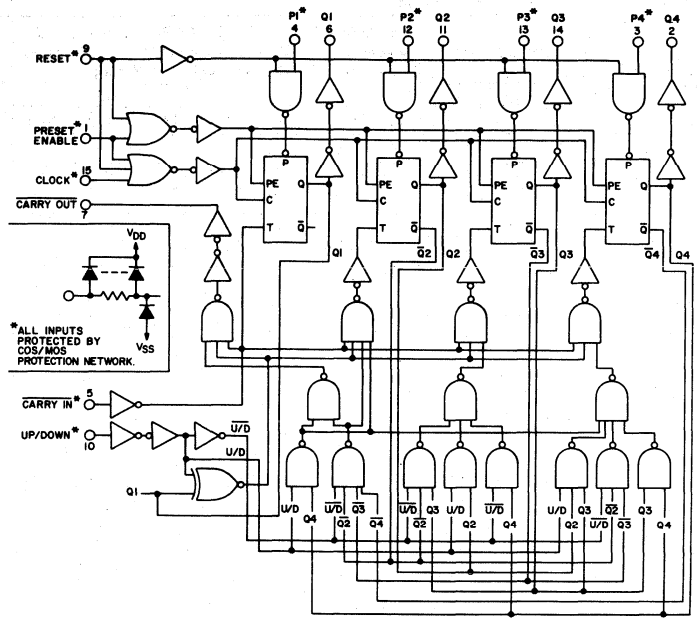


Fig. 12 – Logic Diagram for CD4510B.

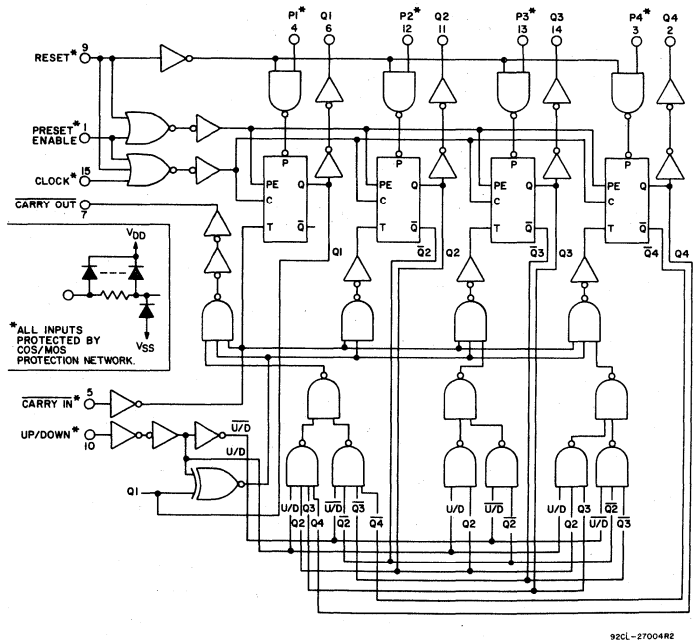


Fig. 13 – Logic Diagram for CD4516B.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
									+25		
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

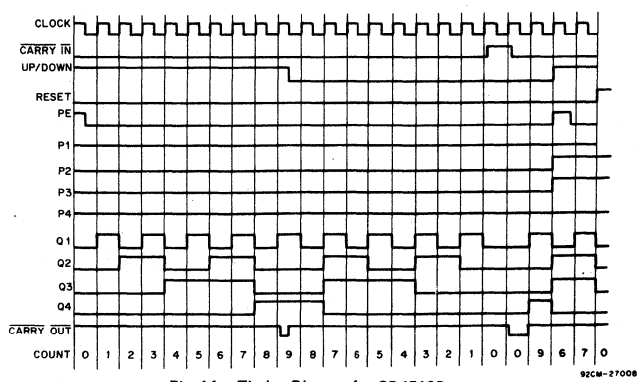


Fig. 14 – Timing Diagram for CD4510B.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 50 pF, Input t_r, t_f = 20 ns, R_L = 200 kΩ

Characteristic	Conditions V_{DD} (V)	Limits All Packages Min.	Typ.	Max.	Units
Propagation Delay Time (t_{PHL}, t_{PLH}):					
Clock-to-Q Output (See Fig. 10)	5	–	200	400	ns
	10	–	100	200	
	15	–	75	150	
Preset or Reset-to-Q Output	5	–	210	420	ns
	10	–	105	210	
	15	–	80	160	
Clock-to-Carry Out	5	–	240	480	ns
	10	–	120	240	
	15	–	90	180	
Carry-In-to-Carry Out	5	–	125	250	ns
	10	–	60	120	
	15	–	50	100	
Preset or Reset-to-Carry Out	5	–	320	640	ns
	10	–	160	320	
	15	–	125	250	
Transition Time (t_{THL}, t_{TLH}) (See Fig. 9)	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Max. Clock Input Frequency (f_{CL})	5	2	4	–	MHz
	10	4	8	–	
	15	5.5	11	–	
Input Capacitance (C_{IN})		–	5	7.5	pF

TRUTH TABLE

CL	$\overline{CI}$	U/D	PE	R	ACTION
X	1	X	0	0	NO COUNT
↓	0	1	0	0	COUNT UP
↓	0	0	0	0	COUNT DOWN
X	X	X	1	0	PRESET
X	X	X	X	1	RESET

X = DON'T CARE

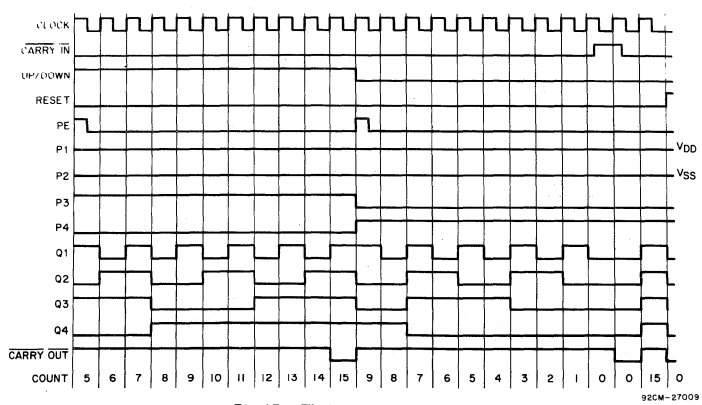


Fig. 15 – Timing diagram for CD4516B.

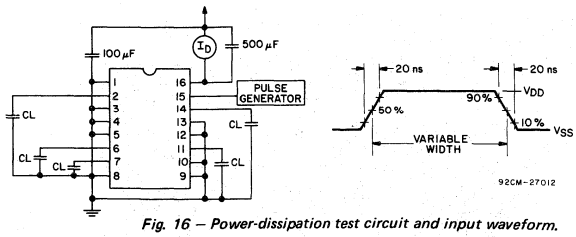


Fig. 16 – Power-dissipation test circuit and input waveform.

TYPICAL APPLICATIONS

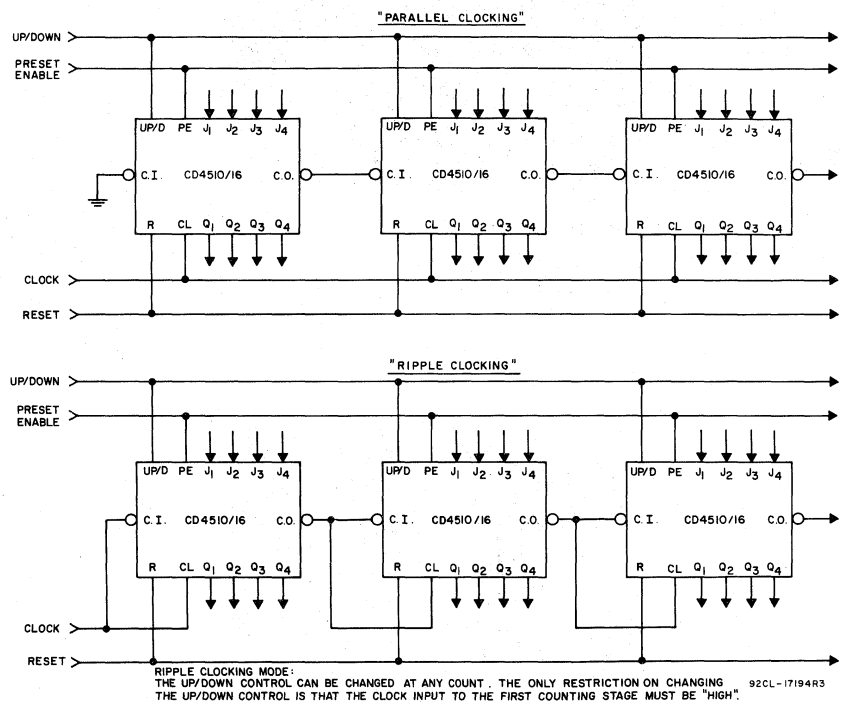
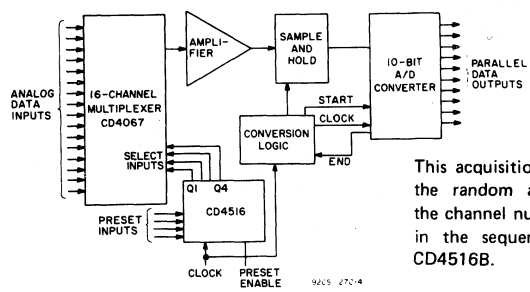
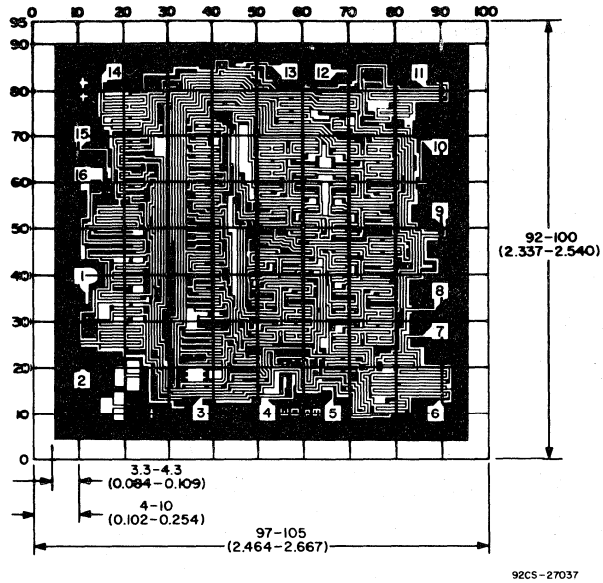


Fig. 17 – Cascading counter packages.

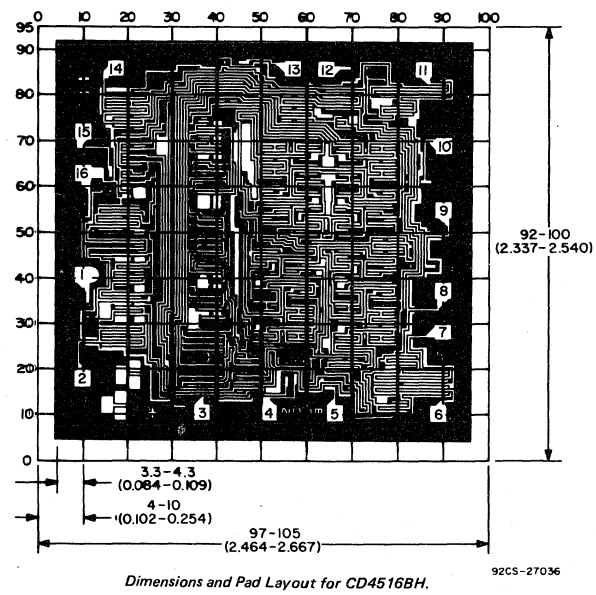


This acquisition system can be operated in the random access mode by jamming in the channel number at the present inputs, or in the sequential mode by clocking the CD4516B.

Fig. 18 – Typical 16-channel, 10-bit data aquisition system.



Dimensions and Pad Layout for CD4510BH.



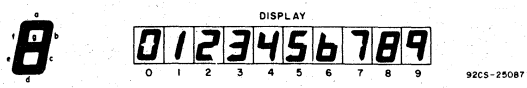
Dimensions and Pad Layout for CD4516BH.

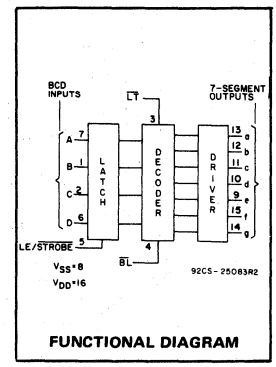
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS BCD-to-7-Segment Latch Decoder Drivers

High-Voltage Types (20-Volt Rating)





FUNCTIONAL DIAGRAM

The CD4511B types are BCD-to-7-segment latch decoder drivers constructed with COS/MOS logic and n-p-n bipolar transistor output devices on a single monolithic structure. These devices combine the low quiescent power dissipation and high noise immunity features of RCA COS/MOS with n-p-n bipolar output transistors capable of sourcing up to 25 mA. This capability allows the CD4511B types to drive LED's and other displays directly.

Lamp Test ($\overline{LT}$), Blanking ($\overline{BL}$), and Latch Enable or Strobe inputs are provided to test the display, shut off or intensity-modulate it, and store or strobe a BCD code, respectively. Several different signals may be multiplexed and displayed when external multiplexing circuitry is used. The CD4511B is supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

These devices are similar to the type MC14511.

Features:

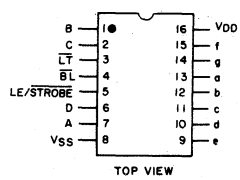
- **High-output-sourcing capability . . . . . up to 25 mA**
- **Input latches for BCD Code storage**
- **Lamp Test and Blanking capability**
- **7-segment outputs blanked for BCD input codes > 1001**
- **100% tested for quiescent current at 20 V**
- **Max. input current of 1 μA at 18 V, over full package-temperature range, 100 nA at 18 V and 25°C**
- **Standardized symmetrical output characteristics**
- **5-V, 10-V, and 15-V parametric ratings**

Applications:

- **Driving common-cathode LED displays**
- **Multiplexing with common-cathode LED displays**
- **Driving incandescent displays**
- **Driving low-voltage fluorescent displays**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C



CD4511B
TERMINAL ASSIGNMENT

OPERATING CONDITIONS AT T_A = 25°C Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges

Characteristic	V_{DD}	Min.	Max.	Units
Supply-Voltage Range (T_A): (Full Package-Temperature Range)	–	3	18	V
Set-Up Time (t_S)	5	150	–	ns
	10	70	–	ns
	15	40	–	ns
Hold Time (t_H)	5	0	–	ns
	10	0	–	ns
	15	0	–	ns
Strobe Pulse Width (t_W)	5	400	–	ns
	10	160	–	ns
	15	100	–	ns

CD4511B Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions				Limits at Indicated Temperatures (°C)							Units
					Values at −55, +25, +125 for D, F, K, H Packages Values at −40, +25, +85 for E Packages							
									+25			
	I_{OH} (mA)	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current: I_{DD} Max.	–	–	–	5	5	5	150	150	–	0.04	5	μA
	–	–	–	10	10	10	300	300	–	0.04	10	
	–	–	–	15	20	20	600	600	–	0.04	20	
	–	–	–	20	100	100	3000	3000	–	0.08	100	
Output Voltage: Low-Level V_{OL} Max.	–	–	0,5	5	0.05				–	0	0.05	V
	–	–	0,10	10	0.05				–	0	0.05	
	–	–	0,15	15	0.05				–	0	0.05	
High-Level V_{OH} Min.	–	–	0,5	5	4	4	4.2	4.2	4.1	4.55	–	V
	–	–	0,10	10	9	9	9.2	9.2	9.1	9.55	–	
	–	–	0.15	15	14	14	14.2	14.2	14.1	14.55	–	
Input Low Voltage, V_{IL} Max.	–	0.5,3.8	–	5	1.5				–	–	1.5	V
	–	1,8.8	–	10	3				–	–	3	
	–	1.5,13.8	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	–	0.5,3.8	–	5	3.5				3.5	–	–	V
	–	1,8.8	–	10	7				7	–	–	
	–	1.5,13.8	–	15	11				11	–	–	
Output Drive Voltage: High Level V_{OH} Min.	0	–	–	5	4.0	4.0	4.20	4.20	4.10	4.55	–	V
	5	–	–		–	–	–	–	–	4.25	–	
	10	–	–		3.80	3.80	3.90	3.90	3.90	4.10	–	
	15	–	–		–	–	3.50	3.50	–	3.95	–	
	20	–	–		3.55	3.55	–	–	3.40	3.75	–	
	25	–	–		3.40	3.40	–	–	3.10	3.55	–	
	0	–	–	10	9.0	9.0	9.20	9.20	9.10	9.55	–	V
	5	–	–		–	–	–	–	–	9.25	–	
	10	–	–		8.85	8.85	9.00	9.00	9.00	9.15	–	
	15	–	–		–	–	–	–	–	9.05	–	
	20	–	–		8.70	8.70	8.40	8.40	8.60	8.90	–	
	25	–	–		8.60	8.60	–	–	8.30	8.75	–	
	0	–	–	15	14.0	14.0	14.20	14.20	14.10	14.55	–	V
	5	–	–		–	–	–	–	–	14.30	–	
	10	–	–		13.90	13.90	14.0	14.0	14.0	14.20	–	
	15	–	–		–	–	–	–	–	14.10	–	
	20	–	–		13.75	13.75	13.50	13.50	13.70	13.95	–	
	25	–	–		13.65	13.65	–	–	13.50	13.80	–	
Output Low (Sink) Current, I_{OL} Min.	–	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	–	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	–	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Input Current, I_{IN} Max.	–	0,18	0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

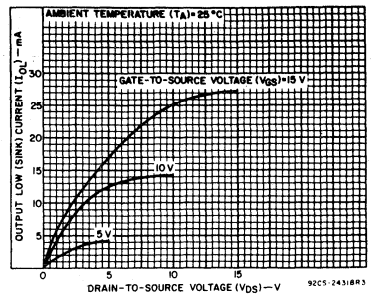


Fig. 1 — Typical output low (sink) current characteristics.

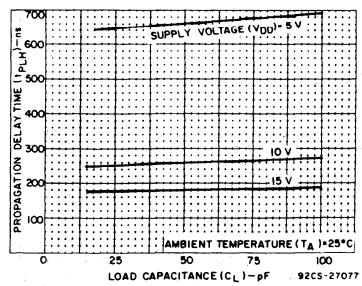


Fig. 2 — Typical data-to-output, low-to-high-level propagation delay time as a function of load capacitance.

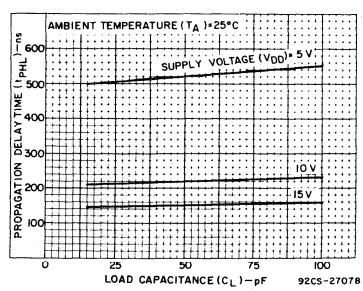


Fig. 3 — Typical data-to-output, high-to-low-level propagation delay time as a function of load capacitance.

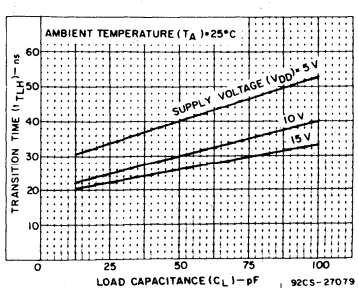


Fig. 4 — Typical low-to-high-level transition time as a function of load capacitance.

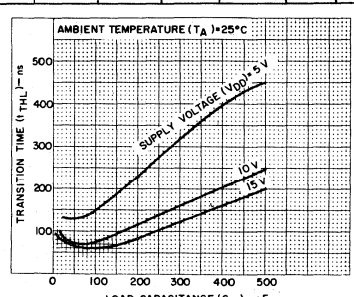


Fig. 5 — Typical high-to-low transition time as a function of load capacitance.

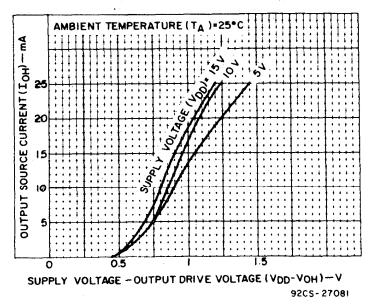


Fig. 6 — Typical voltage drop (V_{DD} to output) vs. output source current as a function of supply.

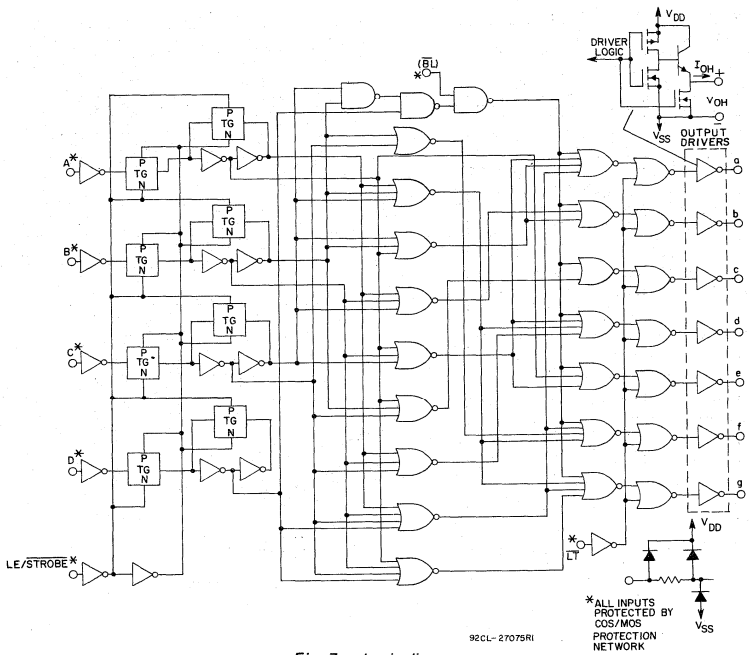


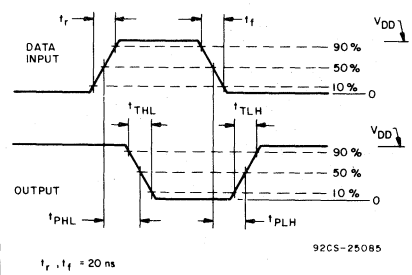
Fig. 7 — Logic diagram.

TRUTH TABLE

LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	Display
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	0	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	1	1	X	X	X	X				*				*

X ≡ Don't Care * Depends on BCD code previously applied when LE = 0

Note: Display is blank for all illegal input codes (BCD > 1001).



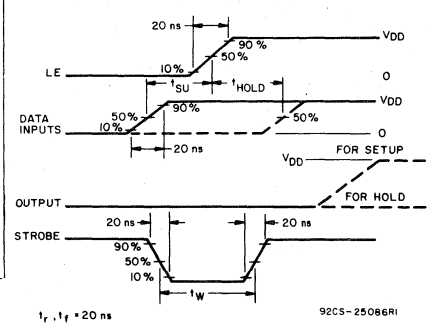
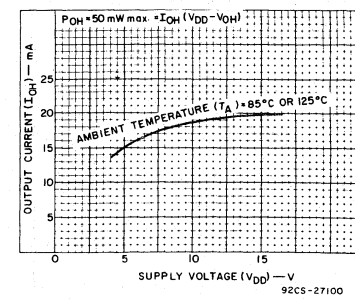


Fig. 10 — Dynamic waveforms.



Maximum continuous derated output current I_{OH} applies to a single output with all other outputs sourcing an equal amount of current at the supply voltages shown. Operation above the derating curve is not recommended.

Fig. 8 — Derated static output current per output at T_A = 125°C (package types D, F, K) and at T_A = 85°C (package type E).

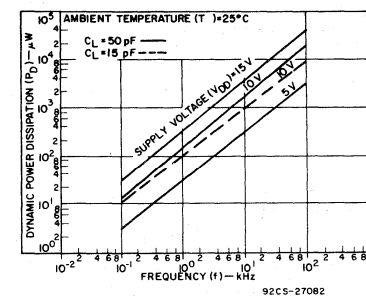


Fig. 9 — Typical dynamic power dissipation characteristics

TEST CIRCUITS

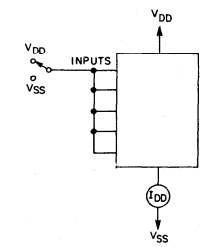


Fig. 11 — Quiescent device current.

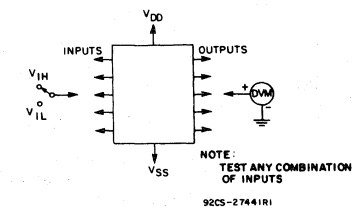
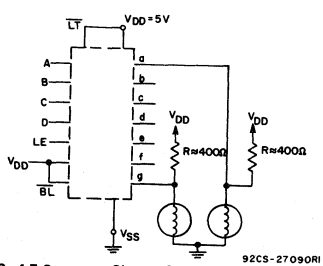


Fig. 12 — Input voltage.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	Test Conditions	LIMITS All Packages			UNITS
	V_{DD} Volts	Min.	Typ.	Max.	
Propagation Delay Time: (Data) High-to-Low Level, t_{PHL}	5	–	520	1040	ns
	10	–	210	420	
	15	–	150	300	
Low-to-High Level, t_{PLH}	5	–	660	1320	ns
	10	–	260	520	
	15	–	180	360	
Propagation Delay Time: ($\overline{BL}$) High-to-Low Level, t_{PHL}	5	–	350	700	ns
	10	–	175	350	
	15	–	125	250	
Low-to-High Level, t_{PLH}	5	–	400	800	ns
	10	–	175	350	
	15	–	150	300	
Propagation Delay Time: ($\overline{LT}$) High-to-Low Level, t_{PHL}	5	–	250	500	ns
	10	–	125	250	
	15	–	85	170	
Low-to-High Level, t_{PLH}	5	–	150	300	ns
	10	–	75	150	
	15	–	50	100	
Transition Time: Low-to-High Level, t_{TLH}	5	–	40	100	ns
	10	–	30	75	
	15	–	20	65	
High-to-Low Level, t_{THL}	5	–	125	310	ns
	10	–	75	185	
	15	–	65	160	
Minimum Set-Up Time, t_S	5	150	75	–	ns
	10	70	35	–	
	15	40	20	–	
Minimum Hold Time, t_H	5	0	–75	–	ns
	10	0	–35	–	
	15	0	–20	–	
Strobe Pulse Width, t_W	5	400	200	–	ns
	10	160	80	–	
	15	100	50		
Input Capacitance, C_{IN}		–	5	7.5	pF



2 of 7 Segments Shown Connected

Resistors R from V_{DD} to each 7-segment driver output are chosen to keep all Numitron segments slightly on and warm.

Fig. 16 – Driving incandescent displays (RCA Numitron DR2000 series displays).

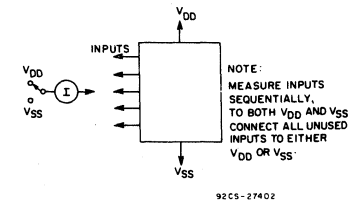


Fig. 13 – Input current.

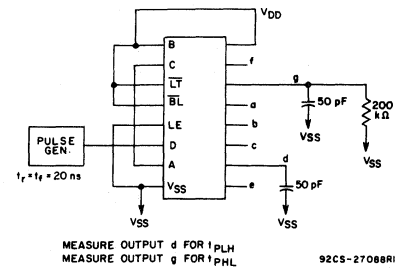


Fig. 14 – Data propagation delay.

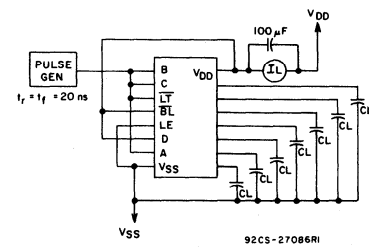
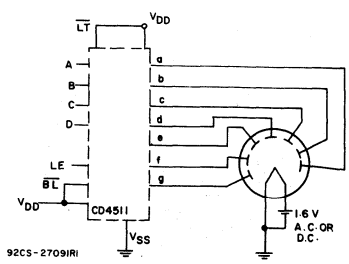


Fig. 15 – Dynamic power dissipation.

APPLICATIONS

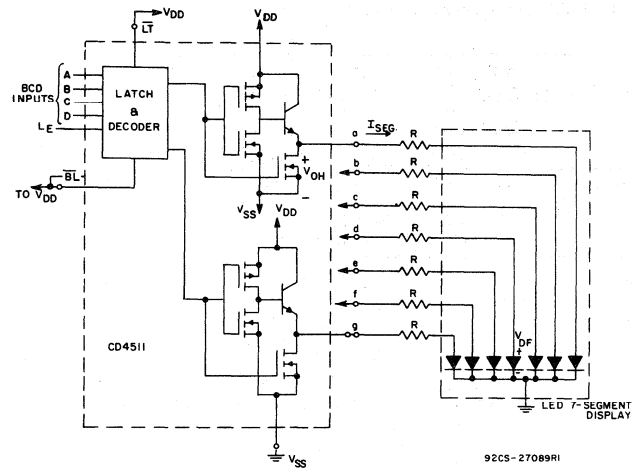
Interfacing with Various Displays



A medium-brightness intensity display can be obtained with low-voltage fluorescent displays such as the Tung-Sol Digivac S/G** Series.

**Trademark Tung-Sol Division Wagner Electric Co.

Fig. 17 – Driving low-voltage fluorescent displays.

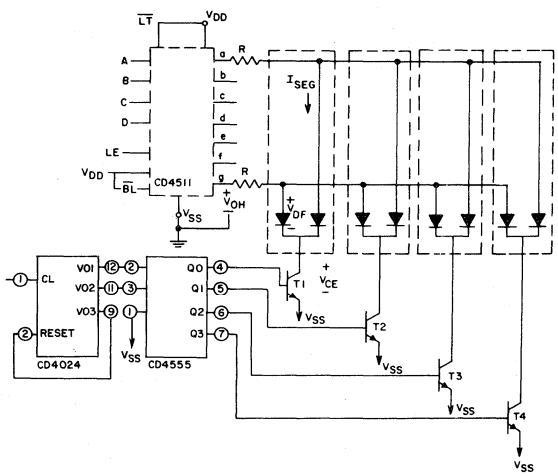


Duty Cycle = 100%

$I_{SEG} = I_{DIODE_{AVG.}}$ = 20 mA at Luminous Intensity/Segment = 250 microcandles

$$R = \frac{V_{OH} - V_{DF}}{I_{SEG}}$$

Fig. 18 — Driving common-cathode 7-segment LED displays (example Hewlet-Packard 5082-7740).



Multiplexing Scheme Showing 2 of 7 Segments Connected

Transistors T_1–T_4 (RCA-2N3053 or 2N2102) have I_C Max. rating $> 7 \times I_{SEG}$

Duty Cycle = 25%

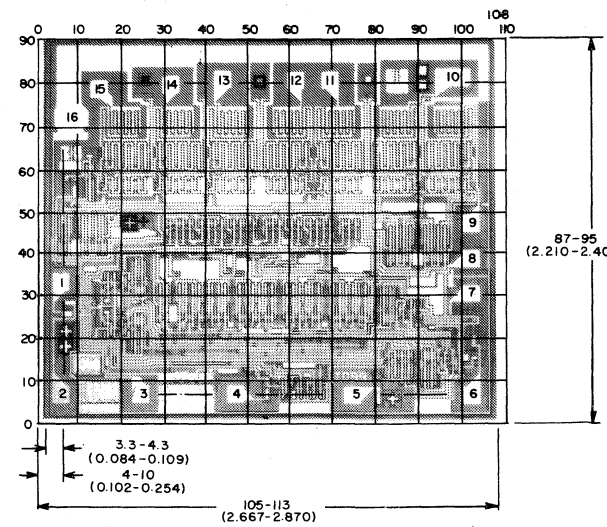
$I_{SEG} = [I_{DIODE_{AVG}}] \times 4$

$$R = \frac{(V_{OH} - V_{DF} - V_{CE})}{I_{SEG}}$$

All unused inputs on CD4555 are connected to V_{DD} or V_{SS}.

Fig. 19 — Multiplexing with common-cathode 7-segment LED displays (example Hewlet-Packard 5082-7404 4 character display or 4 discrete Monosanto Man 3 displays).

Dimensions and Pay Layout for CD4511B Chip



Dimensions and pad layout for CD4511B chip.

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

CD4512B Types

COS/MOS 8-Channel Data Selector

High-Voltage Types (20-Volt Rating)

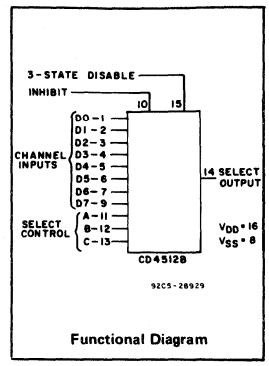
Preliminary Data

Features:

- 3-state output
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Digital multiplexing
- Number-sequence generation
- Signal gating



Functional Diagram

The RCA-CD4512B is an 8-channel data selector featuring a three-state output that can interface directly with, and drive, data lines of bus-oriented systems.

The CD4512B-series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

RECOMMENDED OPERATING CONDITIONS

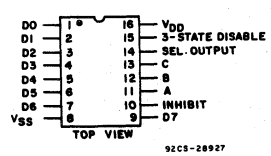
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

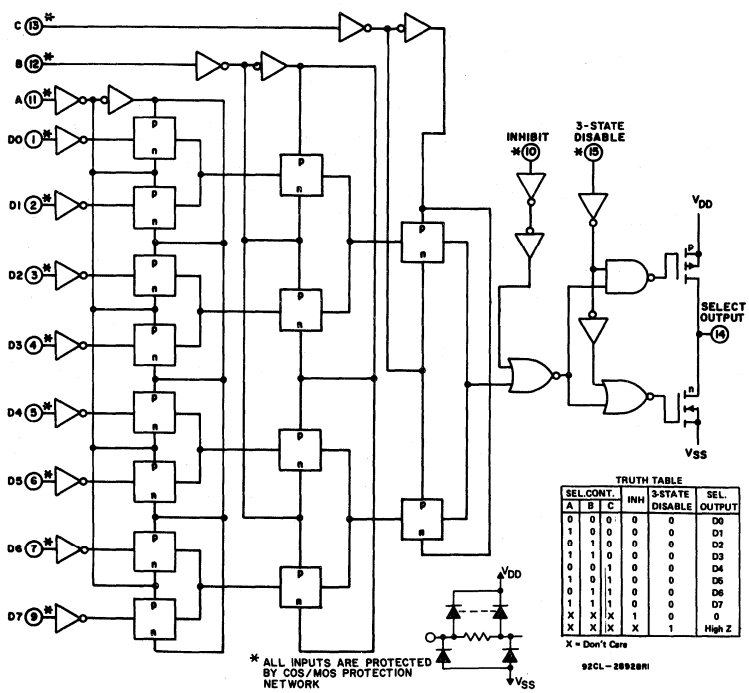
CHARACTERISTIC	Min.	Max.	Units
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . 0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . 0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

TERMINAL ASSIGNMENT





TRUTH TABLE

SEL.CONT. A	B	C	INH	3-STATE DISABLE	SEL. OUTPUT
0	0	0	0	0	D0
1	0	0	0	0	D1
0	1	0	0	0	D2
1	1	0	0	0	D3
0	0	1	0	0	D4
1	0	1	0	0	D5
0	1	1	0	0	D6
1	1	1	0	0	D7
X	X	X	1	0	0
X	X	X	X	1	High Z

X = Don't Care

92CL-28928R1

Fig. 1 — Logic diagram.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	-	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r,t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS TYPICAL VALUES	UNITS
Propagation Delay Time: Inhibit to Output, t_{PHL}, t_{PLH}	5	140	ns
	10	70	
	15	50	
Select to Output	5	280	
	10	115	
	15	80	
Data to Output	5	240	
	10	100	
	15	70	
3-State Disable Delay Time: t_{PZL}, t_{PLZ}, t_{PHZ}, t_{PZH}	5	75	ns
	10	45	
	15	35	
Transition Time, t_{THL}, t_{TLH}	5	100	ns
	10	50	
	15	40	
Input Capacitance, C_{IN} (Any Input)		5	pF

COS/MOS 4-Bit Latch/4-to-16 Line Decoders

High-Voltage Types (20-Volt Rating)
CD4514B Output "High" on Select
CD4515B Output "Low" on Select

The RCA-CD4514B and -CD4515B consist of a 4-bit strobed latch and a 4-to-16-line decoder. The latches hold the last input data presented prior to the strobe transition from 1 to 0. Inhibit control allows all outputs to be placed at 0(CD4514B) or 1(CD4515B) regardless of the state of the data or strobe inputs.

The decode truth table indicates all combinations of data inputs and appropriate selected outputs.

These devices are similar to industry types MC14514 and MC14515.

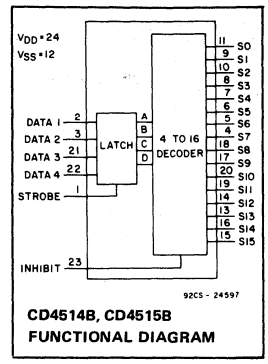
The CD4514B and CD4515B types are supplied in 24-lead hermetic dual-in-line ceramic packages (D and F suffixes), 24-lead dual-in-line plastic packages (E suffix), 24-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Strobed input latch**
- **Inhibit control**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (over full package temperature range):**
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- **5-V, 10-V, and 15-V parametric ratings**
- **Standardized, symmetrical output characteristics.**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

- **Digital multiplexing**
- **Address decoding**
- **Hexadecimal/BCD decoding**
- **Program-counter decoding**
- **Control decoder**



CD4514B, CD4515B FUNCTIONAL DIAGRAM

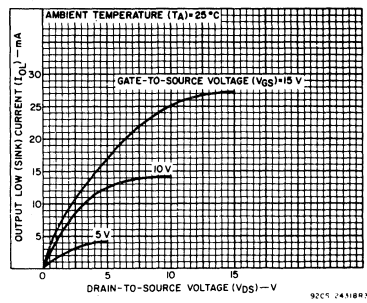


Fig. 1 — Typical output low (sink) current characteristics.

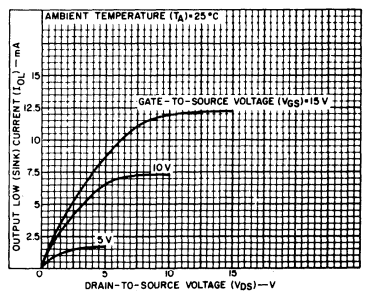


Fig. 2 — Minimum output low (sink) current characteristics.

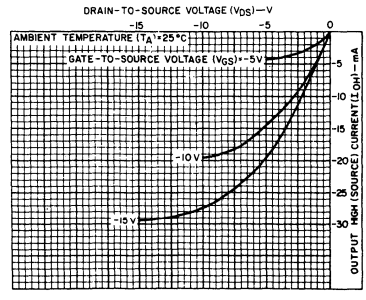


Fig. 3 — Typical output high (source) current characteristics.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	18	V
Data Setup Time, t_S	5	150	—	ns
	10	70	—	
	15	40	—	
Strobe Pulse Width, t_W	5	250	—	ns
	10	100	—	
	15	75	—	

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	1.6	1.5	1.1	0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				–	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	-	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

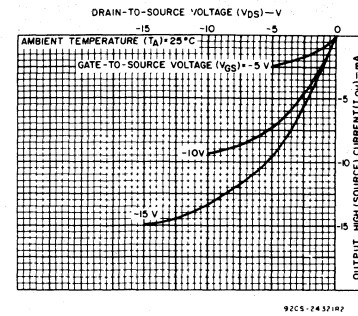


Fig. 4 — Minimum output high (source) current characteristics.

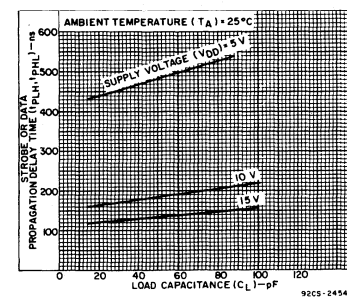


Fig. 5 — Typical strobe or data propagation delay time vs. load capacitance.

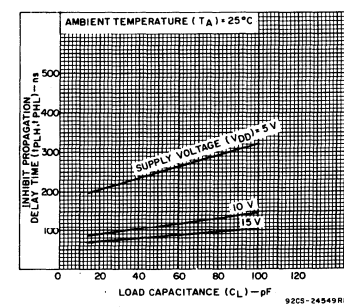


Fig. 6 — Typical inhibit propagation delay time vs. load capacitance.

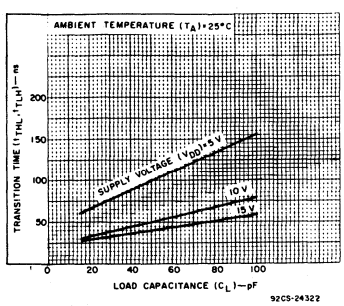


Fig. 7 — Typical low-to-high transition time vs. load capacitance.

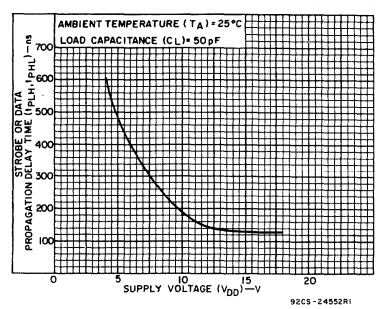


Fig. 8 — Typical strobe or data propagation delay time vs. supply voltage.

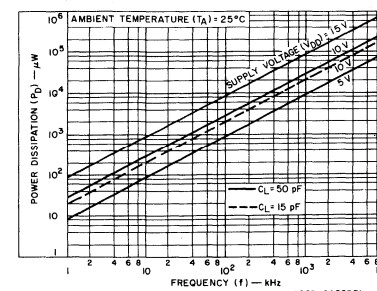


Fig. 9 — Typical power dissipation vs. frequency.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS
		V_{DD} V	Typ.	Max.	
Propagation Delay Time: t_{PHL}, t_{PLH} Strobe or Data		5	485	970	ns
		10	185	370	
		15	135	270	
Inhibit		5	250	500	
		10	110	220	
		15	85	170	
Transition Time, t_{TLH}, t_{THL}		5	100	200	
		10	50	100	
		15	40	80	
Minimum Strobe Pulse Width, t_W		5	125	250	ns
		10	50	100	
		15	40	75	
Minimum Data Setup Time, t_S		5	75	150	ns
		10	35	70	
		15	20	40	
Input Capacitance, C_{IN}	Any Input	–	5	7.5	pF

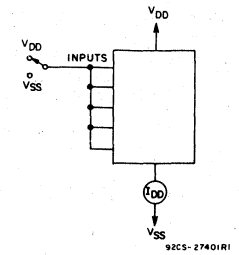


Fig. 10 – Quiescent device current test circuit.

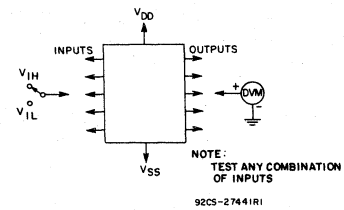


Fig. 11 – Input voltage test circuit.

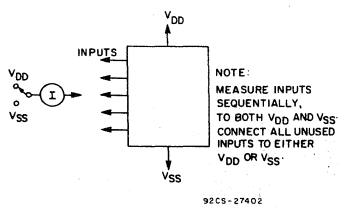


Fig. 12 – Input current test circuit.

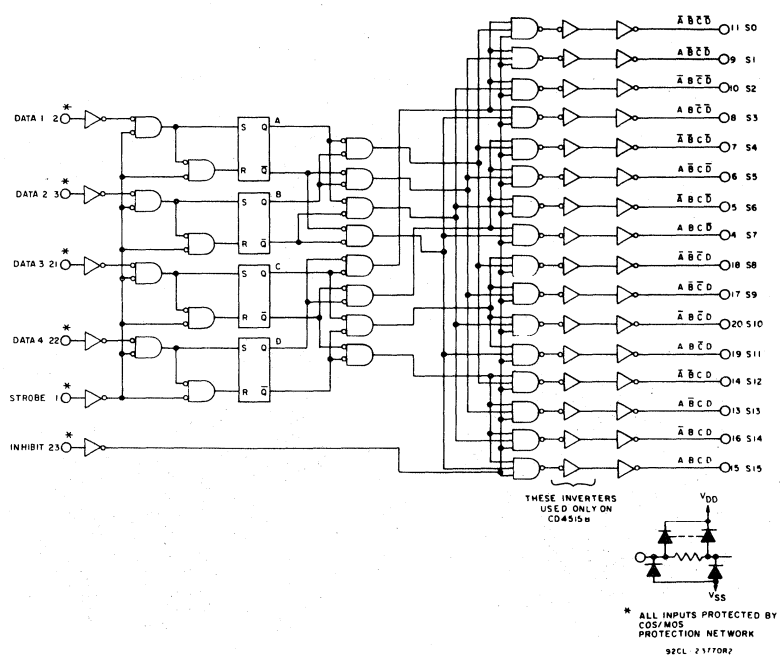


Fig. 13 – Logic diagram for CD4514B and CD4515B.

DECODE TRUTH TABLE (Strobe = 1)

INHIBIT	DECODER INPUTS				SELECTED OUTPUT CD4514B = Logic 1 (High) CD4515B = Logic 0 (Low)
	D	C	B	A	
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15
1	X	X	X	X	All Outputs = 0, CD4514B All Outputs = 1, CD4515B

X = Don't Care Logic 1 = high Logic 0 = low

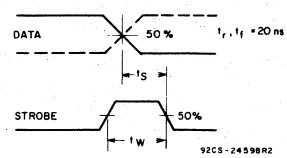
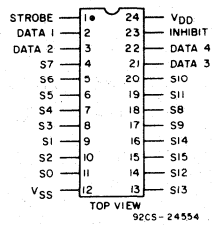
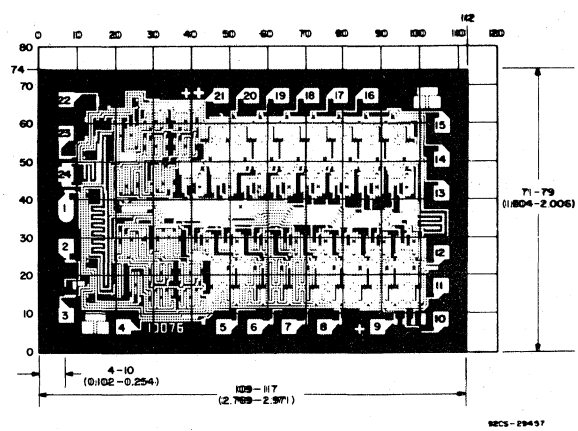


Fig. 14 — Waveforms for setup time and strobe pulse width.



CD4514B
CD4515B

TERMINAL ASSIGNMENT



Dimensions and Pad Layout for CD4515B Chip

(Dimensions and pad layout for the CD4514B are identical)

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS Dual Up-Counters

High-Voltage Types (20-Volt Rating)

CD4518B Dual BCD Up-Counter
CD4520B Dual Binary Up-Counter

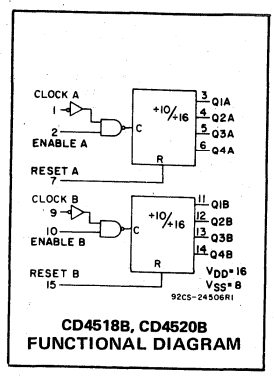
The RCA-CD4518 Dual BCD Up-Counter and CD4520 Dual Binary Up-Counter each consist of two identical, internally synchronous 4-stage counters. The counter stages are D-type flip-flops having interchangeable CLOCK and ENABLE lines for incrementing on either the positive-going or negative-going transition. For single-unit operation the ENABLE input is maintained high and the counter advances on each positive-going transition of the CLOCK. The counters are cleared by high levels on their RESET lines.

The counter can be cascaded in the ripple mode by connecting Q4 to the enable input of the subsequent counter while the CLOCK input of the latter is held low.

The CD4518B and CD4520B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Medium-speed operation – 6-MHz typical clock frequency at 10 V**
- **Positive- or negative-edge triggering**
- **Synchronous internal carry propagation**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin(over full package-temperature range): 1 V at V_{DD} = 5 V; 2 V at V_{DD} = 10 V; 2.5 V at V_{DD} = 15 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Standardized, symmetrical output characteristics**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**



CD4518B, CD4520B FUNCTIONAL DIAGRAM

Applications:

- **Multistage synchronous counting**
- **Multistage ripple counting**
- **Frequency dividers**

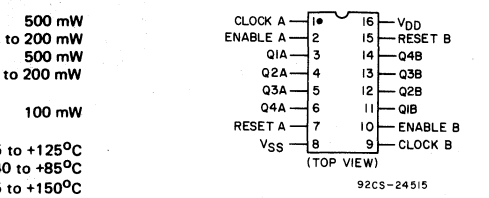
TRUTH TABLE

CLOCK	ENABLE	RESET	ACTION
⌐	1	0	Increment Counter
0	¬	0	Increment Counter
¬	X	0	No Change
X	⌐	0	No Change
⌐	0	0	No Change
1	¬	0	No Change
X	X	1	Q1 thru Q4 = 0

X = Don't Care 1 ≡ High State 0 ≡ Low State

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . –0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = –40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
PACKAGE TYPE E . . . . . –40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C



CD4518B, CD4520B TERMINAL ASSIGNMENT

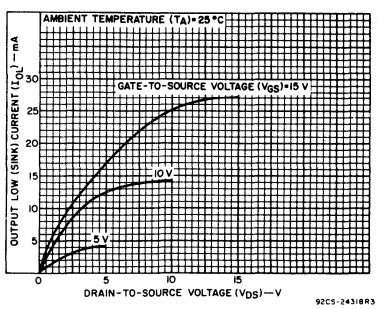


Fig. 1 – Typical output low (sink) current characteristics.

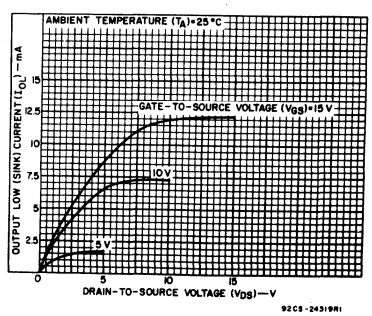


Fig. 2 – Minimum output low (sink) current characteristics.

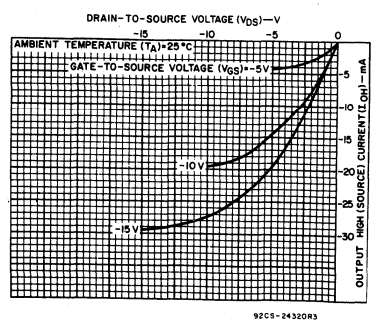


Fig. 3 – Typical output high (source) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	-	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

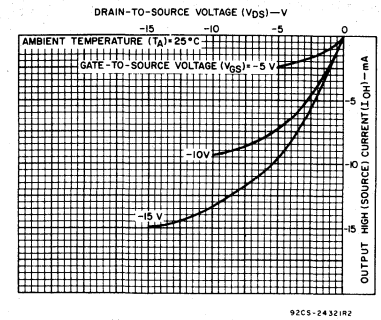


Fig. 4 — Minimum output high (source) current characteristics.

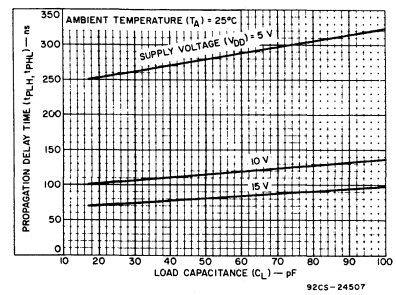


Fig. 5 — Typical propagation delay vs. load capacitance, reset to output.

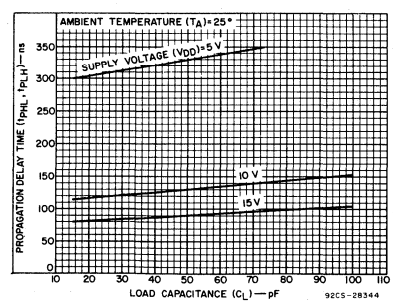


Fig. 6 — Typical propagation delay time vs. load capacitance, clock or enable to output.

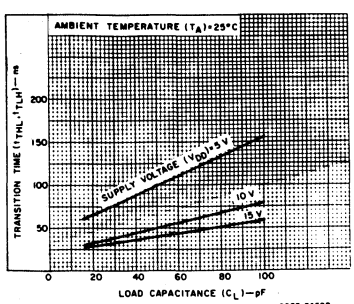


Fig. 7 — Typical transition time vs. load capacitance.

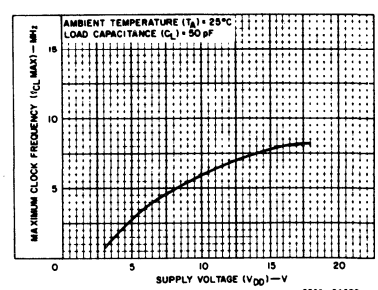


Fig. 8 — Typical maximum-clock-frequency vs. supply voltage.

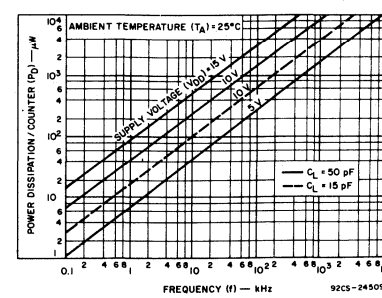


Fig. 9 — Typical power dissipation characteristics.

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)		3	18	V
Enable Pulse Width, t_W	5	400	–	ns
	10	200	–	
	15	140	–	
Clock Pulse Width, t_W	5	200	–	ns
	10	100	–	
	15	70	–	
Clock Input Frequency, f_{CL}	5	dc	1.5	MHz
	10		3	
	15		4	
Clock Rise or Fall Time, t_rCL or t_fCL:	5,10	–	15	μs
	15	–	5	
Reset Pulse Width, t_W	5	250	–	ns
	10	110	–	
	15	80	–	

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C;
Input t_r,t_f=20 ns, C_L=50 pF, R_L=200 KΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
	V_{DD} V	Min.	Typ.	Max.	
Propagation Delay Time, t_{PHL}, t_{PLH}: Clock or Enable to Output	5	–	280	560	ns
	10	–	115	230	
	15	–	80	160	
Reset to Output	5	–	330	650	
	10	–	130	225	
	15	–	90	170	
Transition Time, t_{THL}, t_{TLH}	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Maximum Clock Input Frequency, f_{CL}	5	1.5	3	–	MHz
	10	3	6	–	
	15	4	8	–	
Minimum Clock Pulse Width, t_W	5	-	100	200	ns
	10	-	50	100	
	15	-	35	70	
Clock Rise or Fall Time, t_r or t_f:	5,10	–	–	15	μs
	15	–	–	5	
Minimum Reset Pulse Width, t_W	5	–	125	250	ns
	10	–	55	110	
	15	–	40	80	
Minimum Enable Pulse Width, t_W	5	–	200	400	ns
	10	–	100	200	
	15	–	70	140	
Input Capacitance, C_{IN}	Any Input	–	–	5	7.5	pF
Clock Input Rise or Fall Time, t_{rcl}, t_{rcf}	5	–	–	15	μs
	10	–	–	5	
	15	–	–	5	

TEST CIRCUITS

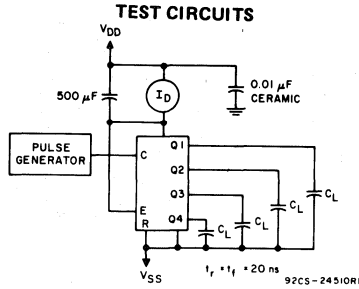


Fig. 10 – Dynamic power dissipation.

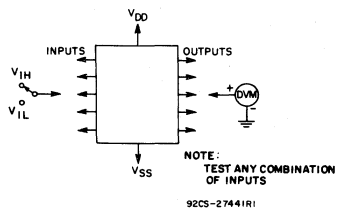


Fig. 11 – Input voltage.

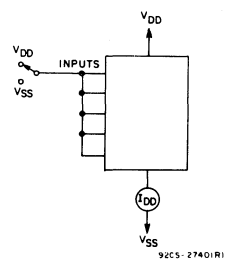


Fig. 12 – Quiescent device current test circuit.

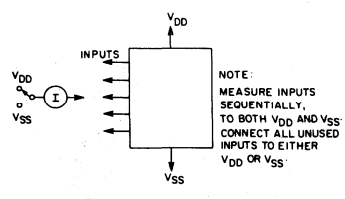


Fig. 13 – Input leakage-current test circuit.

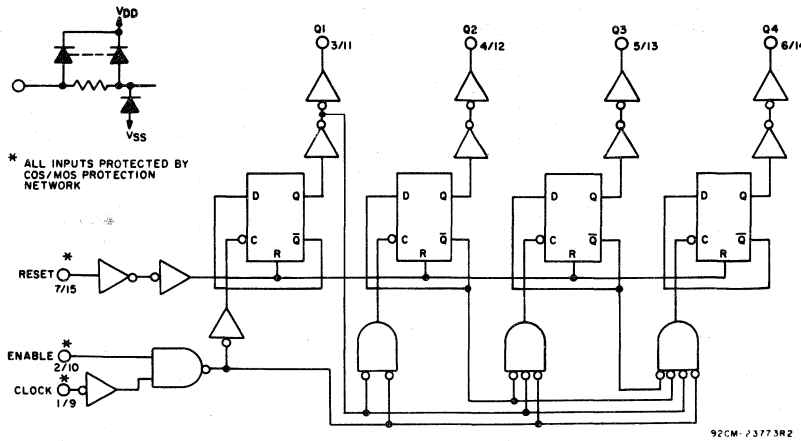


Fig. 14 — Binary counter (CD4520B) logic diagram for one of two identical counters.

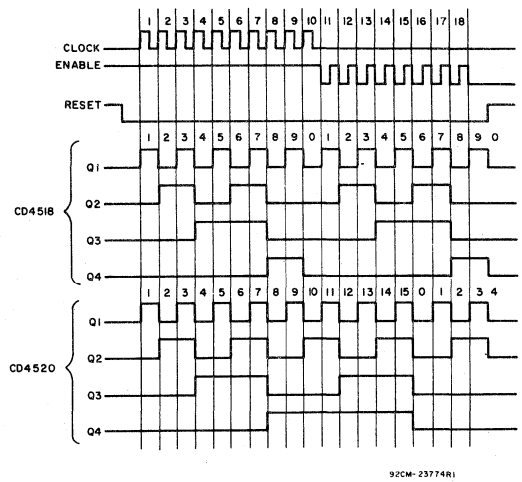


Fig. 15 — Timing diagrams for CD4518B and CD4520B.

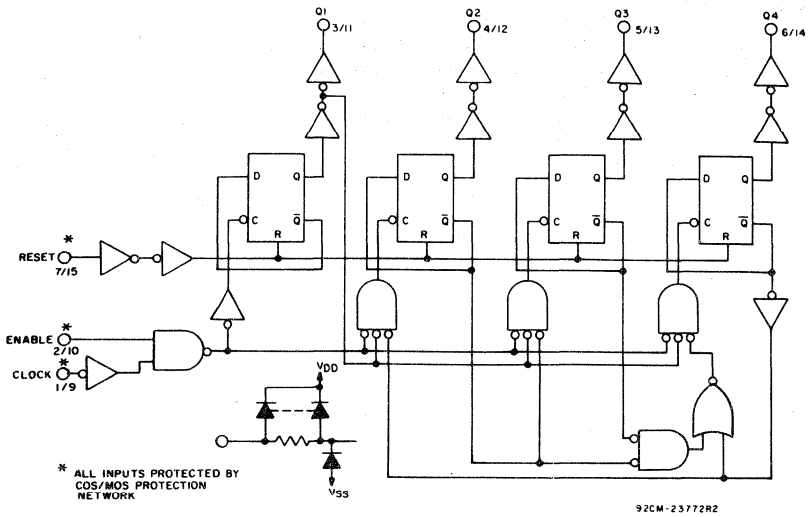
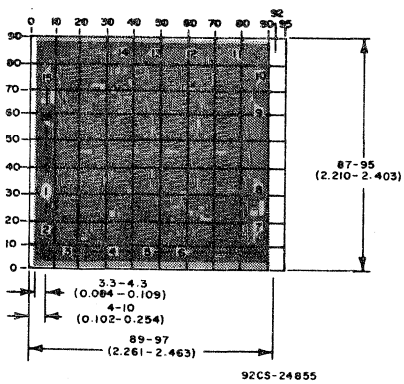
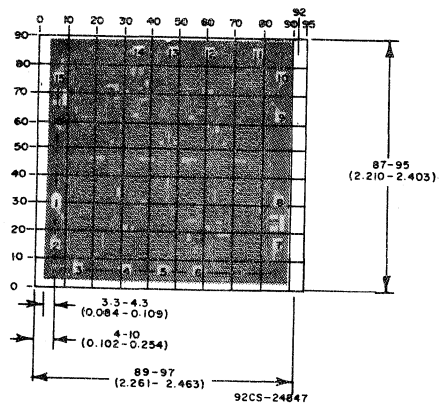


Fig. 16 — Decade counter (CD4518B) logic diagram for one of two identical counters.



Dimensions and pad layout for CD4518BH chip.



Dimensions and pad layout for CD4520BH chip.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS BCD Rate Multiplier

High-Voltage Types (20-Volt Rating)

The RCA-CD4527B is a low-power 4-bit digital rate multiplier that provides an output-pulse rate which is the clock-input-pulse rate multiplier by 1/10 times the BCD input. For example, when the BCD input is 8, there will be 8 output pulses for every 10 input pulses. This device may be used to perform arithmetic operations (add, subtract, divide, raise to a power), solve algebraic and differential equations, generate natural logarithms and trigonometric functions, A/D and D/A conversion, and frequency division.

For fractional multipliers with more than one digit, CD4527B devices may be cascaded in two different modes: the Add mode and the Multiply mode. (See Figs. 9 and 10). In the Add mode,

$$\text{Output Rate} = (\text{Clock Rate})\left[0.1\ BCD_1 + 0.01\ BCD_2 + 0.001\ BCD_3 + \cdots\right]$$

In the Multiply mode, the fraction programmed into the first rate multiplier is multiplied by the fraction programmed into the second one,

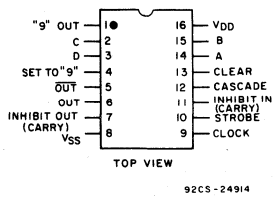
$$\text{e.g.}\ \frac{9}{10} \times \frac{4}{10} = \frac{36}{100}\ \text{or 36 output}$$

pulses for every 100 clock input pulses.

The CD4527B types are supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Applications:

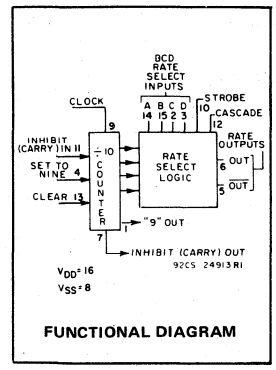
- **Numerical control**
- **Instrumentation**
- **Digital filtering**
- **Frequency synthesis**



TERMINAL ASSIGNMENT

Features:

- **Cascadable in multiples of 4-bits**
- **Set to "9" input and "9" detect output**
- **100% test for quiescent current at 20 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Standardized, symmetrical output characteristics**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (full package-temperature range) =**
  - **1 V at V_{DD} = 5 V**
  - **2 V at V_{DD} = 10 V**
  - **2.5 V at V_{DD} = 15 V**
- **Meets all requirements of JEDEC Tentative Standard No.13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**



FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

RECOMMENDED OPERATING CONDITIONS AT T_A = 25°C, Except as Noted.

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	18	V
Set or Clear Pulse Width, t_W	5	160	–	ns
	10	90	–	
	15	60	–	
Clock Pulse Width, t_W	5	330	–	ns
	10	170	–	
	15	100	–	
Clock Frequency, f_{CL}	5		1.2	MHz
	10	dc	2.5	
	15		3.5	
Clock Rise or Fall Time, t_{rCL} or t_{fCL}	5,10,15	–	15	μs
Inhibit In Setup Time, t_{SU}	5	100	–	ns
	10	40	–	
	15	20	–	
Inhibit In Removal Time, t_{REM}	5	240	–	ns
	10	130	–	
	15	110	–	
Set Removal Time, t_{REM}	5	150	–	ns
	10	80	–	
	15	50	–	
Clear Removal Time, t_{REM}	5	60	–	ns
	10	40	–	
	15	30	–	

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
									+25		
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5, 13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1, 9	–	10	7				7	–	–	
	1.5, 13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

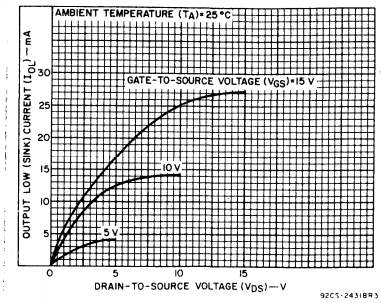


Fig.1 – Typical output low (sink) current characteristics.

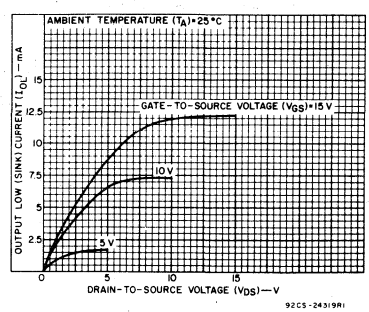


Fig.2 – Minimum output low (sink) current characteristics.

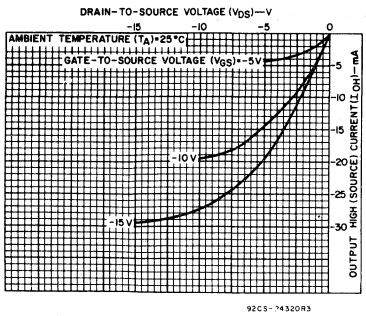


Fig.3 – Typical output high (source) current characteristics.

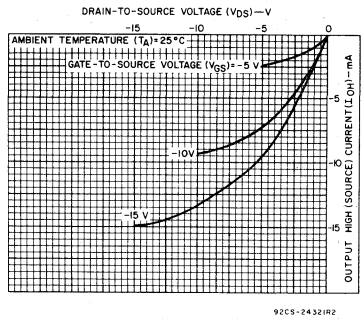


Fig.4 – Minimum output high (source) current characteristics.

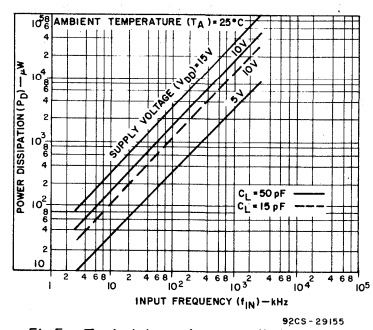


Fig.5 – Typical dynamic power dissipation as a function of input frequency.

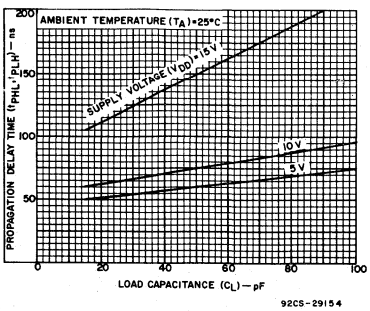


Fig.6 – Typical propagation delay time as a function of load capacitance (Clock or Strobe to Out).

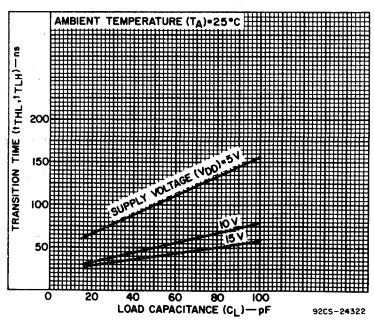


Fig.7 – Typical transition time as a function of load capacitance.

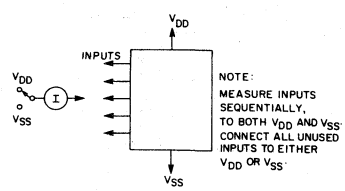


Fig.8 – Input current test circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$:
Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS				UNITS
		V_{DD} (V)	Min.	Typ.	Max.	
Propagation Delay Time, t_{PHL}, t_{PLH} Clock to $\overline{Out}$		5	–	110	220	ns
		10	–	55	110	
		15	–	45	90	
Clock or Strobe to Out		5	–	150	300	ns
		10	–	75	150	
		15	–	60	120	
Clock to Inhibit Out High Level to Low Level		5	–	320	640	ns
		10	–	145	290	
		15	–	100	200	
Low Level to High Level		5	–	250	500	ns
		10	–	100	200	
		15	–	75	150	
Clear to Out		5	–	380	760	ns
		10	–	175	350	
		15	–	130	260	
Clock to "9" or "15" Out		5	–	300	600	ns
		10	–	125	250	
		15	–	90	180	
Cascade to Out		5	–	90	180	ns
		10	–	45	90	
		15	–	35	70	
Inhibit In to Inhibit Out		5	–	130	260	ns
		10	–	60	120	
		15	–	45	90	
Set to Out		5	–	330	660	ns
		10	–	150	300	
		15	–	110	220	
Transition Time, t_{THL}, t_{TLH}		5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Maximum Clock Frequency, f_{CL}		5	1.2	2.4	–	MHz
		10	2.5	5	–	
		15	3.5	7	–	
Minimum Clock Pulse Width, t_W		5	–	165	330	ns
		10	–	85	170	
		15	–	50	100	
Clock Rise or Fall Time, t_{rCL}, t_{fCL}		5	–	–	15	μs
		10	–	–	15	
		15	–	–	15	
Minimum Set or Clear Pulse Width, t_W		5	–	80	160	ns
		10	–	45	90	
		15	–	30	60	
Minimum Inhibit In Setup Time, t_{SU}		5	–	50	100	ns
		10	–	20	40	
		15	–	10	20	
Minimum Inhibit In Removal Time, t_{REM}		5	–	120	240	ns
		10	–	65	130	
		15	–	55	110	
Minimum Set Removal Time, t_{REM}		5	–	75	150	ns
		10	–	40	80	
		15	–	25	50	
Minimum Clear Removal Time, T_{REM}		5	–	30	60	ns
		10	–	20	40	
		15	–	15	30	
Input Capacitance, C_{IN}	Any Input		–	5	7.5	pF

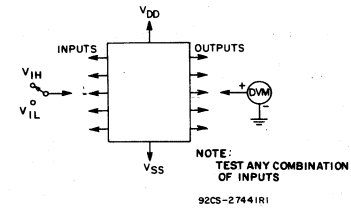


Fig.9 – Input voltage test circuit.

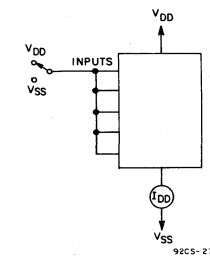


Fig.10 – Quiescent device current test circuit.

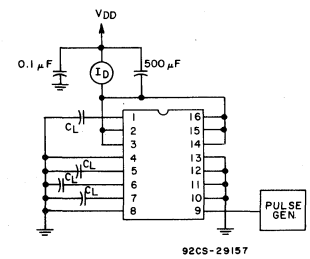


Fig.11 – Dynamic power dissipation test circuit.

APPLICATIONS

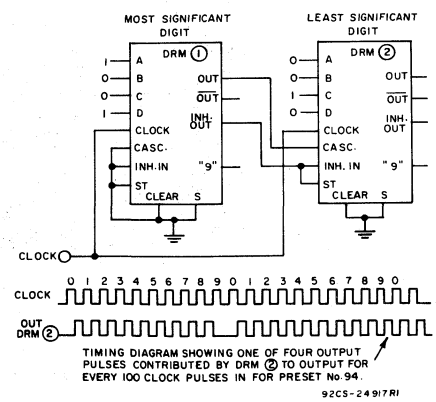


Fig.12 – Two CD4527B's cascaded in the "Add" mode with a preset number of 94 $\left(\frac{9}{10} + \frac{4}{100} = \frac{94}{100}\right)$.

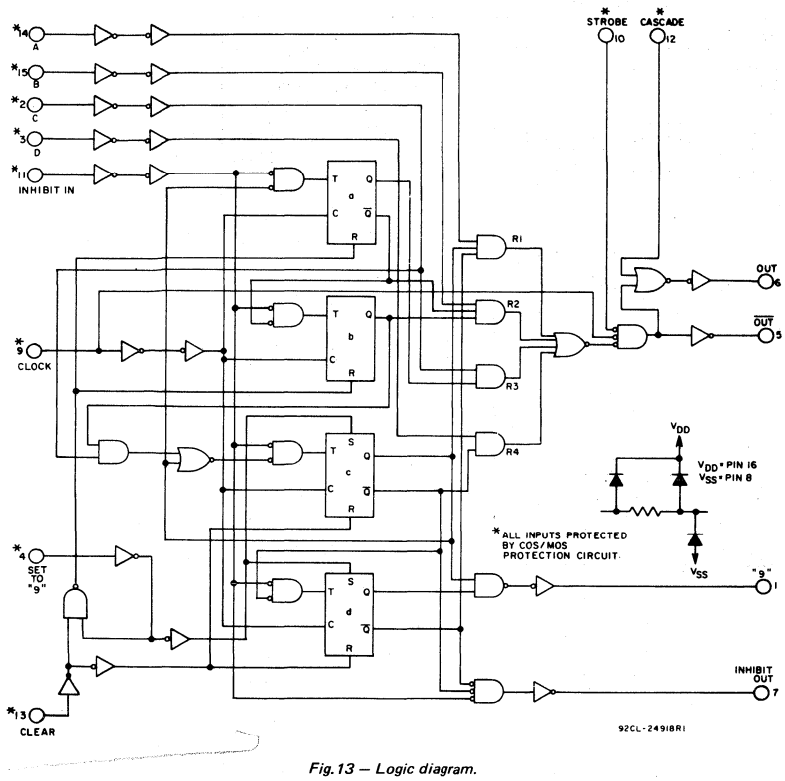


Fig. 13 – Logic diagram.

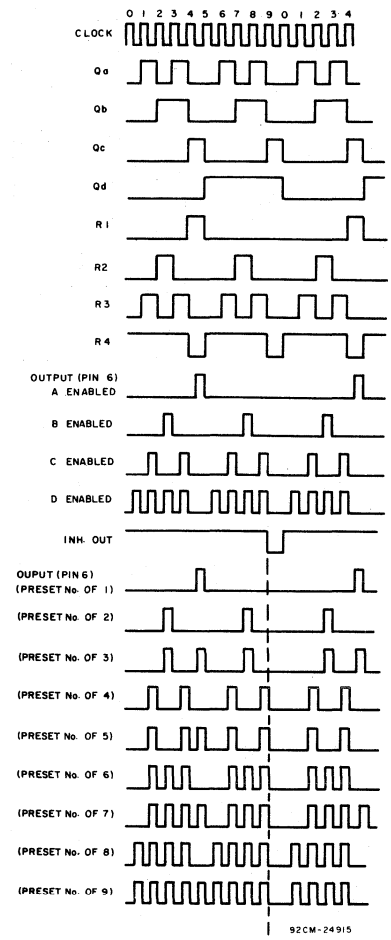
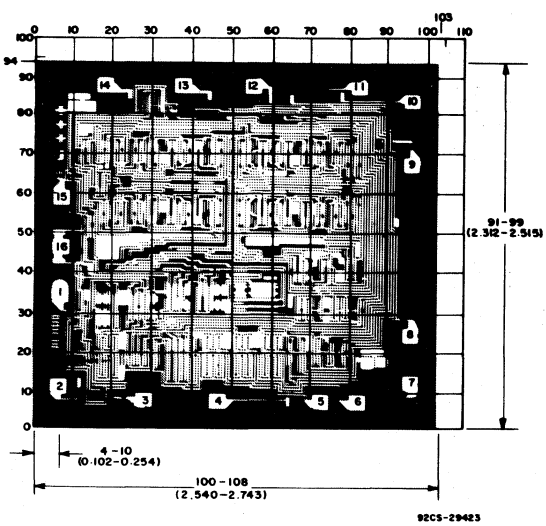


Fig. 14 – Timing diagram (See Logic Diagram).



Dimensions and Pad Layout for CD4527BH

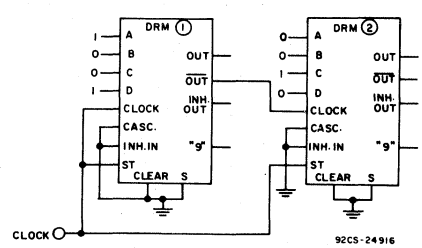


Fig. 15 – Two CD4527B's cascaded in the "Multiply" mode with a preset number of 36 $\left(\frac{9}{10} \times \frac{4}{10} = \frac{36}{100}\right)$.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

TRUTH TABLE

INPUTS										OUTPUTS			
Number of Pulses or Input Logic Level (0 = Low; 1 = High; X = Don't Care)										Number of Pulses or Output Logic Level (L = Low; H = High)			
D	C	B	A	CLK	INH IN	STR	CAS	CLR #	SET #	OUT	$\overline{OUT}$	INH OUT	"9" OUT
0	0	0	0	10	0	0	0	0	0	L	H	1	1
0	0	0	1	10	0	0	0	0	0	1	1	1	1
0	0	1	0	10	0	0	0	0	0	2	2	1	1
0	0	1	1	10	0	0	0	0	0	3	3	1	1
0	1	0	0	10	0	0	0	0	0	4	4	1	1
0	1	0	1	10	0	0	0	0	0	5	5	1	1
0	1	1	0	10	0	0	0	0	0	6	6	1	1
0	1	1	1	10	0	0	0	0	0	7	7	1	1
1	0	0	0	10	0	0	0	0	0	8	8	1	1
1	0	0	1	10	0	0	0	0	0	9	9	1	1
1	0	1	0	10	0	0	0	0	0	8	8	1	1
1	0	1	1	10	0	0	0	0	0	9	9	1	1
1	1	0	0	10	0	0	0	0	0	8	8	1	1
1	1	0	1	10	0	0	0	0	0	9	9	1	1
1	1	1	0	10	0	0	0	0	0	8	8	1	1
1	1	1	1	10	0	0	0	0	0	9	9	1	1
X	X	X	X	10	1	0	0	0	0	†	†	H	†
X	X	X	X	10	0	1	0	0	0	L	H	1	1
X	X	X	X	10	0	0	1	0	0	H	*	1	1
1	X	X	X	10	0	0	0	1	0	10	10	H	L
0	X	X	X	10	0	0	0	1	0	L	H	H	L
X	X	X	X	10	0	0	0	0	1	L	H	L	H

* Output same as the first 16 lines of this truth table (depending on values of A, B, C, D).

†Depends on internal state of counter.

#Clear and Set Inputs should not be high at the same time; device draws increased quiescent current when in this non-valid state.

COS/MOS 8-Bit Priority Encoder

High-Voltage Types (20-Volt Rating)

The RCA-CD4532B consists of combinational logic that encodes the highest priority input (D7-D0) to a 3-bit binary code. The eight inputs, D7 through D0, each have an assigned priority; D7 is the highest priority and D0 is the lowest. The priority encoder is inhibited when the chip-enable input E_I is low. When E_I is high, the binary representation of the highest-priority input appears on output lines Q2-Q0, and the group select line GS is high to indicate that priority inputs are present. The enable-out (E_O) is high when no priority inputs are present. If any one input is high, E_O is low and all cascaded lower-order stages are disabled.

The CD4532B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

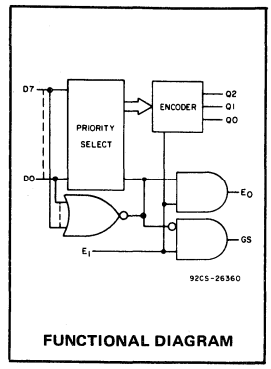
This device is similar to type MC14532.

Features:

- **Converts from 1 of 8 to binary**
- **Provides cascading feature to handle any number of inputs**
- **Group select indicates one or more priority inputs**
- **Standardized, symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (full package-temperature range):**
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

- **Priority encoder**
- **Binary or BCD encoder (keyboard encoding)**
- **Floating point arithmetic**



FUNCTIONAL DIAGRAM

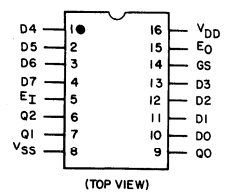
RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	Min.	Max.	Units
Supply Voltage Range (for T_A= Full Package Temp. Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C



TERMINAL ASSIGNMENT

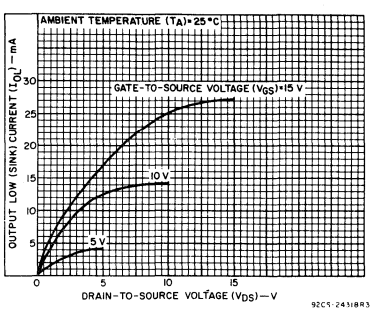


Fig. 1 — Typical output low (sink) current characteristics.

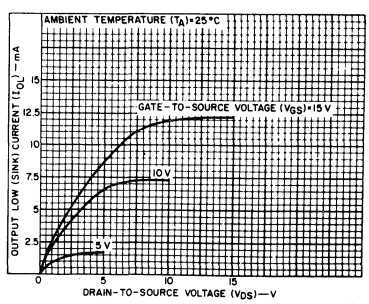


Fig. 2 — Minimum output low (sink) current characteristics.

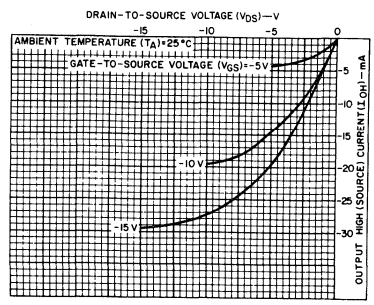


Fig. 3 — Typical output high (source) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C; C_L=50 pF, Input t_r,t_f= 20 ns, R_L=200 KΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} VOLTS	LIMITS ALL TYPES TYP.	LIMITS ALL TYPES MAX.	UNITS
Propagation Delay Time t_{PHL}, t_{PLH} E_I to E_O, E_I to GS	5	110	220	ns
	10	55	110	
	15	45	85	
E_I to Qm, Dn to GS	5	170	340	
	10	85	170	
	15	65	125	
Dn to Q_M	5	220	440	
	10	110	220	
	15	85	160	
Transition Time t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Input Capacitance C_{IN}	Any Input	5	7.5	pF

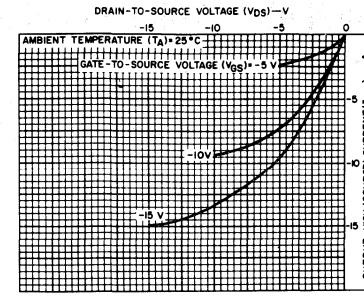


Fig. 4 — Minimum output high (source) current characteristics.

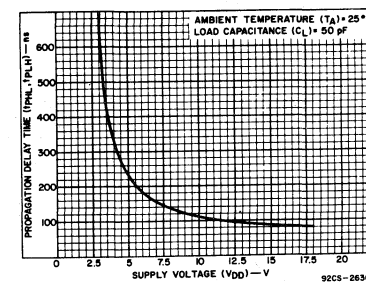


Fig. 5 — Typical propagation delay (Dn to Qm) vs. supply voltage.

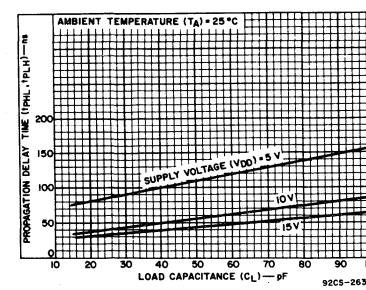


Fig. 6 — Typical propagation delay (E_I to GS, E_I to E_O) vs. load capacitance.

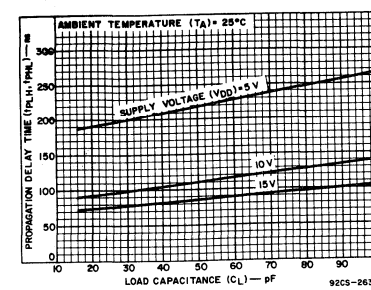


Fig. 7 — Typical propagation delay (Dn to Qm) vs. load capacitance.

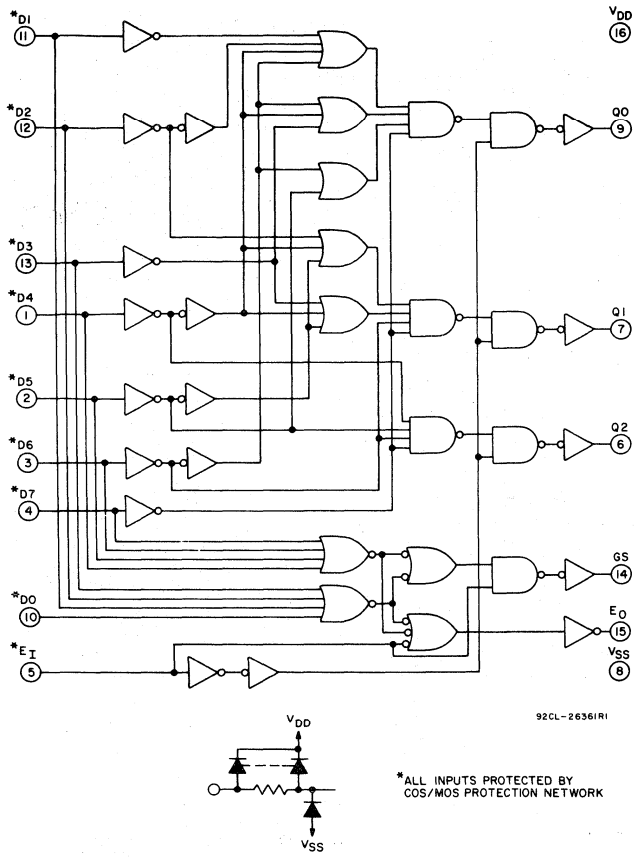


Fig. 8 — CD4532 logic diagram.

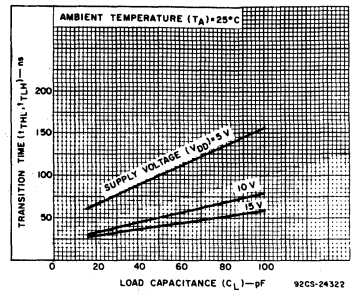


Fig.9 — Typical transition time vs. load capacitance.

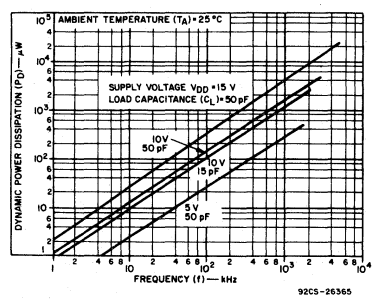


Fig.10 — Typical dynamic power dissipation vs. frequency.

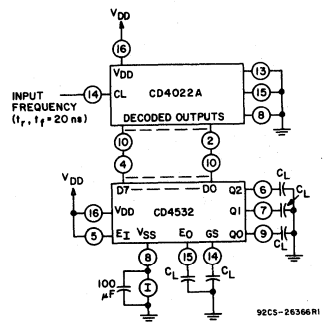


Fig.11 — Dynamic power dissipation test circuit.

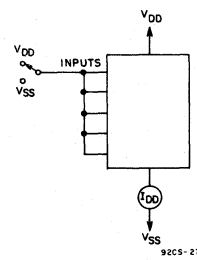


Fig.12 — Quiescent device current test circuit.

TRUTH TABLE

Input									Output				
E_I	D7	D6	D5	D4	D3	D2	D1	D0	GS	Q2	Q1	Q0	E_O
0	X	X	X	X	X	X	X	X	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	X	X	X	X	X	X	X	1	1	1	1	0
1	0	1	X	X	X	X	X	X	1	1	1	0	0
1	0	0	1	X	X	X	X	X	1	1	0	1	0
1	0	0	0	1	X	X	X	X	1	1	0	0	0
1	0	0	0	0	1	X	X	X	1	0	1	1	0
1	0	0	0	0	0	1	X	X	1	0	1	0	0
1	0	0	0	0	0	0	1	X	1	0	0	1	0
1	0	0	0	0	0	0	0	1	1	0	0	0	0

X = Don't Care Logic 1 ≡ High Logic 0 ≡ Low

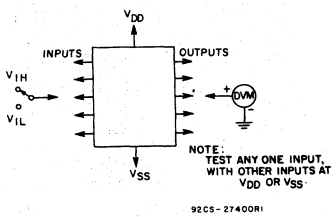


Fig. 13 – Input voltage test circuit.

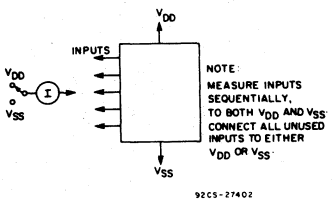
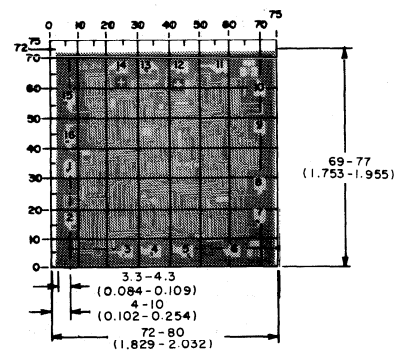


Fig. 14 – Input current test circuit.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions and pad layout for CD4532BH.

APPLICATIONS

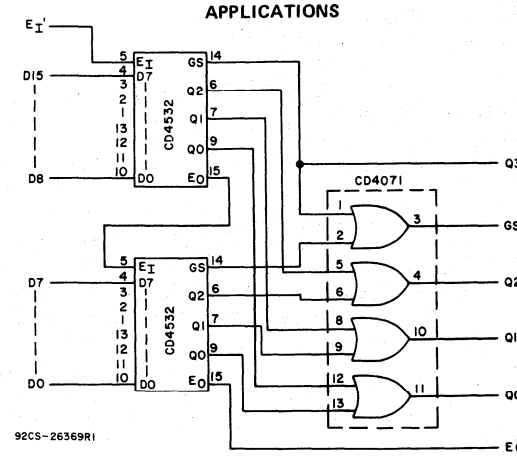
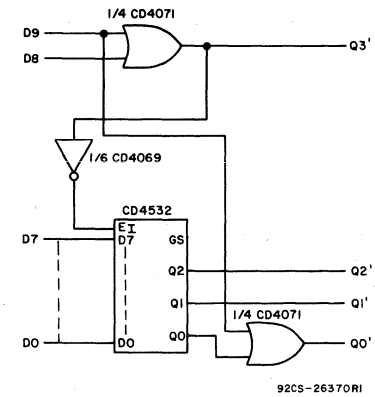


Fig. 15 – 16-level priority encoder.



TRUTH TABLE

Input										Output				
D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	GS	Q3'	Q2'	Q1'	Q0'
1	X	X	X	X	X	X	X	X	X	0	1	0	0	1
0	1	X	X	X	X	X	X	X	X	0	1	0	0	0
0	0	1	X	X	X	X	X	X	X	1	0	1	1	1
0	0	0	1	X	X	X	X	X	X	1	0	1	1	0
0	0	0	0	1	X	X	X	X	X	1	0	1	0	1
0	0	0	0	0	1	X	X	X	X	1	0	1	0	0
0	0	0	0	0	0	1	X	X	X	1	0	0	1	1
0	0	0	0	0	0	0	1	X	X	1	0	0	1	0
0	0	0	0	0	0	0	0	1	X	1	0	0	0	1
0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

X = Don't Care Logic 1 ≡ High Logic 0 ≡ Low

Fig. 16 – 0-to-9 keyboard encoder.

COS/MOS Dual Binary to 1 of 4 Decoder/Demultiplexers

High-Voltage Types (20-Volt Rating)

CD4555B: Outputs High on Select
CD4556B: Outputs Low on Select

The RCA-CD4555B and CD4556B are dual one-of-four decoders/demultiplexers. Each decoder has two select inputs (A and B), an Enable input ($\overline{E}$), and four mutually exclusive outputs. On the CD4555B the outputs are high on select; on the CD4556B the outputs are low on select.

When the Enable input is high, the outputs of the CD4555B remain low and the outputs of the CD4556B remain high regardless of the state of the select inputs A and B. The CD4555B and CD4556B are similar to types MC14555 and MC14556, respectively.

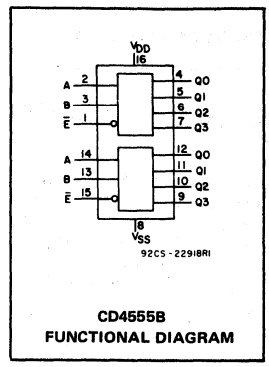
The CD4555B and CD4556B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead-dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

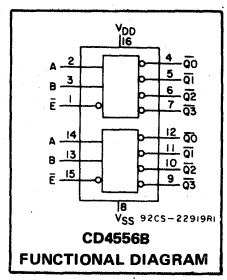
- Expandable with multiple packages
- Standard, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range): 1 V at V_{DD} = 5 V, 2 V at V_{DD} = 10 V, 2.5 V at V_{DD} = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Decoding
- Code conversion
- Demultiplexing (using Enable input as a data input)
- Memory chip-enable selection
- Function selection



CD4555B
FUNCTIONAL DIAGRAM



CD4556B
FUNCTIONAL DIAGRAM

RECOMMENDED OPERATING CONDITIONS

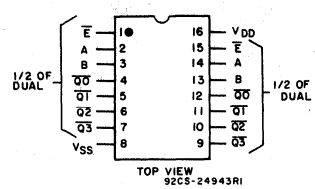
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	V_{DD}	MIN.	MAX.	UNITS
Supply Voltage Range (For T_A = Full Package Temp. Range)	–	3	18	V

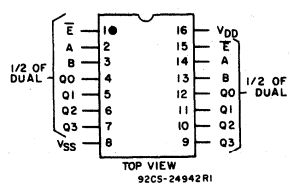
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . –0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = –40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
PACKAGE TYPE E . . . . . –40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

TERMINAL ASSIGNMENTS



CD4556B



CD4555B

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9,5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				—	—	1.5	
	1,9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	—	—	
	1,9	–	10	7				7	—	—	
	1.5,13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ*

CHARACTERISTIC	TEST CONDITIONS	ALL TYPES LIMITS		UNITS
		V_{DD} Volts	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH} A or B Input to Any Output		5	220	440	ns
		10	95	190	
		15	70	140	
$\overline{E}$ Input to Any Output		5	200	400	ns
		10	85	170	
		15	65	130	
Transition Time t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance C_{IN}	Any Input		5	7.5	pF

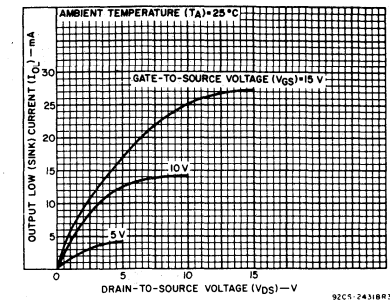


Fig. 1 — Typical output low (sink) current characteristics.

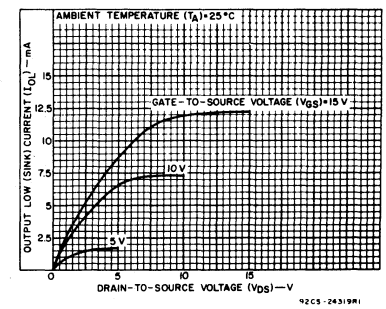


Fig. 2 — Minimum output low (sink) current characteristics.

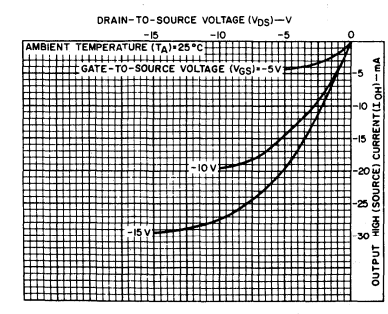


Fig. 3 — Typical output high (source) current characteristics.

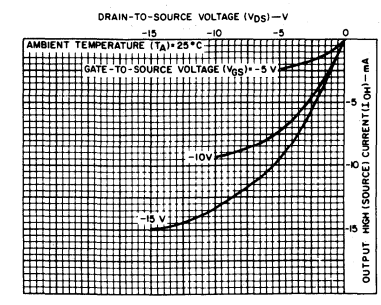


Fig. 4 — Minimum output high (source) current characteristics.

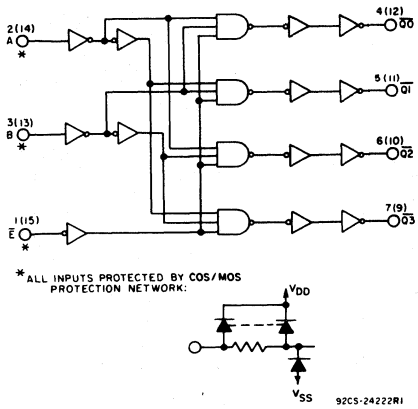


Fig. 5 — CD4556B logic diagram (1 of 2 identical circuits).

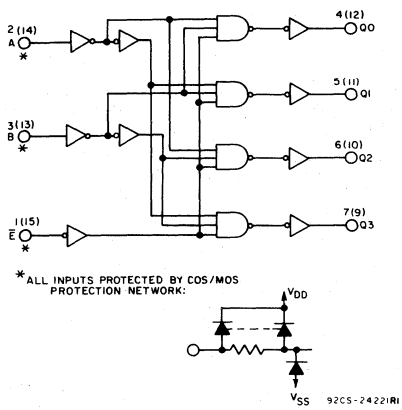


Fig. 6 — CD4555B logic diagram (1 of 2 identical circuits).

TRUTH TABLE

INPUTS			OUTPUTS CD4555B				OUTPUTS CD4556B			
ENABLE	SELECT									
Ē	B	A	Q3	Q2	Q1	Q0	$\overline{Q3}$	$\overline{Q2}$	$\overline{Q1}$	$\overline{Q0}$
0	0	0	0	0	0	1	1	1	1	0
0	0	1	0	0	1	0	1	1	0	1
0	1	0	0	1	0	0	1	0	1	1
0	1	1	1	0	0	0	0	1	1	1
1	X	X	0	0	0	0	1	1	1	1

X = DON'T CARE

LOGIC 1 ≡ HIGH
LOGIC 0 ≡ LOW

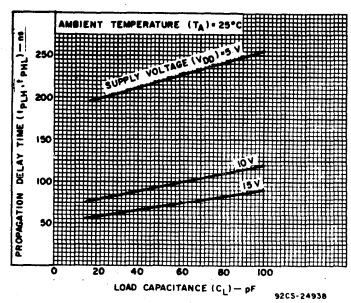


Fig. 7 — Typical propagation delay time vs. load capacitance (A or B input to any output).

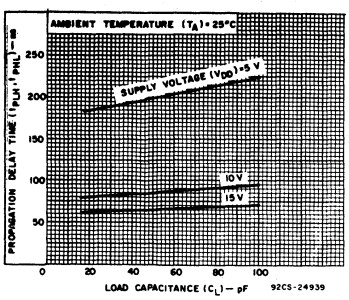


Fig. 8 — Typical propagation delay time vs. load capacitance (Ē input to any output).

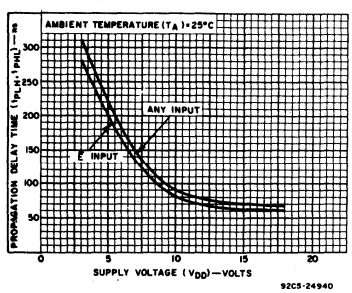


Fig. 9 — Typical propagation delay time vs. supply voltage.

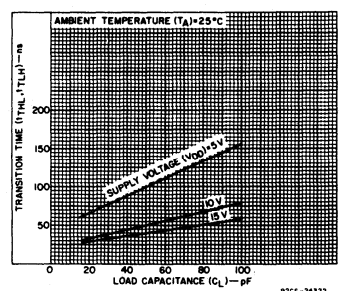


Fig. 10 — Typical transition time vs. load capacitance.

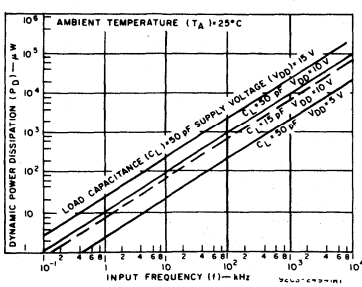


Fig. 11 — Typical dynamic power dissipation vs. frequency.

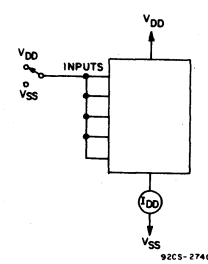


Fig. 12 — Quiescent device current test circuit.

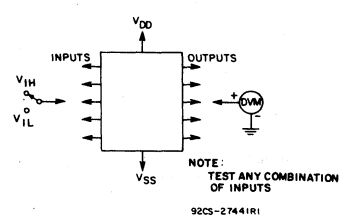


Fig. 13 — Input voltage test circuit.

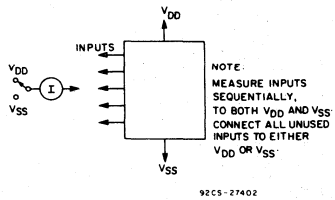


Fig. 14 – Input current test circuit.

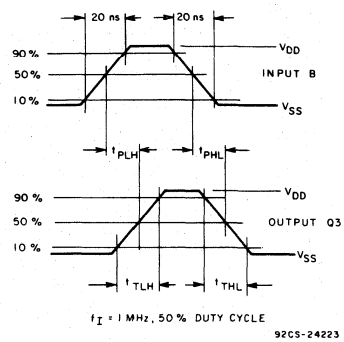


Fig. 15 – CD4555B B input to Q3 output dynamic signal waveforms.

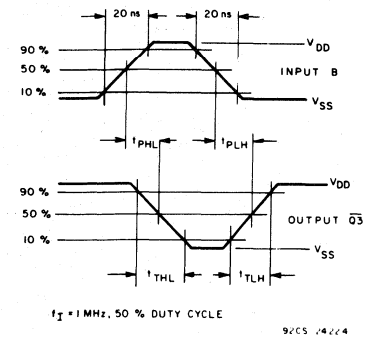


Fig. 16 – CD4556B B input to $\overline{Q3}$ output dynamic signal waveforms.

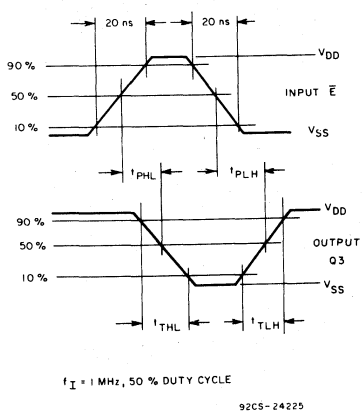


Fig. 17 – CD4555B $\overline{E}$ input to Q3 output dynamic signal waveforms.

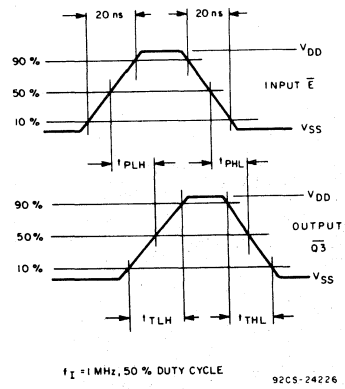
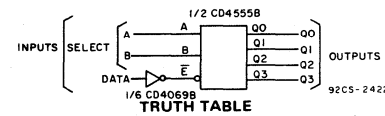


Fig. 18 – CD4556B $\overline{E}$ input to $\overline{Q}_3$ output dynamic signal waveforms.

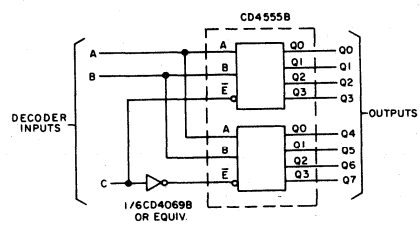
APPLICATIONS



TRUTH TABLE

SELECT INPUTS		OUTPUTS			
B	A	Q0	Q1	Q2	Q3
0	0	DATA	0	0	0
0	1	0	DATA	0	0
1	0	0	0	DATA	0
1	1	0	0	0	DATA

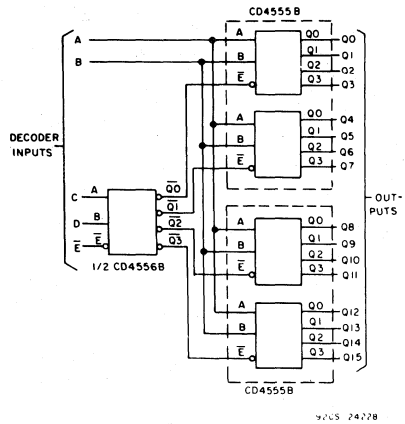
Fig. 19 – 1-of-4 line data demultiplexer using CD4555B.



TRUTH TABLE

INPUTS			Q OUTPUTS							
C	B	A	0	1	2	3	4	5	6	7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Fig. 20 – 1-of-8 decoder using CD4555B.

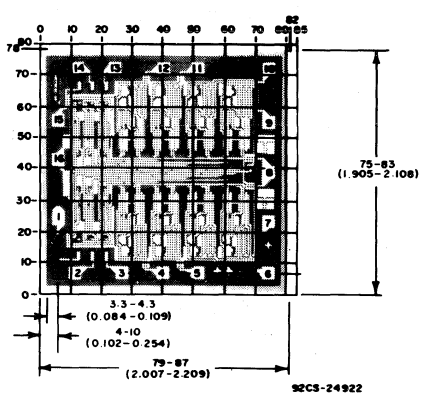


TRUTH TABLE

INPUTS					Q OUTPUTS															
E	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
1	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

X = don't care

Fig. 21 — 1-of-16 decoder using CD4555B and CD4556B.



DIMENSIONS AND PAD LAYOUT FOR CD4555BH. *(Dimensions and pad layout for CD4556BH are identical).*

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS 32-Stage Static Left/Right Shift Register

High-Voltage Types (20-Volt Rating)

The RCA-CD40100B is a 32-stage shift register containing 32 D-type master-slave flip-flops.

The data present at the SHIFT-RIGHT INPUT is transferred into the first register stage synchronously with the positive CLOCK edge, provided the LEFT/RIGHT CONTROL is at a low level, the RECIRCULATE CONTROL is at a high level, and the CLOCK INHIBIT is low. If the LEFT/RIGHT CONTROL is at a high level and the RECIRCULATE CONTROL is also high, data at the SHIFT-LEFT INPUT is transferred into the 32nd register stage synchronously with the positive CLOCK transition, provided the CLOCK INHIBIT is low. The state of the LEFT/RIGHT CONTROL, RECIRCULATE CONTROL, and CLOCK INHIBIT should not be changed when the CLOCK is high.

Data is shifted one stage left or one stage right depending on the state of the LEFT/RIGHT CONTROL, synchronously with the positive CLOCK edge. Data clocked into the first or 32nd register states is available at the SHIFT-LEFT or SHIFT-RIGHT OUTPUT respectively, on the next negative CLOCK transition (see Data Transfer Table). No shifting occurs on the positive CLOCK edge if the CLOCK INHIBIT line is at a high level. With the RECIRCULATE CONTROL low, data in the 32nd stage is shifted into the first stage when the LEFT/RIGHT CONTROL is low and from the 1st stage to the 32nd stage when the LEFT/RIGHT CONTROL is high.

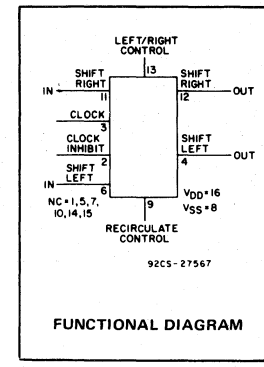
The CD40100B types are supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Fully static operation**
- **Shift left/Shift right capability**
- **Multiple package cascading**
- **Recirculate capability**
- **LIFO or FIFO capability**
- **Standardized, symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (full package-temperature range) =**
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

- **Serial shift registers**
- **Time delay circuits**
- **Expandable N-bit data storage stack (LIFO operation)**



FUNCTIONAL DIAGRAM

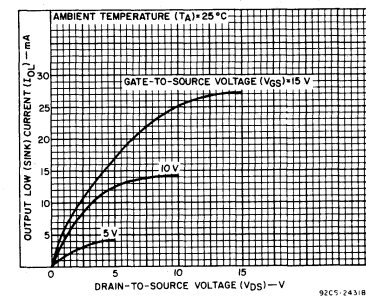


Fig. 1 – Typical output low (sink) current characteristics.

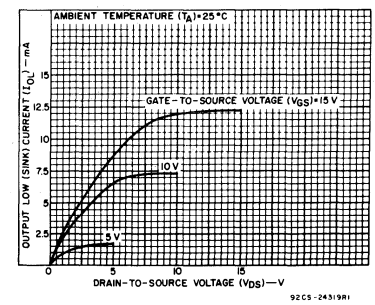


Fig. 2 – Minimum output low (sink) current characteristics.

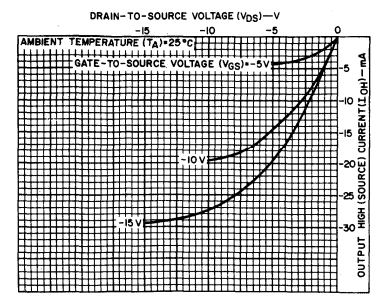


Fig. 3 – Typical output high (source) current characteristics.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

RECOMMENDED OPERATING CONTITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	18	V
Data Setup Time, t_S	5	0	–	ns
	10	0	–	
	15	0	–	
Data Hold Time, t_H	5	275	–	ns
	10	100	–	
	15	75	–	
Clock Input Frequency, f_{CL}	5		1	mHz
	10	dc	2.5	
	15		3	
Clock Input Rise or Fall Time, t_rCL, t_fCL	5	–	15	μs
	10	–	15	
	15	–	15	
Clock Input Pulse Width: Low Level, t_{WL}	5	450	–	ns
	10	230	–	
	15	190	–	
High Level, t_{WH}	5	280	–	ns
	10	150	–	
	15	140	–	

CONTROL TRUTH TABLE

LEFT/RIGHT CONTROL	CLOCK INHIBIT	RECIRCULATE CONTROL	ACTION	INPUT BIT ORIGIN
1	0	1	Shift left	Shift left input
1	0	0	Shift left	Stage 1
0	0	1	Shift right	Shift right input
0	0	0	Shift right	Stage 32
X	1	X	No shift	–

DATA TRANSFER TABLE*

INITIAL STATE			CLOCK	RESULTING STATE	
DATA INPUT	CLOCK INHIBIT	INTERNAL STAGE	LEVEL CHANGE	INTERNAL STAGE Q	OUTPUT
0	0	X		0	NC
X	0	0		NC	0
1	0	X		1	NC
X	0	1		NC	1
X	1	1	X	NC	NC

0 = Low level 1 = High level X = Don't care NC = No change

* For Shift-Right Mode
Data Input = SHIFT-RIGHT INPUT (Term. 11)
Internal Stage = Stage 1 (Q_1)
Output = SHIFT-LEFT OUTPUT (Term. 4)

For Shift-Left Mode
Data Input = SHIFT-LEFT INPUT (Term. 6)
Internal Stage = Stage 32 (Q_{32})
Output = SHIFT-RIGHT OUTPUT (Term. 12)

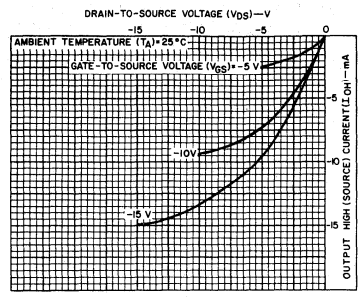


Fig. 4 – Minimum output high (source) current characteristics.

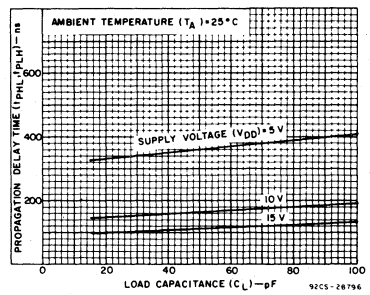


Fig. 5 – Typical propagation delay time (CLOCK to SHIFT LEFT/RIGHT) as a function of load capacitance.

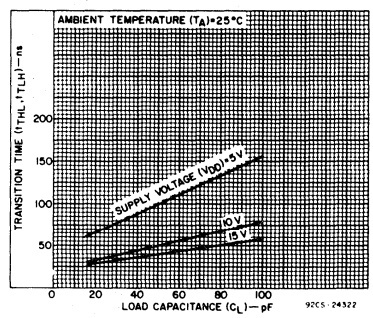


Fig. 6 – Typical transition time as a function of load capacitance.

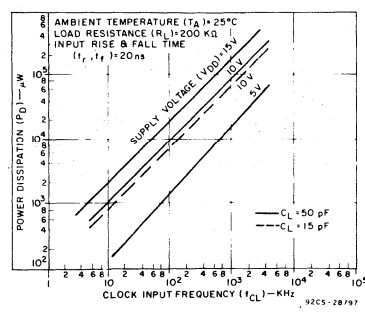


Fig. 7 – Typical dynamic power dissipation as a function of CLOCK frequency.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	-	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

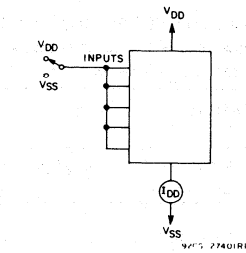


Fig. 8 – Quiescent device current test circuit.

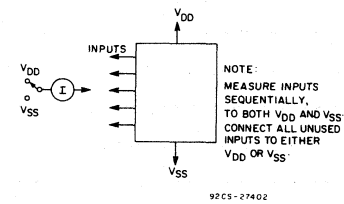


Fig. 9 – Input current test circuit.

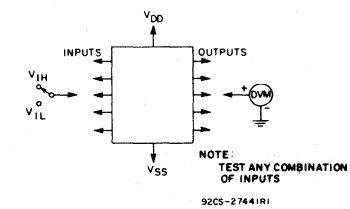
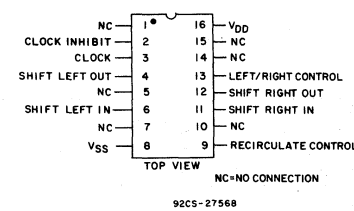


Fig. 10 – Input voltage test circuit.



TERMINAL ASSIGNMENT

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS				UNITS
		V_{DD} V	Min.	Typ.	Max.	
Propagation Delay Time: Clock to Shift Left/Right Output, t_{PLH}, t_{PHL}		5		360	720	ns
		10		165	330	
		15		115	230	
Transition Time, t_{THL}, t_{TLH}		5		100	200	ns
		10		50	100	
		15		40	80	
Minimum Data Setup Time, t_S		5		−40	0	ns
		10		−20	0	
		15		−10	0	
Minimum Data Hold Time, t_H		5		170	275	ns
		10		75	100	
		15		50	75	
Maximum Clock Input Frequency, f_{CL}		5	1	2		MHz
		10	2.5	5		
		15	3	6		
Minimum Clock Input Pulse Width: Low Level, t_{WL}		5		225	450	ns
		10		115	230	
		15		95	190	
High Level, t_{WH}		5		140	280	ns
		10		75	150	
		15		70	140	
Input Capacitance, C_{IN}	Any Input	–		5	7.5	pF

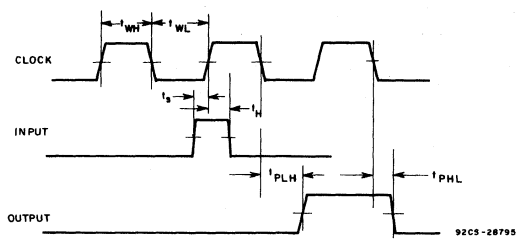


Fig. 11 – Timing diagram defining setup, hold, and propagation delay times.

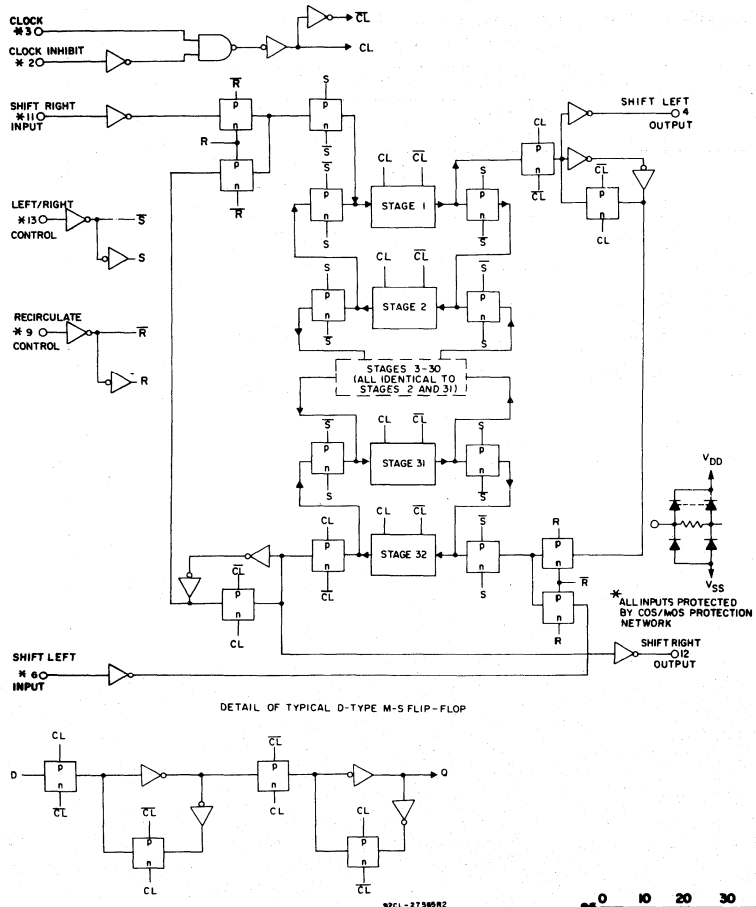
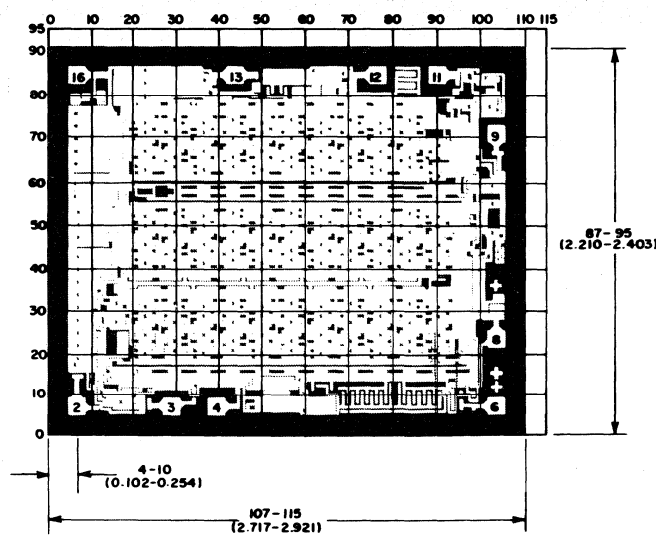


Fig. 12 — Logic diagram.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.



Dimensions and pad layout for CD40100BH.

COS/MOS 9-Bit Parity Generator/Checker

High-Voltage Types (20-Volt Rating)

The RCA-CD40101B is a 9-bit (8 data bits plus 1 parity bit) parity generator/checker. It may be used to detect errors in data transmission or data retrieval. Odd and even outputs facilitate odd or even parity generation and checking.

When used as a parity generator, a parity bit is supplied along with the data to generate an even or odd parity output.

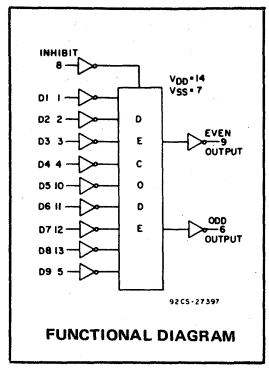
When used as a parity checker, the received data bits and parity bits are compared for correct parity. The even or odd outputs are used to indicate an error in the received data.

Word-length capability is expandable by cascading. The CD40101B is also provided with an inhibit control. If the inhibit control is set at logical "1", the even and odd outputs go to a logical "0".

The CD40101B types are supplied in 14-lead dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **100% tested for maximum quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (full package-temperature range): 1 V at V_{DD} = 5 V; 2 V at V_{DD} = 10 V; 2.5 V at V_{DD} = 15 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Standardized, symmetrical output characteristics**
- **Meets all requirements of JEDEC Tentative Standard No.13A, "Standard Specifications for Description of 'B' Series CMOS Devices."**

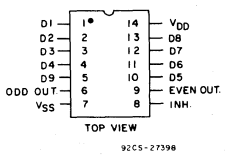


FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

TERMINAL ASSIGNMENT



RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

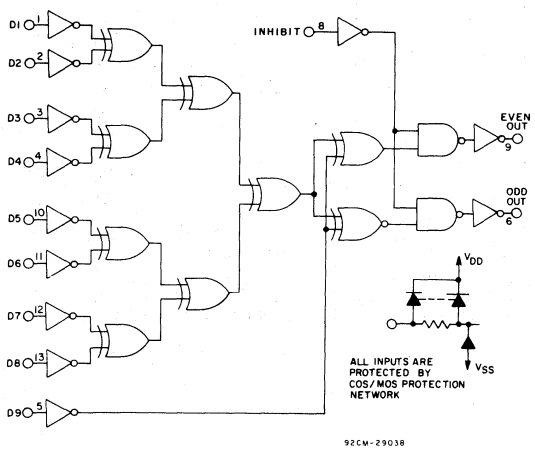


Fig.1 – CD40101B logic diagram.

Truth Table

Inputs		Outputs	
D1-D9	Inhibit	Even	Odd
Σ1's=Even	0	1	0
Σ1's=Odd	0	0	1
X	1	0	0

X = Don't Care
Logic 1 = High
Logic 0 = Low

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1, 9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS
	V_{DD} (V)	Typ.	Max.	
Data Propagation Delay Time, t_{PHL}, t_{PLH}	5	350	700	ns
	10	150	300	
	15	100	200	
Inhibit-to-Output Propagation Delay Time, t_{PHL}, t_{PLH}	5	140	280	
	10	70	140	
	15	50	100	
Transition Time, t_{THL}, t_{TLH}	5	100	200	
	10	50	100	
	15	40	80	
Input Capacitance, C_{IN}	Any Input	5	7.5	pF

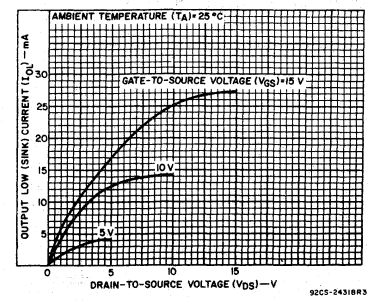


Fig.2 – Typical output low (sink) current characteristics.

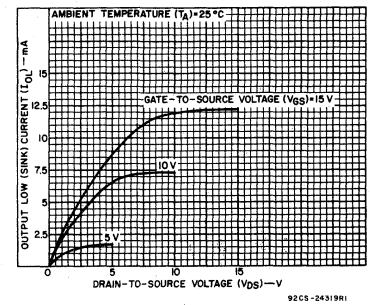


Fig.3 – Minimum output low (sink) current characteristics.

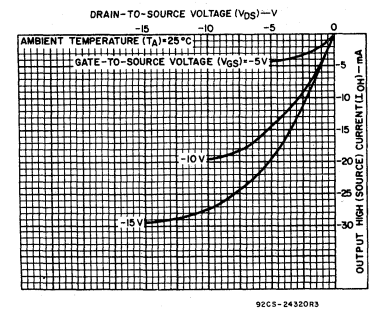


Fig.4 – Typical output high (source) current characteristics.

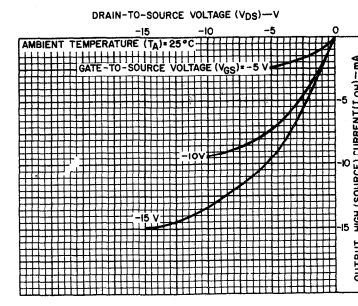


Fig.5 – Minimum output high (source) current characteristics.

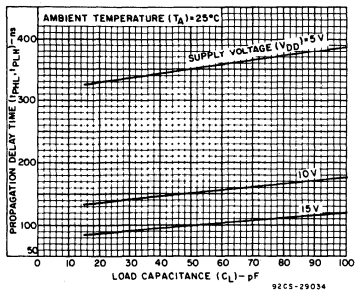


Fig.6 – Typical propagation delay time as a function of load capacitance.

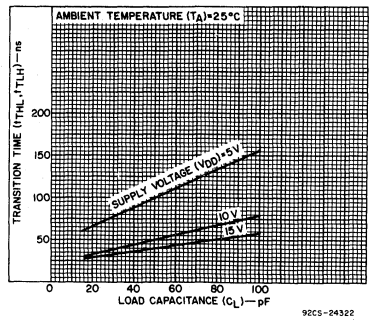


Fig.7 – Transition time as a function of load capacitance.

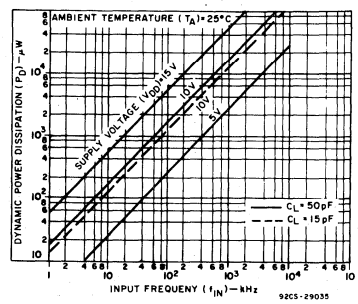


Fig.8 – Dynamic power dissipation as a function of input frequency.

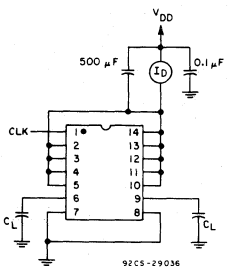


Fig.9 – Dynamic power dissipation test circuit.

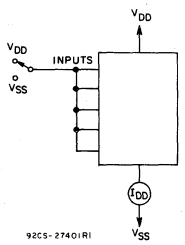


Fig.10 – Quiescent-device-current test circuit.

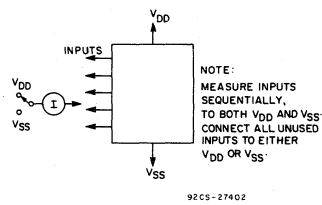


Fig.11 – Input-leakage current.

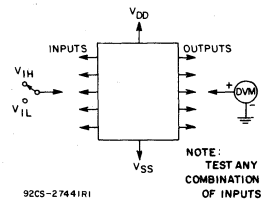
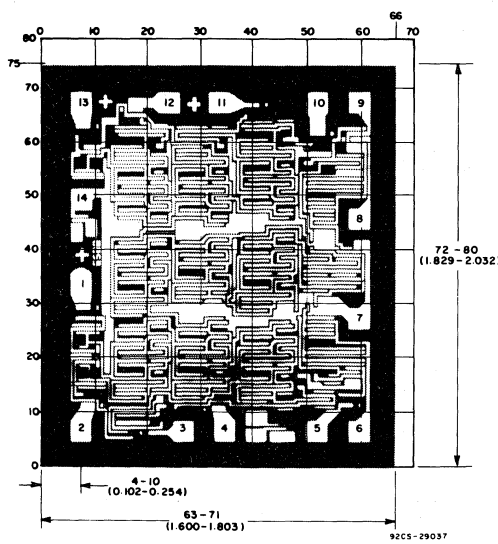


Fig.12 – Input-voltage test circuit.

DIMENSIONS AND PAD LAYOUT FOR CD40101B



The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

COS/MOS 8-Stage Presettable Synchronous Down Counters

High-Voltage Types (20-Volt Rating)

CD40102B – 2-Decade BCD Type
CD40103B – 8-Bit Binary Type

The RCA-CD40102B, and CD40103B consist of an 8-stage synchronous down counter with a single output which is active when the internal count is zero. The CD40102B is configured as two cascaded 4-bit BCD counters, and the CD40103B contains a single 8-bit binary counter: Each type has control inputs for enabling or disabling the clock, for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the CARRY-OUT/ZERO-DETECT output are active-low logic.

In normal operation, the counter is decremented by one count on each positive transition of the CLOCK. Counting is inhibited when the CARRY-IN/COUNTER ENABLE ($\overline{CI/CE}$) input is high. The CARRY-OUT/ZERO-DETECT ($\overline{CO/ZD}$) output goes low when the count reaches zero if the $\overline{CI/CE}$ input is low, and remains low for one full clock period.

When the SYNCHRONOUS PRESET-ENABLE ($\overline{SPE}$) input is low, data at the JAM input is clocked into the counter on the next positive clock transition regardless of the state of the $\overline{CI/CE}$ input. When the ASYNCHRONOUS PRESET-ENABLE ($\overline{APE}$) input is low, data at the JAM inputs is asynchronously forced into the counter regardless of the state of the $\overline{SPE}$, $\overline{CI/CE}$, or CLOCK inputs. JAM inputs JO-J7 represent two 4-bit BCD words for the CD40102B and a single 8-bit binary word for the CD40103B.

When the CLEAR ($\overline{CLR}$) input is low, the counter is asynchronously cleared to its maximum count (99_{10} for the CD40102B and 255_{10} for the CD40103B) regardless of the state of any other input. The precedence relationship between control inputs is indicated in the truth table.

If all control inputs are high at the time of zero count, the counters will jump to the maximum count, giving a counting sequence of 100 or 256 clock pulses long.

The CD40102B and CD40103B may be cascaded using the $\overline{CI/CE}$ input and the $\overline{CO/ZD}$ output, in either a synchronous or ripple mode as shown in Figs.21 and 22.

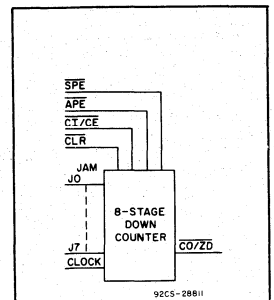
The CD40102B and CD40103B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Synchronous or asynchronous preset**
- **Medium-speed operation: f_{CL} = 3.6 MHz (typ.) @ V_{DD} = 10 V**
- **Cascadable**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (full package-temperature range) = 1 V at V_{DD} = 5 V, 2 V at V_{DD} = 10 V, 2.5 V at V_{DD} = 15 V**
- **Standardized, symmetrical output characteristics**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No.13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

- **Divide-by-"N" counters**
- **Programmable timers**
- **Interrupt timers**
- **Cycle/program counter**



CD40102B, CD40103B
FUNCTIONAL DIAGRAM

RECOMMENDED OPERATING CONDITIONS AT T_A = 25°C, Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V_{DD}	Min.	Max.	Units
Supply Voltage Range (At T_A = Full Package-Temperature Range)		3	18	V
Clock Pulse Width, t_W	5	300	–	ns
	10	180	–	
	15	80	–	
$\overline{Clear}$ Pulse Width, t_W	5	320	–	ns
	10	160	–	
	15	100	–	
$\overline{APE}$ Pulse Width, t_W	5	360	–	ns
	10	160	–	
	15	120	–	
Clock Input Frequency, f_{CL}	5	–	0.7	MHz
	10	–	1.8	
	15	–	2.4	
Clock Rise and Fall Time, t_rCL, t_fCL	5	–	15	μs
	10	–		
	15	–		
$\overline{SPE}$ Setup Time, t_{SU}	5	280	–	ns
	10	140	–	
	15	100	–	
Jam Setup Time, t_{SU}	5	200	–	ns
	10	80	–	
	15	60	–	

CD40102B, CD40103B Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . 0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

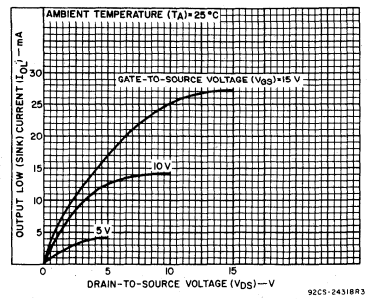


Fig. 1 — Typical output low (sink) current characteristics.

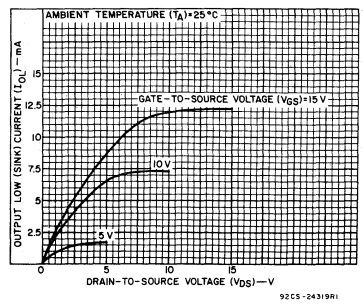


Fig. 2 — Minimum output low (sink) current characteristics.

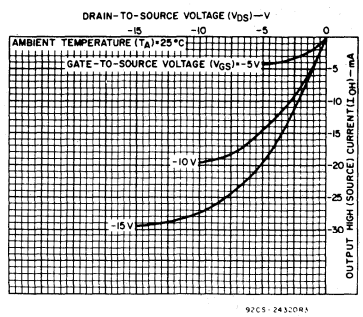


Fig. 3 — Typical output high (source) current characteristics.

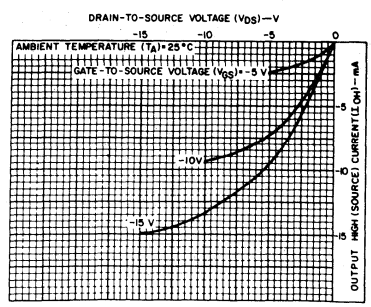


Fig. 4 — Minimum output high (source) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
									+25		
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	-	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 50 pF, Input t_r, t_f = 20 ns, R_L = 200 kΩ

Characteristic	Conditions V_{DD} (V)	Limits All Packages Min.	Typ.	Max.	Units
Propagation Delay Time (t_{PHL}, t_{PLH}):					
Clock-to-Output (See Fig.10)	5	–	300	600	ns
	10	–	130	260	
	15	–	95	190	
Carry In/Counter Enable-to-Output	5	–	200	400	
	10	–	90	180	
	15	–	65	130	
Asynchronous Preset Enable-to-Output	5	–	650	1300	
	10	–	300	600	
	15	–	200	400	
$\overline{\text{Clear}}$-to-Output	5	–	375	750	
	10	–	180	360	
	15	–	100	200	
Transition Time (t_{THL},t_{TLH}) (See Fig.9)	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Minimum Clock Pulse Width, (t_W)	5	–	150	300	ns
	10	–	90	180	
	15	–	40	80	
Minimum $\overline{\text{CLR}}$ Pulse Width (t_W)	5	–	160	320	
	10	–	80	160	
	15	–	50	100	
Minimum $\overline{\text{APE}}$ Pulse Width (t_W)	5	–	180	360	
	10	–	80	160	
	15	–	60	120	
Minimum $\overline{\text{SPE}}$ Set-Up Time (t_{SU})	5	–	140	280	
	10	–	70	140	
	15	–	50	100	
Minimum JAM Set-Up Time (t_{SU})	5	–	100	200	
	10	–	40	80	
	15	–	30	60	
Maximum Clock Input Frequency (f_{CL}) (See Fig.11)	5	0.7	1.4	–	MHz
	10	1.8	3.6	–	
	15	2.4	4.8	–	
Input Capacitance (C_{IN})		–	5	7.5	pF

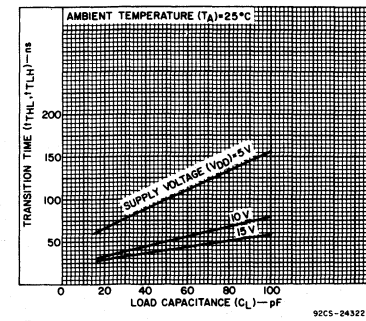


Fig. 5 — Typical transition time as a function of load capacitance.

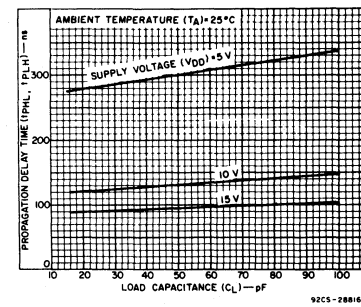


Fig. 6 — Typical propagation delay time as a function of load capacitance (clock to CO/ZD).

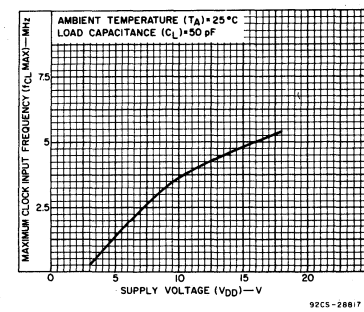


Fig. 7 — Typical maximum clock input frequency as a function of supply voltage.

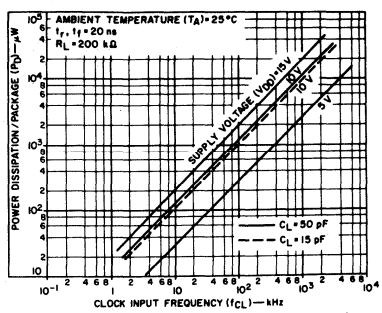


Fig. 8 — Typical dynamic power dissipation as a function of frequency.

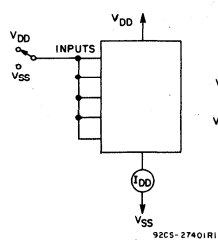


Fig. 9 — Quiescent device current test circuit.

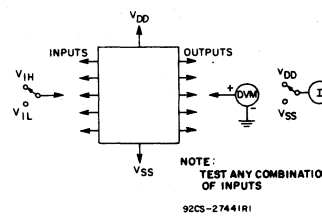


Fig. 10 — Input voltage test circuit.

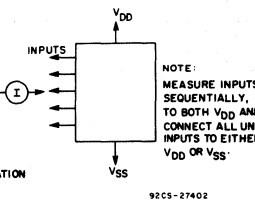


Fig. 11 — Input current test circuit.

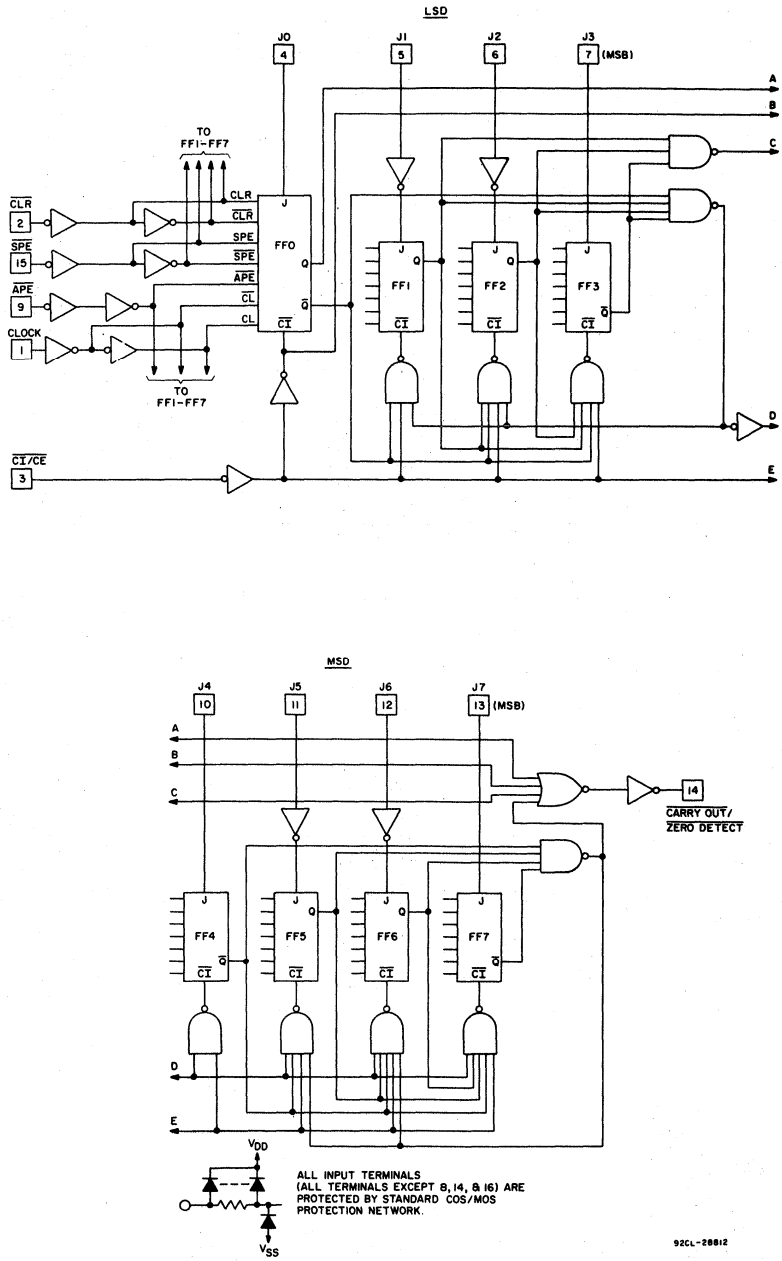


Fig. 12 – Logic diagram for CD40102B.

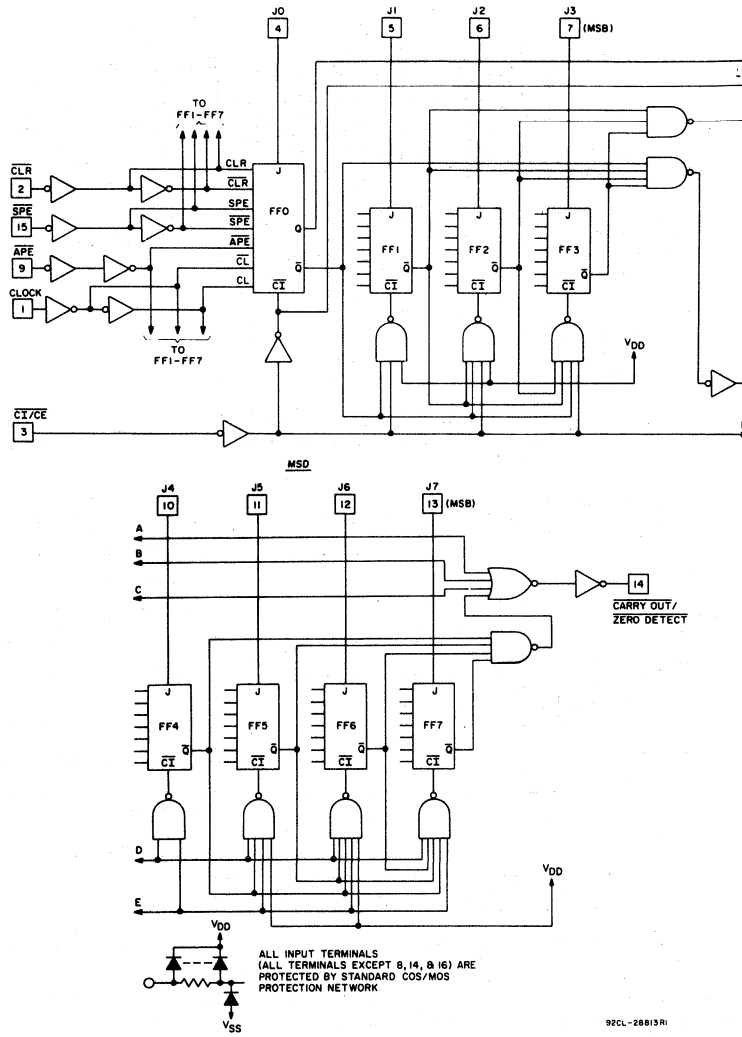


Fig. 13 – Logic diagram for CD40103B.

TRUTH TABLE

CONTROL INPUTS				PRESET MODE	ACTION
$\overline{CLR}$	$\overline{APE}$	$\overline{SPE}$	$\overline{CI}/\overline{CE}$		
1	1	1	1	Synchronous	Inhibit counter
1	1	1	0		Count down
1	1	0	X		Preset on next positive clock transition
1	0	X	X	Asynchronous	Preset asynchronously
0	X	X	X		Clear to maximum count

Notes: 1. 0 = Low level
1 = High level
X = Don't care

2. Clock connected to clock input
3. Synchronous operation: changes occur on negative-to-positive clock transitions
4. JAM inputs: CD40102B BCD; MSD = J7,J6,J5,J4 (J7 is MSB)
LSD = J3,J2,J1,J0 (J3 is MSB)
CD40103B Binary; MSB = J7, LSB = J0

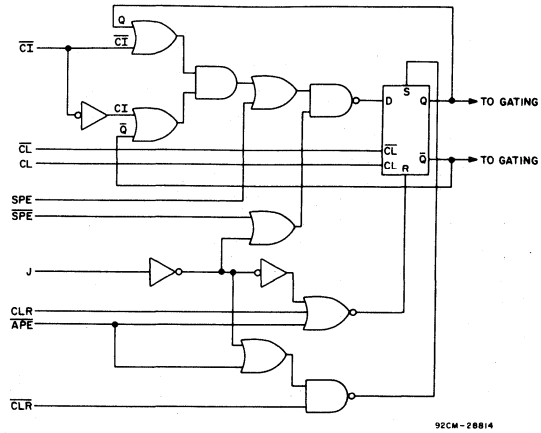


Fig. 14 – Detail logic diagram for flip-flops, FFO – FF7, used in logic diagrams for CD40102B and CD40103B.

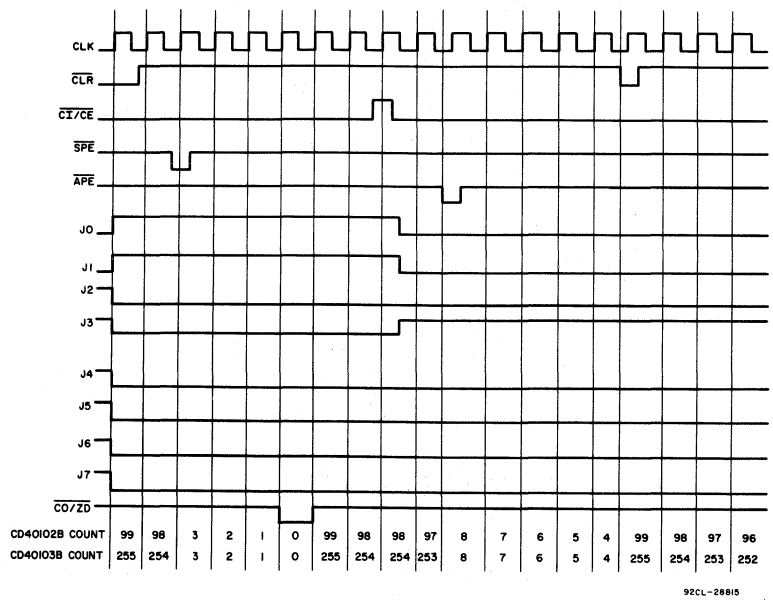
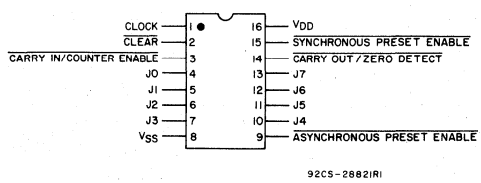


Fig. 15 – Timing diagram for CD40102B and CD40103B.



CD40102B, CD40103B

TERMINAL ASSIGNMENT

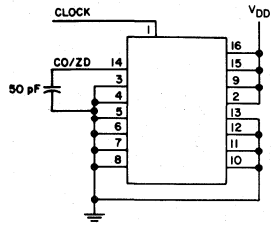


Fig.16 – Maximum clock frequency test circuit.

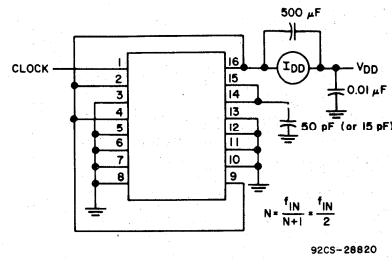


Fig.17 – Dynamic power dissipation test circuit (÷2 mode).

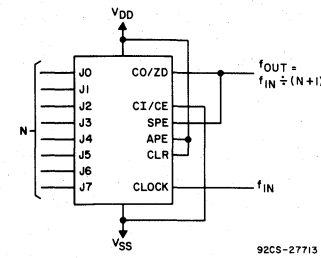


Fig.18 – Divide-by-"N" counter.

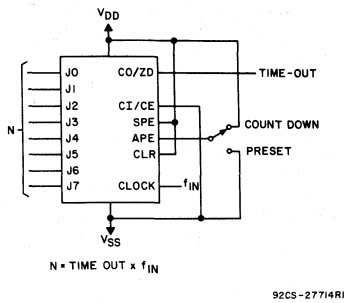


Fig.19 – Programmable timer.

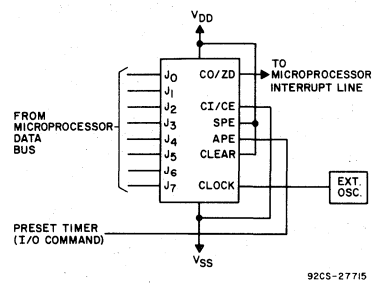
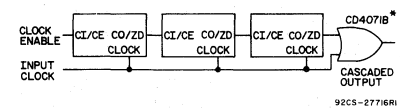


Fig.20 – Microprocessor interrupt timer.



* An output spike (160 ns @ V_{DD} = 5 V) occurs whenever two or more devices are cascaded in the parallel-clocked mode because the clock-to-carry out delay is greater than the carry-in-to-carry out delay. This spike is eliminated by gating the output of the last device with the clock as shown.

Fig.21 – Synchronous cascading.

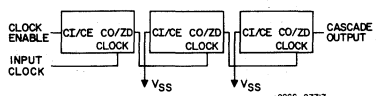
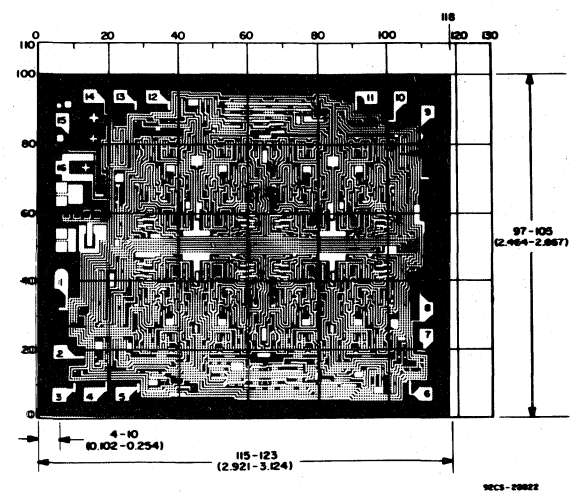


Fig.22 – Ripple cascading.

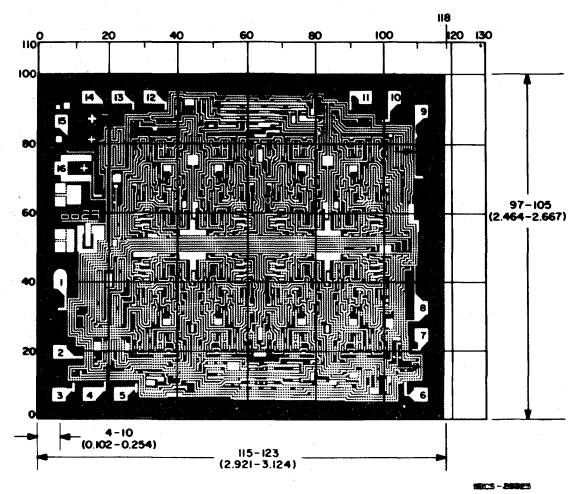
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17mm) larger in both dimensions.

Dimensions and pad layout for CD40102B.



Dimensions and pad layout for CD40103B.



CD40104B Types

Preliminary Data

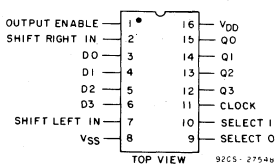
COS/MOS 4-Bit Bidirectional Universal Register

High-Voltage Types (20-Volt Rating)

The RCA-CD40104B is a universal register featuring parallel inputs, parallel outputs, shift-right and shift-left serial inputs, and a high-impedance third output state allowing the device to be used in bus-organized systems.

In the parallel-load mode, data is loaded into the associated flip-flop and appears at the output after the positive transition of the clock input. During loading, serial data flow is inhibited. Shift-right and shift-left are accomplished synchronously on the positive clock edge with serial data entered at the shift-right and shift-left serial inputs, respectively. Clearing the register is accomplished by setting both mode controls low and clocking the register. The mode controls should be changed only when the clock input is low. When the output enable input is low, all outputs assume the high impedance state.

The CD40104B types are supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).



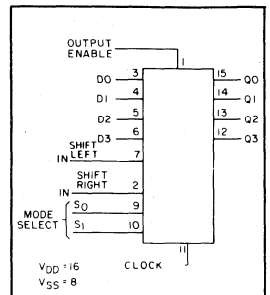
TERMINAL ASSIGNMENT

Features:

- **Medium speed operation—f_{CL} = 9 MHz (typ.) at V_{DD} = 10 V**
- **Fully static operation**
- **Synchronous parallel or serial operation**
- **Three-state outputs**
- **100% tested for quiescent current at 20 V**
- **Standardized,symmetrical output characteristics**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

- **Arithmetic unit bus registers**
- **Serial/parallel conversions**
- **General-purpose register for bus-organized systems**



92CS-24816R2

FUNCTIONAL DIAGRAM

CONTROL TRUTH TABLE

CLOCK▲	MODE S_0	SELECT S_1	OUTPUT ENABLE	ACTION
⎍	0	0	1	Reset
⎍	1	0	1	Shift right (Q_0 toward Q_3)
⎍	0	1	1	Shift left (Q_3 toward Q_0)
⎍	1	1	1	Parallel load
X	X	X	0	Outputs assume high impedance

1 = High level
0 = Low level
X = Don't care
▲ = Level change

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1		mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6		
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8		
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	1		
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2		
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6		
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				–	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS *at $T_A = 25°$ C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ*

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	TYPICAL VALUES	UNITS
Propagation Delay Time: Clock to Q t_{PHL}, t_{PLH}	5	375	ns
	10	150	
	15	110	
3-State Output 1 or 0 to High Impedance (Note) t_{PHZ}, t_{PLZ}	5	120	ns
	10	50	
	15	40	
3-State Output High Impedance to 1 or 0 (Note) t_{PZH}, t_{PZL}	5	150	ns
	10	60	
	15	45	
Output Transition Time t_{THL}, t_{TLH}	5	100	ns
	10	50	
	15	40	
Minimum Setup Time: D0, D3, Shift-Right In, Shift-Left In, to Clock t_S	5	60	ns
	10	25	
	15	20	
Select 0, Select 1 to Clock t_S	5	170	ns
	10	70	
	15	50	
Minimum Hold Time: D0, D3, Shift-Right In, Shift-Left In, Select 0, Select 1 to Clock t_H	5	0	ns
	10	0	
	15	0	
Minimum Clock Pulse Width t_W	5	85	ns
	10	35	
	15	25	
Maximum Clock Input Frequency f_{CL}	5	4	MHz
	10	9	
	15	12	
Maximum Clock Input Rise or Fall Time t_{fCL}, t_{rCL}	5	15	μs
	10	5	
	15	5	
Input Capacitance C_{IN}	Any Input	5	pF

NOTE: Measured at the point of 10% change in output with an output load of 50 pF, R_L = 1 kΩ to V_{DD} for t_{PZL}, t_{PLZ} and R_L = 1 kΩ to V_{SS} for t_{PZH}, t_{PHZ}.

Preliminary Data

COS/MOS FIFO Register

4 Bits Wide X 16 Bits Long
High-Voltage Types (20-Volt Rating)

The RCA-CD40105B is a low-power 4-bit-wide-by-16-bit-long first-in-first-out (FIFO) register whose 4 X 16 data register is under constant control of a logic network. Each word position in the array is clocked by a control flip-flop, which stores a marker bit. A "1" signifies that the position's data is filled and a "0" denotes a vacancy in that position. The control flip-flop detects the state of the preceding flip-flop and communicates its own status to the succeeding flip-flop. When a control flip-flop is in the "0" state and sees a "1" in the preceding flip-flop, it generates a clock pulse, transferring data from the preceding four data latches into its own four data latches and resetting the preceding flip-flop to "0". The first and last control flip-flops have buffered outputs. Since all empty locations "bubble" automatically to the input end, and all valid data ripple through to the output end, the status of the first control flip-flop (DATA-IN READY) indicates if the FIFO is full, and the status of the last flip-flop (DATA-OUT READY) indicates if the FIFO contains data. As the earliest data are removed from the bottom of the data stack (the output end), all data entered later will automatically propagate (ripple) toward the output.

Loading Data – Data can be entered whenever the DATA-IN READY (DIR) flag is high, by a high level on the SHIFT-IN (SI) input. This input must go low momentarily before the next nibble (4-bits) of data is accepted by the FIFO. The DIR flag will go low momentarily, until the data have been transferred to the second location. The flag will remain low when all 16-word locations are filled with valid data, and further pulses on the SI input will be ignored until DIR goes high.

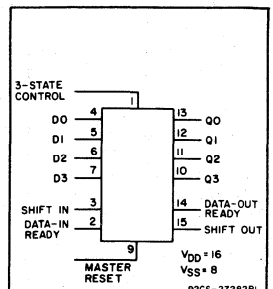
Unloading Data – As soon as the first data have rippled to the output, DATA-OUT READY (DOR) goes high, and data can be removed by a falling edge on the SO input. This falling edge causes the DOR signal to go low while the word on the output is dumped and the next word moves to the output. As long as valid data are available in the FIFO, the DOR signal will go high again signifying that the next nibble of data is ready at the output. When the FIFO is empty, DOR will remain low, and any further commands will be ignored until a "1" marker ripples down to the last control register, when DOR goes high. Unloading of data is inhibited while the 3-state control input is high. The 3-state control signal should not be shifted from high to low (data outputs turned on) while the SHIFT-OUT is at logic 0. This level change would cause the first nibble to be shifted out (unloaded) immediately and the data to be lost.

Features:

- **Independent asynchronous inputs and outputs**
- **3-state outputs** ■ **Expandable in either direction**
- **Status indicators on input and output** ■ **Reset capability**
- **Standardized, symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

- **Bit rate smoothing**
- **CPU/terminal buffering**
- **Data communications**
- **Peripheral buffering**
- **Line printer input buffers**
- **Auto dialers**
- **CRT buffer memories**



FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . –0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = –40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
PACKAGE TYPE E . . . . . –40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS ALL TYPES		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

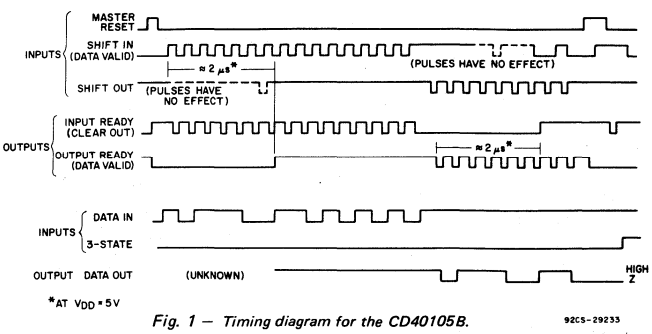


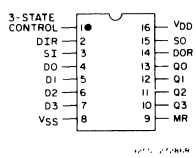
Fig. 1 – Timing diagram for the CD40105B. 92CS-29233

Cascading – The CD40105B can be cascaded to form longer registers simply by connecting the DIR to SO and DOR to SI. For words wider than 4 bits, the DIR and the DOR outputs must be gated together with AND gates. Their outputs drive the SI and SO inputs in parallel, if expanding is done in both directions (See Figs. 3 and 4).

3-State Outputs – In order to facilitate data busing, 3-state outputs are provided on the data output lines, while the load condition of the register can be detected by the state of the DOR output.

Master Reset – A high on the MASTER RESET (MR) sets all the control logic marker bits to "0". DOR goes low and DIR goes high. The contents of the data register are not changed, only declared invalid, and will be superseded when the first nibble of data is loaded.

The CD40105B types are supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).



TERMINAL ASSIGNMENT

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
									+25		
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5, 13.5	–	15	4				–	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5, 13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA
3-State Output Leakage Current I_{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	–	$\pm 10^{-4}$	±0.4	μA

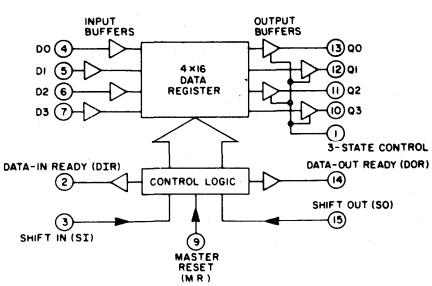


Fig. 2 – CD40105B functional block diagram.

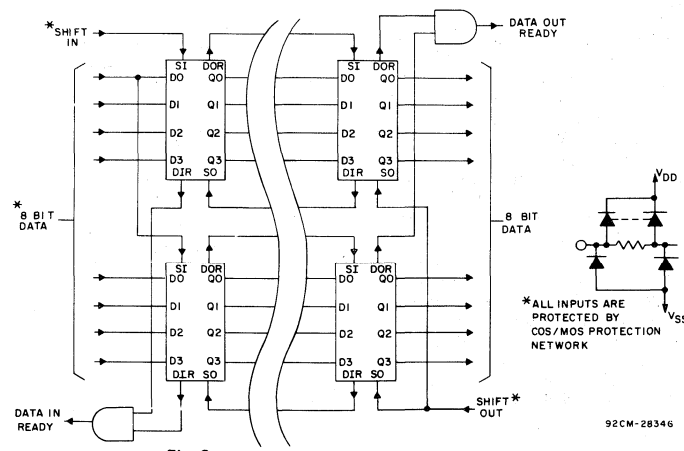


Fig. 3 – Expansion, 8-bits-wide-by-16 N-bits long.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C;
Input t_r,t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC		TEST CONDITIONS V_{DD} (V)	ALL TYPES TYPICAL VALUES	UNITS
Propagation Delay Time: Reset to Output Ready	t_{PHL}	5	90	ns
		10	45	
		15	35	
Shift-In to Input Ready	t_{PHL}	5	240	ns
		10	120	
		15	90	
Shift-Out to Output Ready	t_{PHL}	5	120	ns
		10	60	
		15	45	
3-State Control to Data Out (Turn-on)	t_{PZH}, t_{PZL}	5	100	ns
		10	50	
		15	40	
Transition Time	t_{TLH}, t_{THL}	5	100	ns
		10	50	
		15	40	
Ripple-Through Delay, Input to Output		5	2	μs
		10	1	
		15	0.7	
Maximum Shift-In or Shift-Out Rate		5	3	MHz
		10	6	
		15	8	
Minimum Data Setup Time	t_S	5	35	ns
		10	20	
		15	15	
Minimum Shift-Out or Shift-In Pulse Width		5	100	ns
		10	40	
		15	30	
Maximum Shift-Out or Shift-In Rise or Fall Time		5	15	μs
		10	5	
		15	5	
Minimum Master Reset Pulse Width	t_W	5	80	ns
		10	40	
		15	30	
Input Capacitance	C_{IN}	Any Input	5	pF

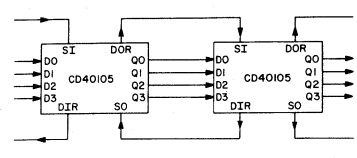


Fig. 4 – Expansion, 4-bits-wide-by-16 N-bits long.

COS/MOS Hex Schmitt Triggers

High-Voltage Types (20-Volt Rating)

The RCA-CD40106B consists of six Schmitt-trigger circuits. Each circuit functions as an inverter with Schmitt-trigger action on the input. The trigger switches at different points for positive- and negative-going signals. The difference between the positive-going voltage (VP) and the negative-going voltage (V_N) is defined as hysteresis voltage (V_H) (see Fig.6).

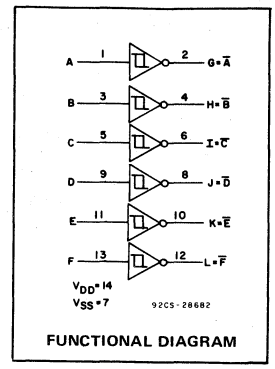
The CD40106B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Schmitt-trigger action with no external components**
- **Hysteresis voltage (typ.) 0.9 V at V_{DD} = 5 V, 2.3 V at V_{DD} = 10 V, and 3.5 V at V_{DD} = 15 V**
- **Noise immunity greater than 50%**
- **No limit on input rise and fall times**
- **Standardized, symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Low V_{DD} to V_{SS} current during slow input ramp**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No.13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

- **Wave and pulse shapers**
- **High-noise-environment systems**
- **Monostable multivibrators**
- **Astable multivibrators**



FUNCTIONAL DIAGRAM

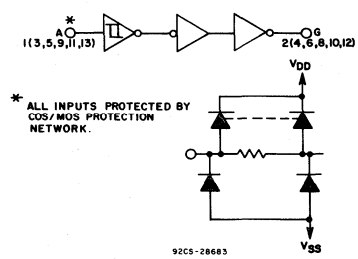


Fig.1 – Logic diagram (1 of 6 Schmitt triggers).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS		UNITS
		V_{DD} (V)	TYP.	MAX.	
Propagation Delay Time: t_{PHL}, t_{PLH}		5	140	280	ns
		10	70	140	
		15	60	120	
Transition Time: t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input		5	7.5	pF

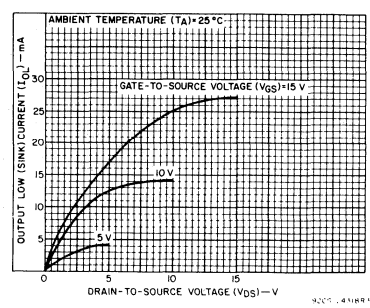


Fig.2 – Typical output low (sink) current characteristics.

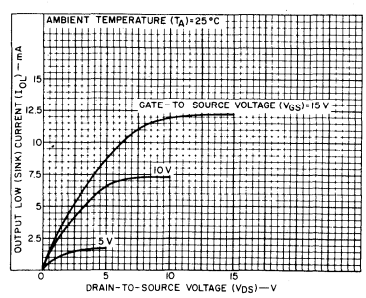


Fig.3 – Minimum output low (sink) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55,+25,+125 Apply to D,K,F,H Packages Values at −40,+25,+85 Apply to E Packages							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Positive Trigger Threshold Voltage V_P Min.	–	–	5	2.2	2.2	2.2	2.2	2.2	2.9	–	V
	–	–	10	4.6	4.6	4.6	4.6	4.6	5.9	–	
	–	–	15	6.8	6.8	6.8	6.8	6.8	8.8		
V_P Max.	–	–	5	3.6	3.6	3.6	3.6	–	2.9	3.6	
	–	–	10	7.1	7.1	7.1	7.1	–	5.9	7.1	
	–	–	15	10.8	10.8	10.8	10.8	–	8.8	10.8	
Negative Trigger Threshold Voltage V_N Min.	–	–	5	0.9	0.9	0.9	0.9	0.9	1.9	–	V
	–	–	10	2.5	2.5	2.5	2.5	2.5	3.9	–	
	–	–	15	4	4	4	4	4	5.8	–	
V_N Max.	–	–	5	2.8	2.8	2.8	2.8	–	1.9	2.8	
	–	–	10	5.2	5.2	5.2	2.8	–	3.9	5.2	
	–	–	15	7.4	7.4	7.4	7.4	–	5.8	7.4	
Hysteresis Voltage V_H Min.	–	–	5	0.3	0.3	0.3	0.3	0.3	0.9	–	V
	–	–	10	1.2	1.2	1.2	1.2	1.2	2.3	–	
	–	–	15	1.6	1.6	1.6	1.6	1.6	3.5	–	
V_H Max.	–	–	5	1.6	1.6	1.6	1.6	–	0.9	1.6	
	–	–	10	3.4	3.4	3.4	3.4	–	2.3	3.4	
	–	–	15	5	5	5	5	–	3.5	5	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0.5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage Low-Level, V_{OL} Max.	–	5	5	0.05				–	0	0.05	V
	–	10	10	0.05				–	0	0.05	
	–	15	15	0.05				–	0	0.05	
Output Voltage High Level, V_{OH} Min.	–	0	5	4.95				4.95	5	–	
	–	0	10	9.95				9.95	10	–	
	–	0	15	14.95				14.95	15	–	
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

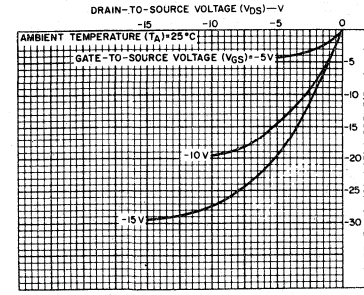


Fig.4 – Typical output high (source) current characteristics.

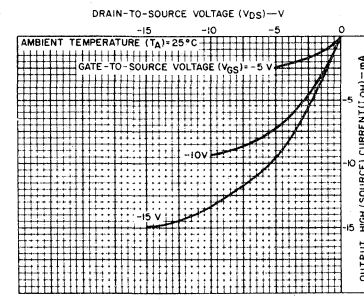


Fig.5 – Minimum output high (source) current characteristics.

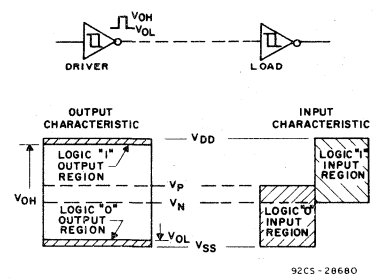
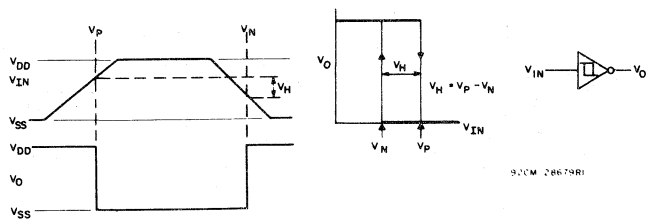


Fig.7 – Input and output characteristics.



a) Definition of V_P, V_N, V_H *b) Transfer characteristics of 1 of 6 gates*

Fig.6 – Hysteresis definition, characteristics, and test set-up.

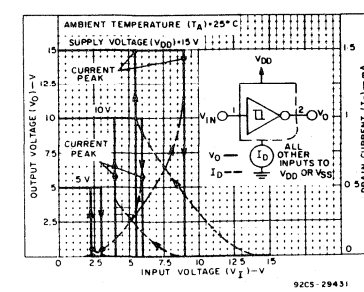


Fig.8 – Typical current and voltage transfer characteristics.

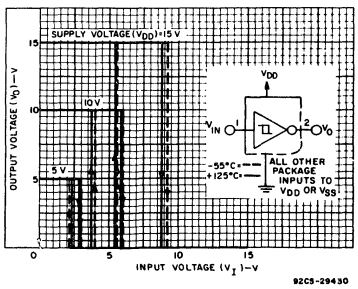


Fig.9 — Typical voltage transfer characteristics as a function of temperature.

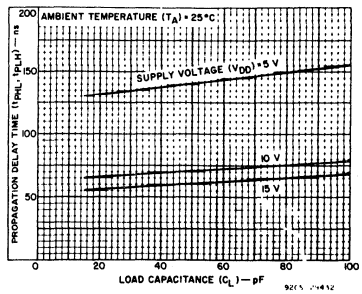


Fig.10 — Typical propagation delay time as a function of load capacitance.

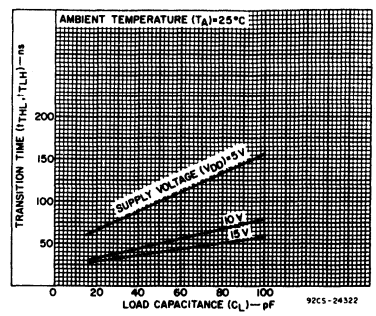


Fig.11 — Typical transition time as a function of load capacitance.

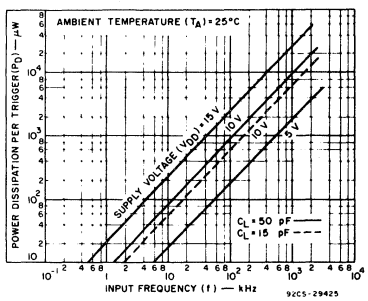


Fig.12 — Typical power dissipation per trigger as a function of input frequency.

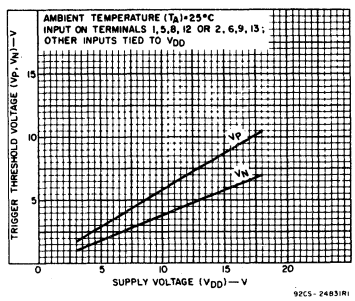


Fig.13 — Typical trigger threshold voltage as a function of supply voltage.

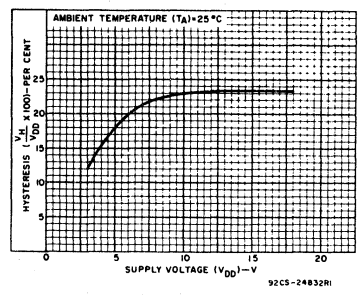


Fig.14 — Typical per cent hysteresis as a function of supply voltage.

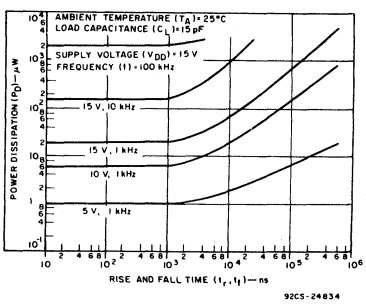


Fig.15 — Typical power dissipation as a function of rise and fall times.

APPLICATIONS

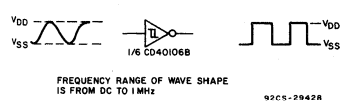


Fig.16 — Wave shaper.

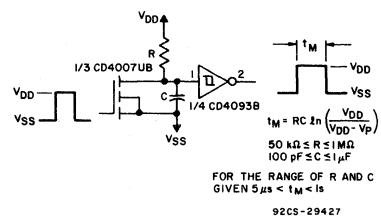


Fig.17 — Monostable multivibrator.

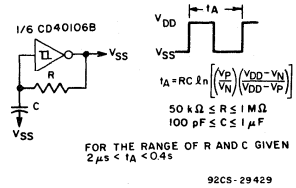


Fig.18 — Astable multivibrator.

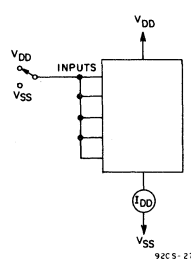


Fig.19 — Quiescent device current test circuit.

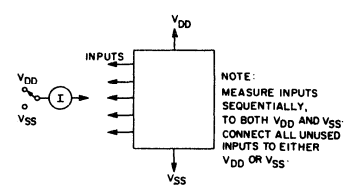


Fig.20 — Input current test circuit.

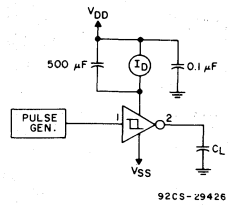
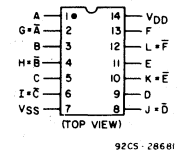
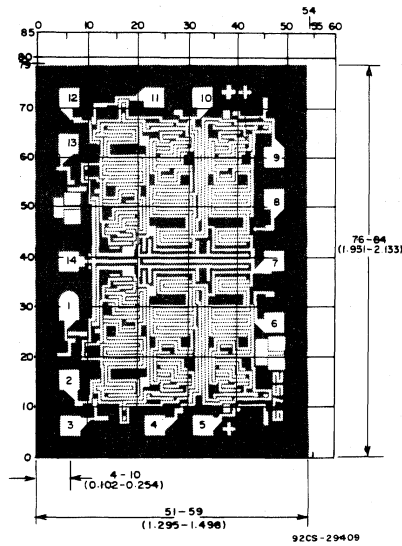


Fig.21 – Dynamic power dissipation test circuit.



TERMINAL ASSIGNMENT



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions and Pad Layout for CD40106BH

COS/MOS Dual 2-Input NAND Buffer/Driver

High-Voltage Type (20-Volt Rating)

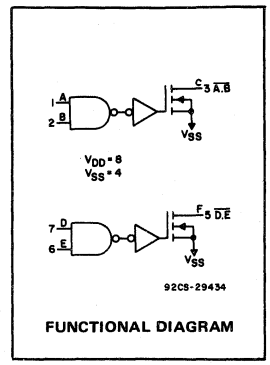
The RCA-CD40107B is a dual 2-input NAND buffer/driver containing two independent 2-input NAND buffers with open-drain single n-channel transistor outputs. This device features a wired-OR capability and high output sink current capability (136 mA typ. at V_{DD} = 10 V, V_{DS} = 1 V). The CD40107B is supplied in the 8-lead dual-in-line plastic (Mini-DIP) package (E suffix) and in chip form (H suffix).

Features:

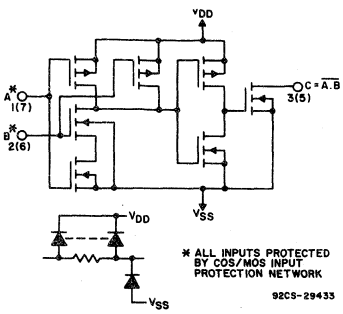
- **32 times standard B-Series output current drive sinking capability – 136 mA typ. @ V_{DD} = 10 V, V_{DS} = 1 V**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 mA at 18 V and 25°C**
- **5-V, 10-V, and 15-V parametric ratings**
- **Noise margin, full package temperature range, R_L to V_{DD} = 10 kΩ:**
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- **Meets all requirements of JEDEC Tentative Standard No.13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications

- **Driving relays, lamps, LEDs**
- **Line driver**
- **Level shifter (up or down)**



FUNCTIONAL DIAGRAM



TRUTH TABLE

A	B	C	
0	0	1*	Z#
1	0	1*	Z#
0	1	1*	Z#
1	1	0	

*Requires external pull-up resistor (R_L) to V_{DD}.

#Without pull-up resistor (3-state).

Fig. 1 – Schematic diagram of CD40107B (one of 2 gates)

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . –0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = –40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE H . . . . . –55 to +125°C
PACKAGE TYPE E . . . . . –40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

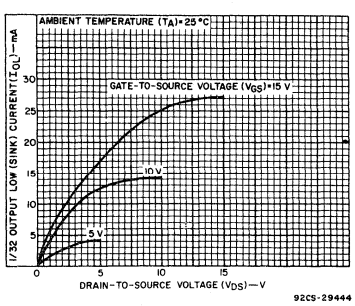


Fig.2 – Typical output low (sink) current characteristics.

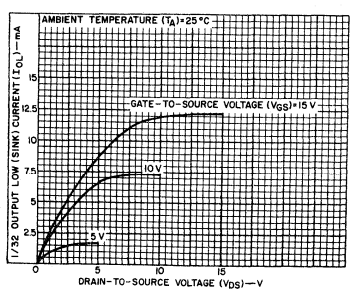


Fig.3 – Minimum output low (sink) current characteristics.

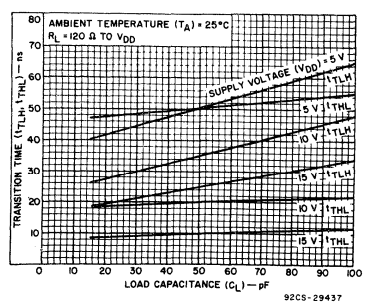


Fig.4 – Typical transition time as a function of load capacitance.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to H Package Values at −40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	21	20	14	12	16	32	–	mA
	1	0,5	5	44	42	30	25	34	68	–	
	0.5	0,10	10	49	46	32	28	37	74	–	
	1	0,10	10	89	85	60	51	68	136	–	
	0.5	0,15	15	66	63	44	38	50	100	–	
Output High (Source) Current I_{OH} Min.	No Internal Pull-Up Device										
Input Low Voltage V_{IL} Max.*	4.5	–	5	1.5				–	–	1.5	V
	9	–	10	3				–	–	3	
	13.5	–	15	4				–	–	4	
Input High Voltage V_{IH} Min.*	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA
Output Leakage Current I_{OZ} Max.	18	0,18	18	2	2	20	20	–	10^{-4}	2	μA

* Measured with external pull-up resistor, R_L = 10 kΩ to V_{DD}.

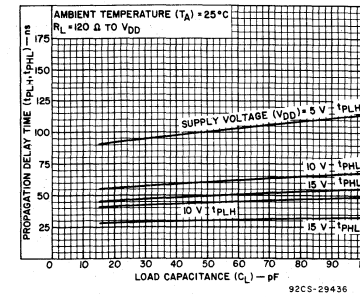


Fig.5 – Typical propagation delay time as a function of load capacitance.

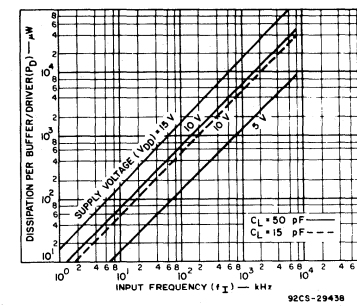


Fig.6 – Typical power dissipation as a function of input frequency.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 50 pF, Input t_r, t_f = 20 ns

CHARACTERISTIC	TEST CONDITIONS	V_{DD} Volts	LIMITS Typ.	LIMITS Max.	UNITS
Propagation Delay: High-to-Low, t_{PHL}	R_L* = 120 Ω	5	100	200	ns
		10	45	90	
		15	30	60	
Low-to-High, t_{PLH}	R_L* = 120 Ω	5	100	200	ns
		10	60	120	
		15	50	100	
Transition Time: High-to-Low, t_{THL}	R_L* = 120 Ω	5	50	100	ns
		10	20	40	
		15	10	20	
Low-to-High, t_{TLH}	R_L* = 120 Ω	5	50	100	ns
		10	35	70	
		15	25	50	
Average Input Capacitance, C_{IN}	Any Input		5	7.5	pF
Average Output Capacitance, C_{OUT}	Any Output		30	–	pF

* R_L is external pull-up resistor to V_{DD}.

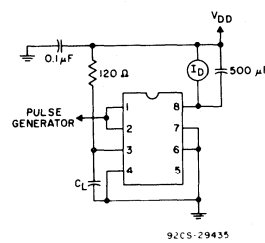


Fig.7 – Power-dissipation test circuit.

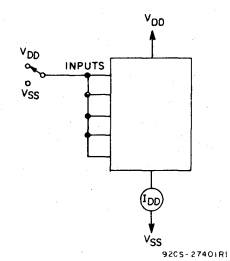


Fig.8 – Quiescent-device current test circuit.

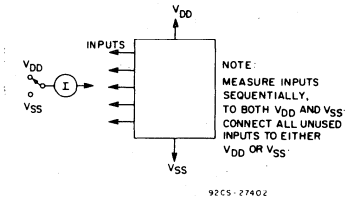


Fig.9 – Input leakage current test circuit.

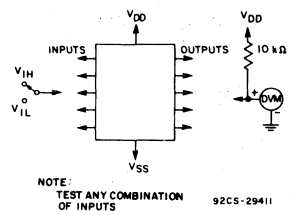
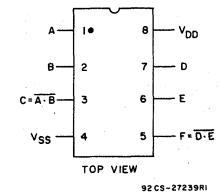
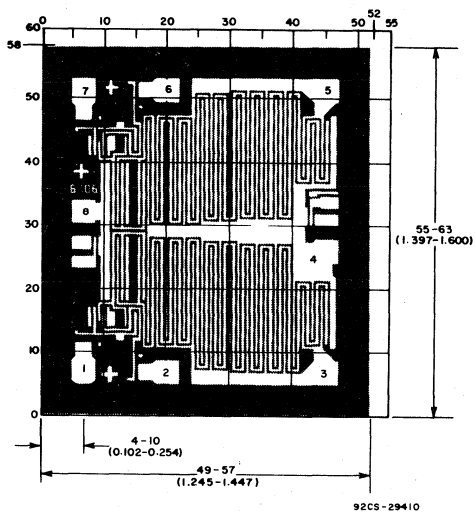


Fig.10 – Input-voltage test circuit.



TERMINAL ASSIGNMENT



Dimensions and Pad Layout for CD40107BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS 4 x 4 Multiport Register

High-Voltage Types (20-Volt Rating)

The RCA-CD40108B is a 4 x 4 multiport register containing four 4-bit registers, write address decoder, two separate read address decoders, and two 3-state output buses.

When the ENABLE input is low, the corresponding output bus is switched, independently of the clock, to a high-impedance state. The high-impedance third state provides the outputs with the capability of being connected to the bus lines in a bus-organized system without the need for interface or pull-up components.

When the WRITE ENABLE input is high, all data input lines are latched on the positive transition of the CLOCK and the data is entered into the word selected by the write address lines. When WRITE ENABLE is low, the CLOCK is inhibited and no new data is entered. In either case, the contents of any word may be accessed via the read address lines independent of the state of the CLOCK input.

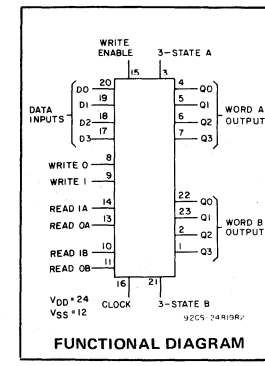
The CD40108B types are supplied in hermetic 24-lead dual-in-line ceramic packages (D suffix), 24-lead dual-in-line plastic packages (E and F suffixes), 24-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- Four 4-bit registers
- One input and two output buses
- Unlimited expansion in bit and word directions
- Data lines have latched inputs
- 3-state outputs
- Separate control of each bus, allowing simultaneous independent reading of any of four registers on Bus A and Bus B and independent writing into any of the four registers
- CD40108B is pin-compatible with industry type MC14580
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range):
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Scratch-pad memories
- Arithmetic units
- Data storage



FUNCTIONAL DIAGRAM

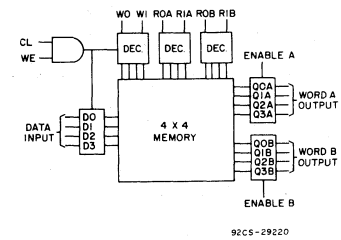


Fig. 1 – Block diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . –0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = –40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
PACKAGE TYPE E . . . . . –40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

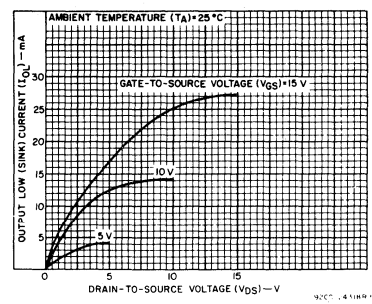


Fig. 2 – Typical output low (sink) current characteristics.

TRUTH TABLE

CLOCK	WRITE ENABLE	WRITE 1	WRITE 0	READ 1A	READ 0A	READ 1B	READ 0B	ENABLE A	ENABLE B	D_n	O_{nA}	O_{nB}
⎍⎍	1	S1	S2	S1	S2	S1	S2	1	1	1	1	1
⎍⎍	1	S1	S2	S1	S2	S1	S2	1	1	0	0	0
X	X	X	X	X	X	X	X	0	0	X	Z	Z
⎍⎍	1	0	0	0	1	1	0	1	1	D_n to word 0	Word 1 out	Word 2 out
⎍⎍	0	0	0	0	1	1	0	1	1	Word 0 not altered	Word 1 out	Word 2 out
X	X	X	X	1	0	0	1	1	1	X	Word 2 out	Word 1 out
⎍⎍	X	X	X	X	X	X	X	1	1	X	NC	NC

1 = HIGH LEVEL; 0 = LOW LEVEL; X = DON'T CARE; Z= HIGH IMPEDANCE
S1 and S2 refer to input states of either 1 or 0

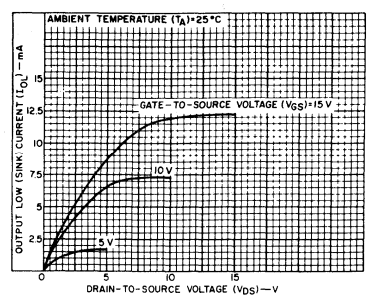


Fig. 3 – Minimum output low (sink) current characteristics.

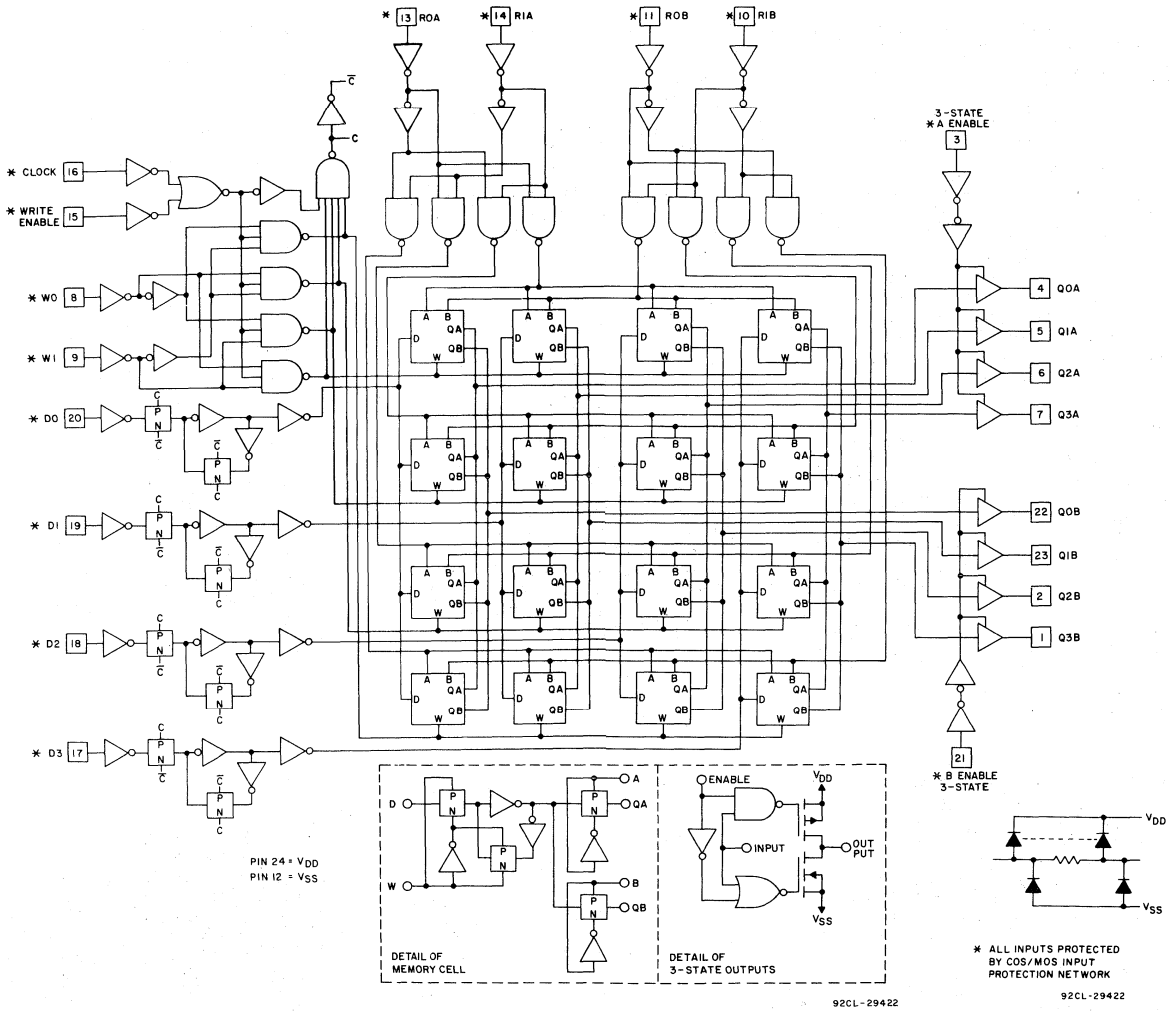


Fig. 4 – Logic diagram.

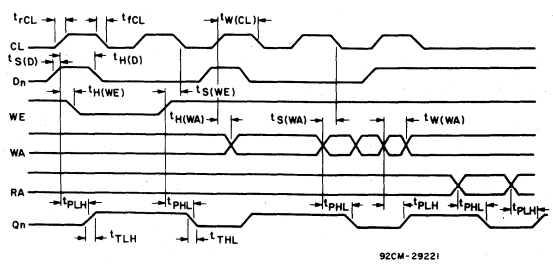


Fig. 5 – Timing diagram.

RECOMMENDED OPERATING CONDITIONS *at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:*

CHARACTERISTIC	V_{DD} (V)	LIMITS MIN.	LIMITS MAX.	UNITS
Supply Voltage Range (For T_A = Full Package Temperature Range)	–	3	18	V
Set-Up Time: Data to Clock, $t_{S(D)}$	5	0	–	ns
	10	0	–	
	15	0	–	
Write Enable to $\overline{Clock}$, $t_{S(WE)}$	5	250	–	ns
	10	100	–	
	15	70	–	
Write Address to $\overline{Clock}$, $t_{S(WA)}$	5	250	–	ns
	10	100	–	
	15	70	–	
Hold Time: Data to Clock, $t_{H(D)}$	5	220	–	ns
	10	100	–	
	15	80	–	
Write Enable to Clock, $t_{H(WE)}$	5	270	–	ns
	10	130	–	
	15	80	–	
Write Address to Clock, $t_{H(WA)}$	5	330	–	ns
	10	140	–	
	15	90	–	
Clock Input Frequency, f_{CL}	5	–	1.5	MHz
	10	–	3.5	
	15	–	4.5	
Clock Pulse Width, CL or WE t_W	5	350	–	ns
	10	130	–	
	15	90	–	
Clock Rise or Fall Time, t_rCL or t_fCL	5	–	15	μs
	10	–	5	
	15	–	5	

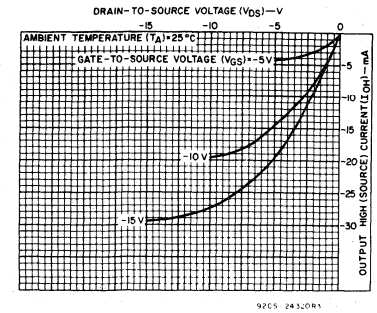


Fig. 6 – Typical output high (source) current characteristics.

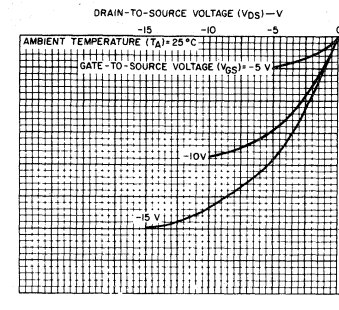


Fig. 7 – Minimum output high (source) current characteristics.

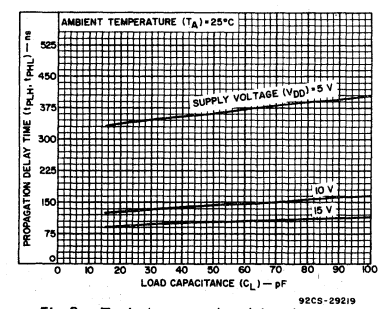


Fig. 8 – Typical propagation delay time as a function of load capacitance (CL or WE to Q).

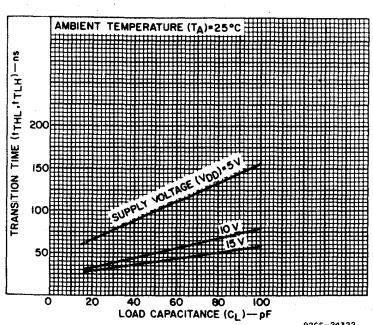


Fig. 9 – Typical transition time as a function of load capacitance.

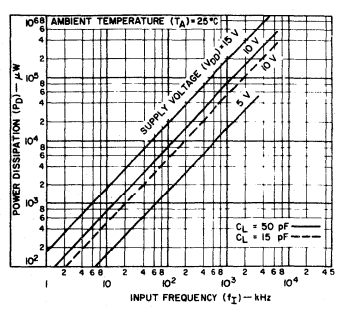


Fig. 10 – Typical power dissipation as a function of input frequency.

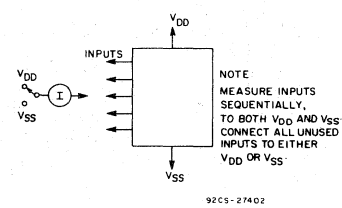
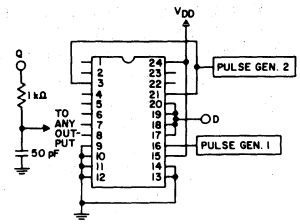
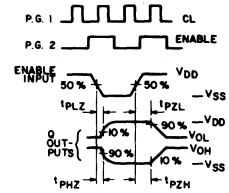


Fig. 11 – Input leakage current test circuit.

STATIC ELECTRICAL CHARACTERISTICS

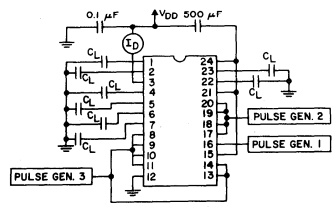
CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5, 13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA
3-State Output Leakage Current I_{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	–	$\pm 10^{-4}$	±0.4	μA





CHAR	TEST VOLTAGE	
	at D	at Q
t_{PHZ}	V_{DD}	V_{SS}
t_{PZH}	V_{DD}	V_{SS}
t_{PLZ}	V_{SS}	V_{DD}
t_{PZL}	V_{SS}	V_{DD}

Fig. 12 — Output-enable-delay-times test circuit and waveforms.



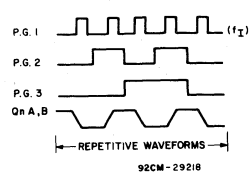
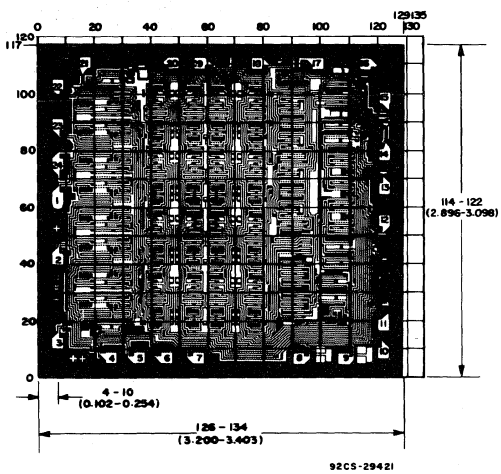


Fig. 13 — Power-dissipation test circuit and waveforms.



Dimensions and Pad Layout for CD40108BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r,t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Propagation Delay Time: t_{PHL}, t_{PLH} Clock or Write Enable to Q	5	–	360	720	ns
	10	–	140	280	
	15	–	100	200	
Read or Write Address to Q	5	–	300	600	ns
	10	–	120	240	
	15	–	85	170	
3-State Disable Delay Time: t_{PZH}, t_{PHZ}	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
t_{PZL}, t_{PLZ}	5	–	130	260	ns
	10	–	60	120	
	15	–	50	100	
Output Transition Time: t_{THL}, t_{TLH}	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Minimum Setup Time: Data to Clock $t_{S(D)}$	5	–	−95	0	ns
	10	–	−35	0	
	15	–	−20	0	
Write Enable to $\overline{Clock}$ $t_{S(WE)}$	5	–	125	250	ns
	10	–	50	100	
	15	–	35	70	
Write Address to $\overline{Clock}$ $t_{S(WA)}$	5	–	125	250	ns
	10	–	50	100	
	15	–	35	70	
Clock Rise and Fall Time: t_rCL, t_fCL	5	–	–	15	μs
	10	–	–	5	
	15	–	–	5	
Minimum Hold Time: Data to Clock $t_{H(D)}$	5	–	110	220	ns
	10	–	50	100	
	15	–	40	80	
Write Enable to Clock $t_{H(WE)}$	5	–	135	270	ns
	10	–	65	130	
	15	–	40	80	
Write Address to $\overline{Clock}$ $t_{S(WA)}$	5	–	165	330	ns
	10	–	70	140	
	15	–	45	90	
Maximum Clock Input Frequency, f_{CL}	5	1.5	3	–	MHz
	10	3.5	7	–	
	15	4.5	9	–	
Minimum Clock Pulse Width, Clock or Write Enable $t_{W(CL)}$	5	–	175	350	ns
	10	–	65	130	
	15	–	45	90	
Write Address $t_{W(WA)}$	5	–	150	300	ns
	10	–	75	150	
	15	–	45	90	
Average Input Capacitance, (Any Input) C_I	–	–	5	7.5	pF

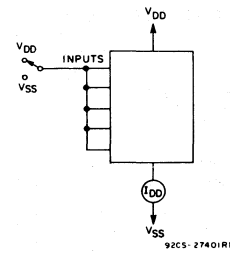


Fig. 14 – Quiescent-device-current test circuit.

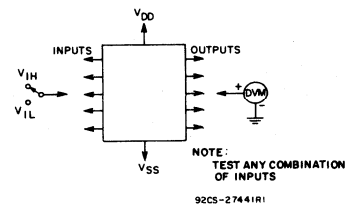
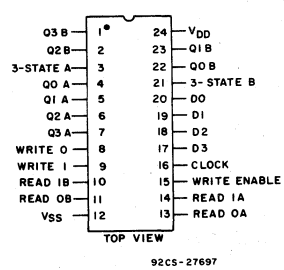


Fig. 15 – Input-voltage test circuit.



TERMINAL ASSIGNMENT

COS/MOS Quad Low-to-High Voltage Level Shifter

High-Voltage Types (20-Volt Rating)

The RCA-CD40109B contains four low-to-high-voltage level-shifting circuits. Each circuit will shift a low-voltage digital-logic input signal (A, B, C, D) with logical 1 = V_{CC} and logical 0 = V_{SS} to a higher-voltage output signal (E, F, G, H) with logical 1 = V_{DD} and logical 0 = V_{SS}.

The RCA-CD40109, unlike other low-to-high level-shifting circuits, does not require the presence of the high-voltage supply (V_{DD}) before the application of either the low-voltage supply (V_{CC}) or the input signals. There are no restrictions on the sequence of application of V_{DD}, V_{CC}, or the input signals. In addition, there are no restrictions on the relative magnitudes of the supply voltages or input signals within the device maximum ratings; V_{CC} may exceed V_{DD}, and input signals may exceed V_{CC} and V_{DD}. When operated in the mode $V_{CC} > V_{DD}$, the CD40109 will operate as a high-to-low level-shifter.

The CD40109 also features individual three-state output capability. A low level on any of the separately enabled three-state output controls produces a high-impedance state in the corresponding output.

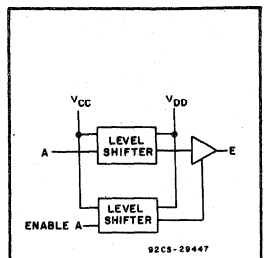
The CD40109B-Series types are supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Applications:

- **High-or-low level-shifting with three-state outputs for unidirectional or bidirectional bussing**
- **Isolation of logic subsystems using separate power supplies from supply sequencing, supply loss and supply regulation considerations**

Features:

- **Independence of power supply sequence considerations—V_{CC} can exceed V_{DD}, input signals can exceed both V_{CC} and V_{DD}**
- **Up and down level-shifting capability**
- **Three-state outputs with separate enable controls**
- **Standardized, symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (full package-temperature range)**
  = 1 V at V_{CC} = 5 V, V_{DD} = 10 V
  = 2 V at V_{CC} = 10 V, V_{DD} = 15 V
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**



FUNCTIONAL DIAGRAM
(1 of 4 units)

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC}, V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to +20 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K). . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

TRUTH TABLE

MODE	INPUTS		OUTPUTS
	A, B, C, D	ENABLE A, B, C, D	E, F, G, H
Low-to-high level shift	0	1	0
	1	1	1
	X	0	Z

LOGIC 0 = LOW(V_{SS}) X = DON'T CARE Z = HIGH IMPEDANCE
LOGIC 1 = V_{CC} at INPUTS and V_{DD} at OUTPUTS

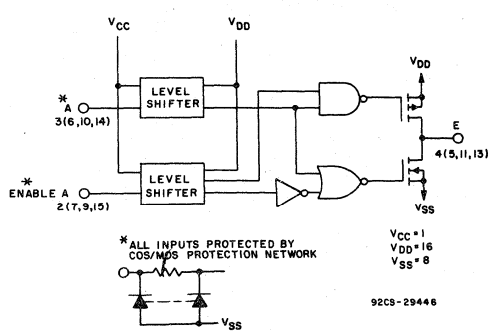


Fig. 1 — CD40109B logic diagram (1 of 4 units).

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	−	0,5	5	1	1	30	30	−	0.02	1	μA
	−	0,10	10	2	2	60	60	−	0.02	2	
	−	0,15	15	4	4	120	120	−	0.02	4	
	−	0,20	20	20	20	600	600	−	0.04	20	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	−	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	−	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	−	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	−	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	−	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	−	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	−	
Output Voltage: Low-Level, V_{OL} Max.	−	0,5	5	0.05				−	0	0.05	V
	−	0,10	10	0.05				−	0	0.05	
	−	0,15	15	0.05				−	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	−	0,5	5	4.95				4.95	5	−	
	−	0,10	10	9.95				9.95	10	−	
	−	0,15	15	14.95				14.95	15	−	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	−	$\pm 10^{-5}$	±0.1	μA
3-State Output Leakage Current I_{OUT} Max.		0,18	18	±0.4	±0.4	±12	±12	−	$\pm 10^{-4}$	±0.4	μA
	V_O (V)	V_{CC} (V)	V_{DD} (V)								
Input Low Voltage, V_{IL} Max.	1,9	5	10	1.5				—	—	1.5	V
	1.5, 13.5	10	15	3				—	—	3	
Input High Voltage, V_{IH} Min.	1,9	5	10	3.5				3.5	—	—	
	1.5,13.5	10	15	7				7	—	—	

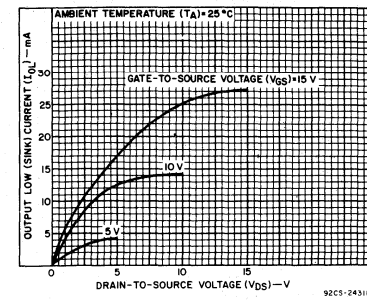


Fig.2 – Typical output low (sink) current characteristics.

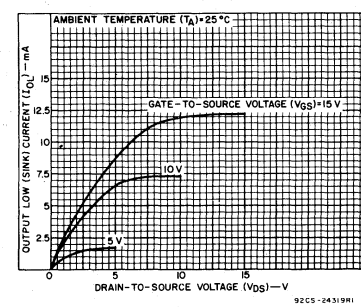


Fig.3 – Minimum output low (sink) current characteristics.

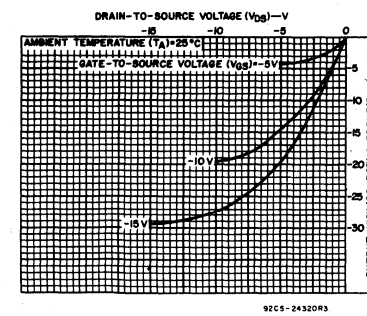


Fig.4 – Typical output high (source).

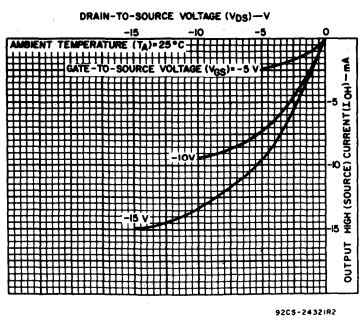


Fig.5 – Minimum output high (source) current characteristics.

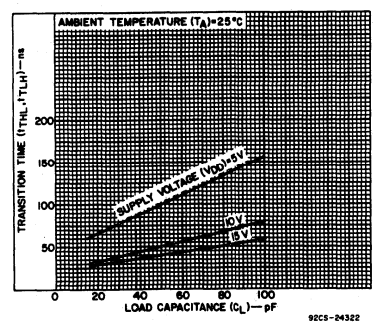


Fig.6 – Typical transition time as a function of load capacitance.

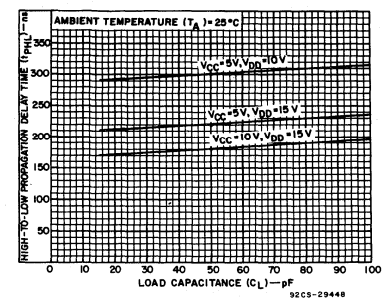


Fig.7 – Typical high-to-low propagation delay time as a function of load capacitance.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	SHIFTING MODE	V_{CC} (V)	V_{DD} (V)	LIMITS Typ.	LIMITS Max.	UNITS
Propagation Delay – Data Input to Output: High-to-Low Level, t_{PHL}	L–H	5	10	300	600	ns
		5	15	220	440	
		10	15	180	360	
	H–L	10	5	850	1600	
		15	5	850	1600	
		15	10	290	580	
Low-to-High Level, t_{PLH}	L–H	5	10	130	260	ns
		5	15	120	240	
		10	15	70	140	
	H–L	10	5	230	460	
		15	5	230	460	
		15	10	80	160	
3-State Disable Delay: Output High to High Impedance, t_{PHZ}	L–H	5	10	60	120	ns
		5	15	50	100	
		10	15	35	70	
	H–L	10	5	120	240	
		15	5	150	300	
		15	10	40	80	
Output Low to High Impedance, t_{PLZ}	L–H	5	10	370	740	ns
		5	15	300	600	
		10	15	250	500	
	H–L	10	5	850	1600	
		15	5	850	1600	
		15	10	350	700	
High Impedance to Output High, t_{PZH}	L–H	5	10	320	640	ns
		5	15	230	460	
		10	15	180	360	
	H–L	10	5	800	1500	
		15	5	800	1500	
		15	10	280	560	
High Impedance to Output Low, t_{PZL}	L–H	5	10	100	200	ns
		5	15	80	160	
		10	15	40	80	
	H–L	10	5	120	240	
		15	5	120	240	
		15	10	40	80	
Transition Time, t_{THL}, t_{TLH}	L–H	5	10	50	100	ns
		5	15	40	80	
		10	15	40	80	
	H–L	10	5	100	200	
		15	5	100	200	
		15	10	50	100	
Input Capacitance, C_I		Any Input		5	7.5	pF

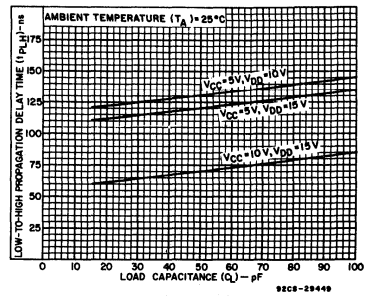


Fig.8 – Typical low-to-high propagation delay time as a function of load capacitance.

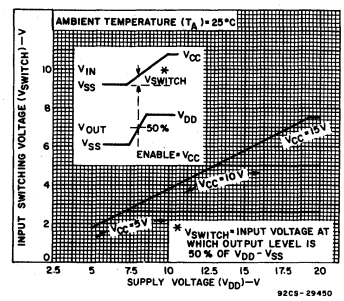


Fig.9 – Typical input switching as a function of high-level supply voltage.

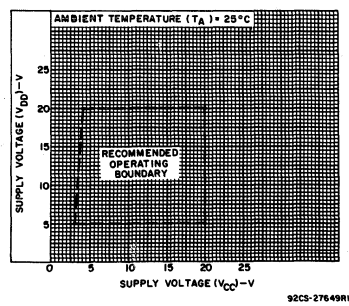


Fig.10 – High-level supply voltage vs. low-level supply voltage.

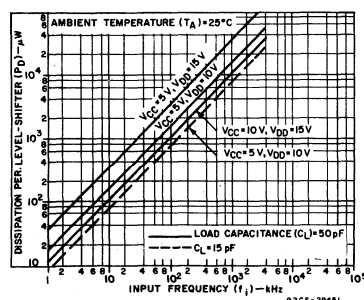


Fig.11 – Typical dynamic power dissipation as a function of input frequency.

TEST CIRCUITS

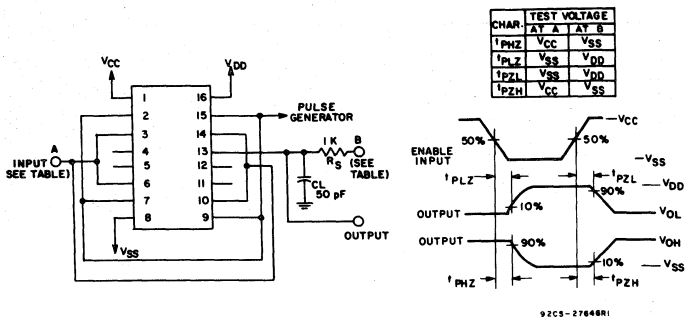


Fig. 12 — Output enable delay times test circuit and waveforms.

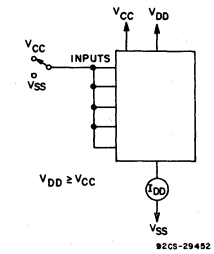


Fig. 13 — Quiescent device current.

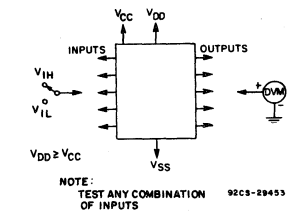


Fig. 14 — Input voltage.

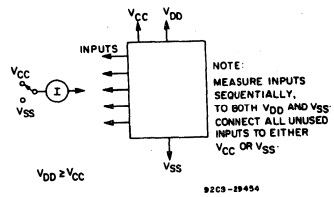


Fig. 15 — input current.

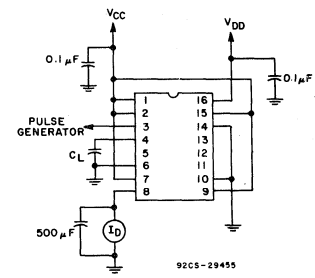
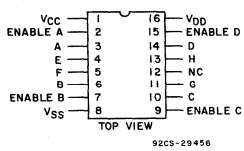


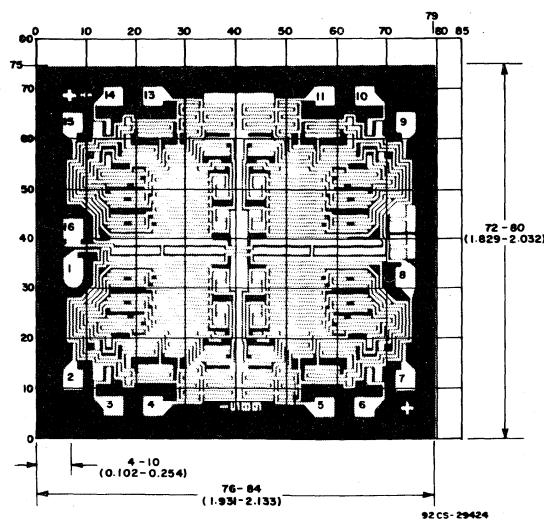
Fig. 16 — Dynamic power dissipation test circuit.



CD40109B
TERMINAL ASSIGNMENT

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.



Dimensions and pad layout for CD40109BH.

CD40110B

COS/MOS Decade Up-Down Counter/Decoder/ Latch/Driver

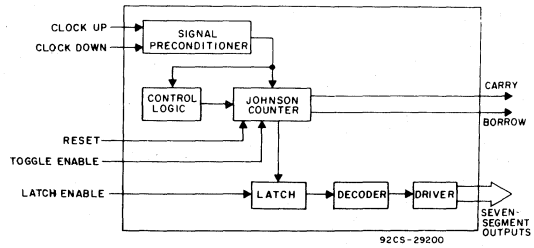
High-Voltage Type (20-V Rating)

The RCA-CD40110B is a dual-clocked up/down counter with a special preconditioning circuit that allows the counter to be clocked up or down regardless of the state or timing of the other clock line.

The signal is fed into the control logic and Johnson counter after it is preconditioned. The outputs of the Johnson counter (which include anti-lock gating to avoid being locked at an illegal state) are fed into a latch. This data can be fed directly to the decoder through the latch or can be strobed to hold a particular count while the Johnson counter continues to be clocked. The decoder feeds a seven-segment bipolar output driver which can source up to 25 mA to drive LEDs and other displays directly.

The CARRY and BORROW outputs can be tied directly to the clock-up and clock-down lines respectively of another CD40110B for easy cascading of several counters.

Objective Data



Functional Block Diagram

Features:

- **Separate clock-up and clock-down lines (allows clocking of one of these lines regardless of the state of the other line)**
- **Capable of driving LEDs and other displays directly**
- **Allows cascading without any external circuitry**

Applications:

- **Rate comparators**
- **General counting applications where display is desired**
- **Up/down counting applications where input pulses are random in nature**

COS/MOS 8-Bit Dual-Slope A/D Converter

High-Voltage Type (20-V Rating)

Objective Data

The RCA-CD40112B is a modified dual-slope analog-to-digital converter. The input voltage to be measured is converted to a current which causes an external capacitor to charge. The discharge time of the capacitor is compared with an internally generated reference time and the resulting time differential is displayed as a particular output count. The output count is latched and changes at the end of each complete conversion cycle.

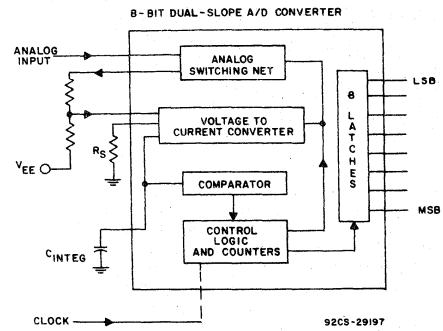
The CD40112B is designed for use in circuits requiring moderate-accuracy low-speed A/D conversion.

Features:

- **Single-supply operation — wide supply-voltage range**
- **Low power**
- **Economical 16-lead package**
- **Latched parallel binary outputs**
- **Requires only external clock and four low-cost passive components**

Applications:

- **General low-speed A/D applications where power and size are major considerations**
- **Data-acquisition systems requiring binary output data for microprocessors or minicomputers**



Functional Block Diagram

CD40113B

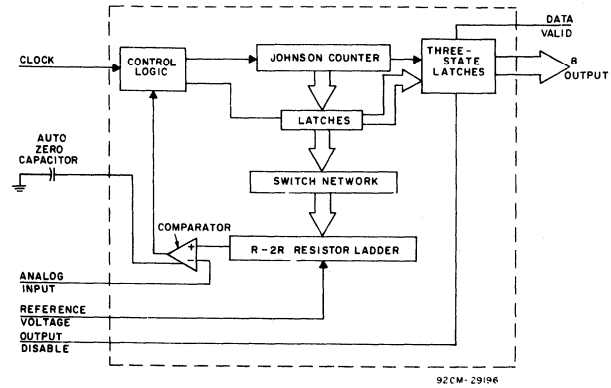
COS/MOS Successive Approximation 8-Bit A/D Converter

High-Voltage Type (20-V Rating)

The RCA-CD40113B successive approximation A/D converter compares an analog input to an internally generated signal until both match to 8-bit accuracy. The internal signal is then transferred to the output latches, at which time the data-valid signal goes low and remains there until the data transfer is completed. The data-valid signal is normally high.

A continuous clock results in continuous operation of the CD40113B. External gating of the clock, analog input, or data-valid signals can result in increased system design flexibility.

Objective Data



Functional Block Diagram

Features:

- **Single supply operation**
- **Low power**
- **16-lead package**
- **Needs only external clock, capacitor, and reference voltage for auto-zeroing**
- **3-state outputs for busing applications**
- **Parallel binary outputs**

Applications:

- **High-speed microprocessor system inputs**
- **Instrumentation and control**

COS/MOS 64-Bit Random Access Memory

High-Voltage Type (20-V Rating)

The RCA-CD40114B 16-word x 4-bit random access memory (RAM) comprises four address inputs, four DATA INPUTS, a WRITE ENABLE (WE) input, a MEMORY ENABLE (ME) input, and four 3-state DATA OUTPUTS. The ME input, and the 3-state data outputs allow memory expansion. The four address inputs are decoded internally to select one of the 16 possible word locations. The address information is latched on the negative edge of the ME input by an internal address register. The selected output assumes a high-impedance condition when the device is writing or disabled.

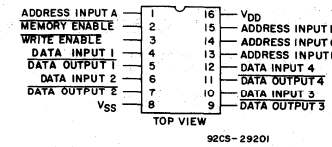
Objective Data

Features:

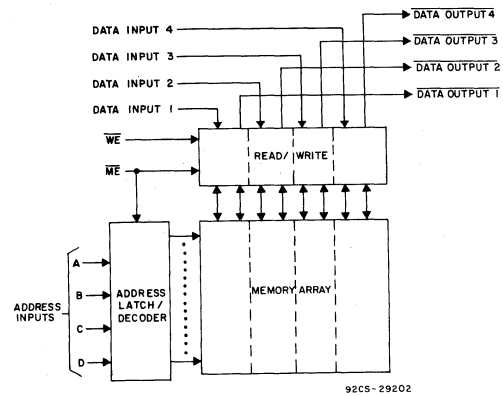
- **Input address latch**
- **3-state outputs**
- **Low-power TTL compatible**
- **High noise immunity**
- **Wide supply-voltage range**
- **Low power consumption**
- **Equivalent to and pin-compatible with National 74C89**
- **Pin-compatible with 74S189**

Applications:

- **Main frame memories**
- **Memory storage**



Terminal Assignment



Functional Block Diagram

$\overline{ME}$	$\overline{WE}$	MODE	OUTPUTS
H	X	CHIP INHIBIT	HIGH IMPEDANCE
L	H	READ	COMPLEMENT OF SELECTED WORD
L	L	WRITE	HIGH IMPEDANCE

Truth Table

10-Line to 4-Line BCD Priority Encoder

The RCA-CD40147B COS/MOS encoder features priority encoding of the inputs to ensure that only the highest-order data line is encoded. Ten data input lines are encoded to four-line (8, 4, 2, 1) BCD. All four output lines are logic 1 (V_{SS}) when all input lines are logic 0. All inputs and outputs are buffered, and each output can drive one TTL low-power Schottky load. The CD40147B is functionally similar to the TTL 54/74147.

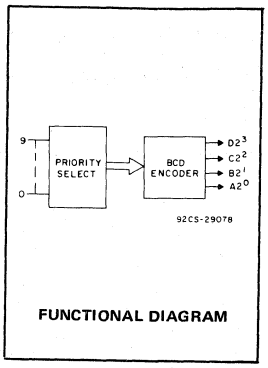
Objective Data

Features:

- **Encodes 10-line to 4-line BCD**
- **Active low inputs and outputs**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

- **Keyboard encoding**
- **10-line to BCD encoding**
- **Range selection**



FUNCTIONAL DIAGRAM

TRUTH TABLE (Negative Logic)

INPUTS										OUTPUTS			
0	1	2	3	4	5	6	7	8	9	D	C	B	A
0	0	0	0	0	0	0	0	0	0	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0	0	0	0
X	1	0	0	0	0	0	0	0	0	0	0	0	1
X	X	1	0	0	0	0	0	0	0	0	0	1	0
X	X	X	1	0	0	0	0	0	0	0	0	1	1
X	X	X	X	1	0	0	0	0	0	0	1	0	0
X	X	X	X	X	1	0	0	0	0	0	1	0	1
X	X	X	X	X	X	1	0	0	0	0	1	1	0
X	X	X	X	X	X	X	1	0	0	0	1	1	1
X	X	X	X	X	X	X	X	1	0	1	0	0	0
X	X	X	X	X	X	X	X	X	1	1	0	0	1

0 = High Level 1 = Low Level X = Don't Care

Preliminary Data

COS/MOS Synchronous Programmable 4-Bit Counters

High-Voltage Types (20-Volt Rating)

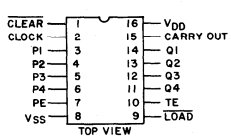
CD40160B – Decade with Asynchronous Clear
CD40161B – Binary with Asynchronous Clear
CD40162B – Decade with Synchronous Clear
CD40163B – Binary with Synchronous Clear

RCA-CD40160B, CD40161B, CD40162B, and CD40163B are 4-bit synchronous programmable counters. These devices are functionally equivalent to the TTL counter series 74160, 74161, 74162, and 74163, respectively. The CLEAR function of the CD40162B and CD40163B is synchronous and a low level at the $\overline{\text{CLEAR}}$ input sets all four outputs low on the next positive CLOCK edge. The CLEAR function of the CD40160B and CD40161B is asynchronous and a low level at the $\overline{\text{CLEAR}}$ input sets all four outputs low regardless of the state of the CLOCK, $\overline{\text{LOAD}}$, or ENABLE inputs. A low level at the $\overline{\text{LOAD}}$ input disables the counter and causes the output to agree with the setup data after the next CLOCK pulse regardless of the conditions of the ENABLE inputs.

Counting is enabled when both PE and TE inputs are high. The TE input is fed forward to enable C_{OUT}. This enabled output produces a positive output pulse with a duration approximately equal to the positive portion of the Q1 output. This pulse can be used to enable successive cascaded stages.

The CD40160B, CD40161B, CD40162B, and CD40163B types are supplied in 16-lead dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

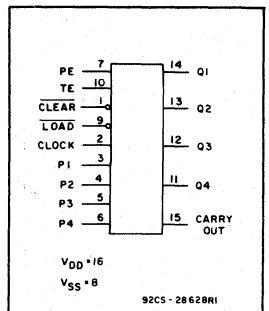
The CD40160B through CD40163B types are functionally equivalent to and pin-compatible with industry types MC14160B through MC14163B.



92CS-29459

Features:

- Internal look-ahead for fast counting
- Carry output for cascading
- Synchronously programmable
- Clear asynchronous input (CD40160B, CD40161B)
- Clear synchronous input (CD40162B, CD40163B)
- Load control input
- Low-power TTL compatibility
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"



FUNCTIONAL DIAGRAM

Applications:

- Programmable binary and decade counting
- Magnitude and sign generation
- Difference counting

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
									+25		
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	-	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

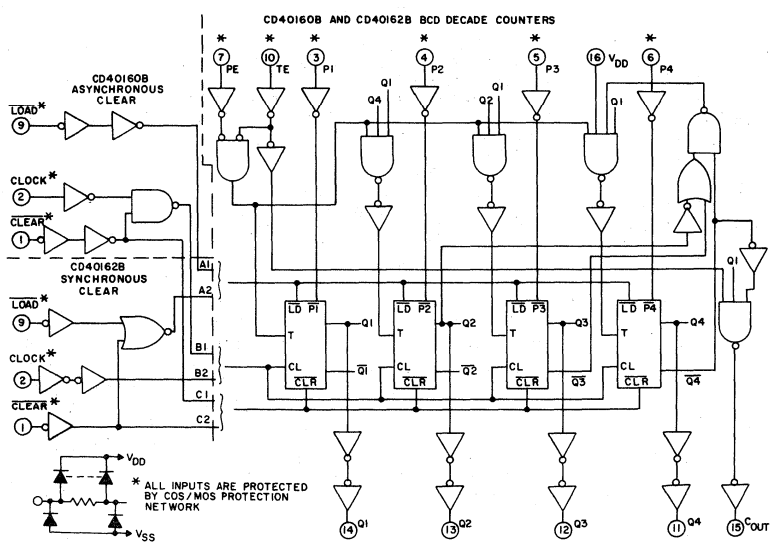


Fig. 1 – Logic diagrams for CD40160B and CD40162B BCD decade counters.

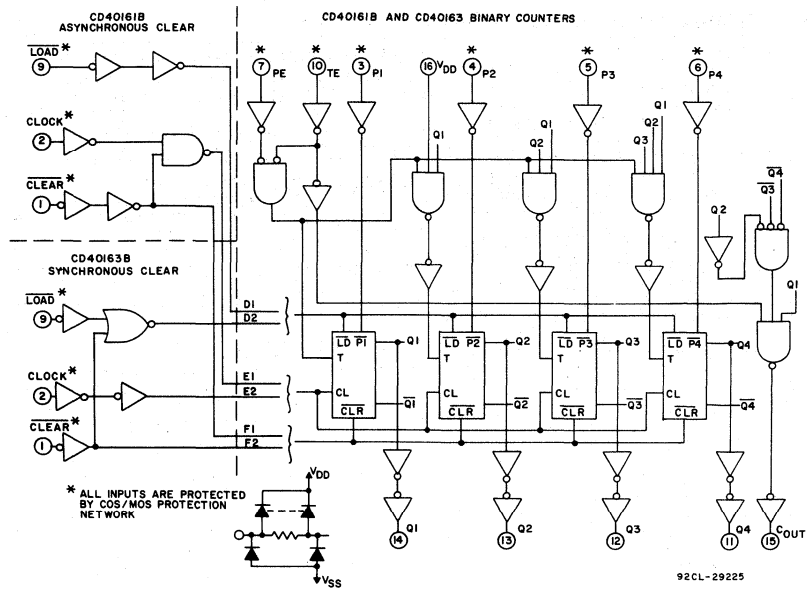


Fig. 2 – Logic diagrams for CD40161B and CD40163B binary counters.

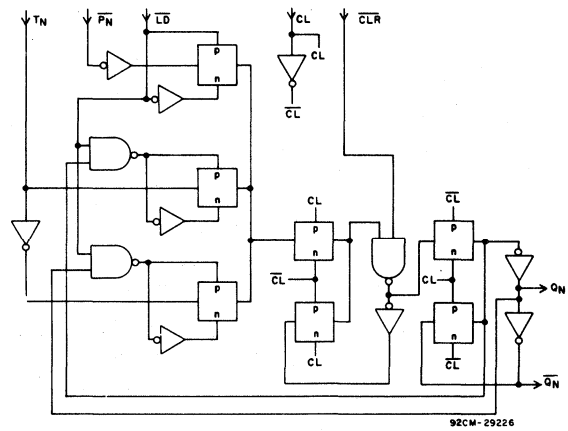


Fig. 3 – Detail of flip-flops of CD40160B and CD40161B (asynchronous clear).

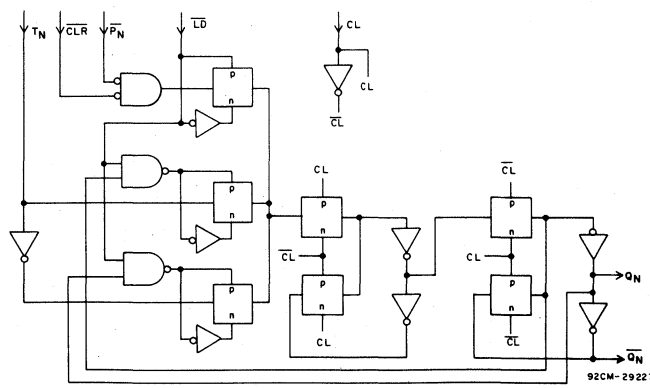


Fig. 4 – Detail of flip-flops for CD40162B and CD40163B (synchronous clear).

TRUTH TABLES (SYNCHRONOUS MODE)

CD40160B and CD40161B

CLOCK▲	$\overline{CLR}$	$\overline{LOAD}$	PE	TE	OPERATION
⎍	1	0	X	X	PRESET
⎍	1	1	0	X	NC
⎍	1	1	X	0	NC
⎍	1	1	1	1	COUNT
X	0	X	X	X	RESET

CD40162B and CD40163B

CLOCK▲	$\overline{CLR}$	$\overline{LOAD}$	PE	TE	OPERATION
⎍	1	0	X	X	PRESET
⎍	1	1	0	X	NC
⎍	1	1	X	0	NC
⎍	1	1	1	1	COUNT
⎍	0	X	X	X	RESET

1 = HIGH LEVEL 0 = LOW LEVEL X = DON'T CARE
▲ = LEVEL CHANGE NC = NO CHANGE

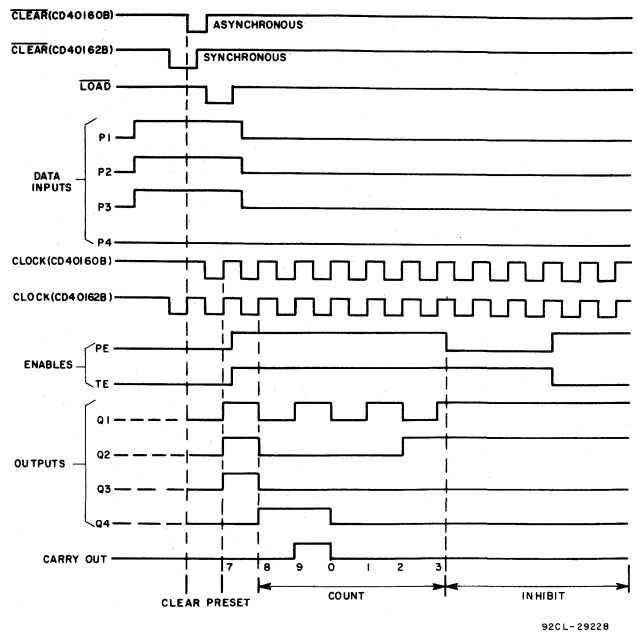


Fig. 5 – Timing diagram for CD40160B, CD40162B.

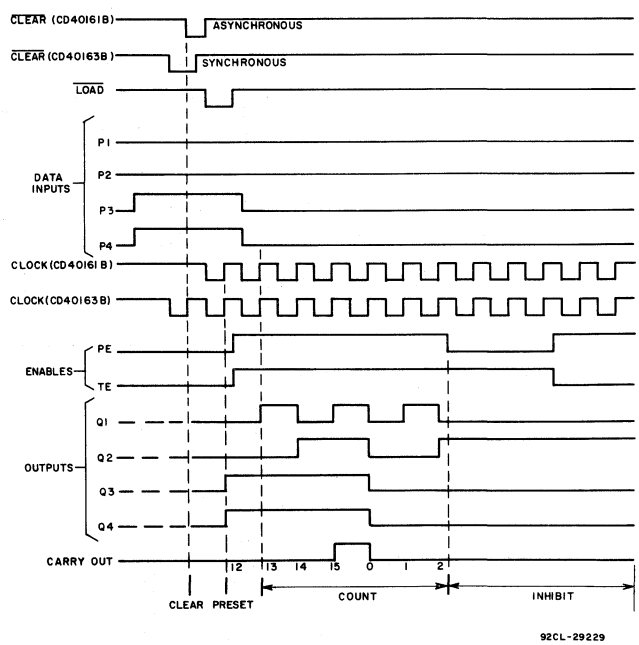


Fig. 6 – Timing diagram for CD40161B, CD40163B.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$;
Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC		TEST CONDITIONS V_{DD} (V)	TYPICAL VALUES	UNITS
CLOCK OPERATION				
Propagation Delay Time, Clock to Q	t_{PHL}, t_{PLH}	5 10 15	200 80 60	ns
Clock to C_{OUT}		5 10 15	290 120 75	ns
TE to C_{OUT}		5 10 15	180 70 50	ns
Minimum Setup Time, Data to Clock	t_{SU}	5 10 15	120 45 30	ns
$\overline{\text{Load}}$ to Clock		5 10 15	120 45 30	ns
PE or TE to Clock		5 10 15	170 70 50	ns
Transition Time,	t_{THL}, t_{TLH}	5 10 15	100 50 40	ns
Minimum Clock Pulse Width,	t_W	5 10 15	90 35 25	ns
Maximum Clock Frequency,	f_{CL}	5 10 15	3 8.5 12	MHz
Maximum Clock Rise or Fall Time,	t_{rCL}, t_{fCL}	5 10 15	200 70 20	μs
CLEAR OPERATION				
Propagation Delay Time, (CD40160B, CD40161B) Clear to Q	t_{PHL}, t_{PLH}	5 10 15	190 80 50	ns
Minimum Setup Time, (CD40162B, CD40163B) Clear to Clock	t_{SU}	5 10 15	120 50 30	ns

CD40174B Types

COS/MOS Hex 'D'-Type Flip-Flop

Preliminary Data

High-Voltage Types (20-Volt Rating)

The RCA-CD40174B consists of six identical 'D'-type flip-flops having independent DATA inputs. The CLOCK and CLEAR inputs are common to all six units. Data is transferred to the Q outputs on the positive-going transition of the clock pulse. All six flip-flops are simultaneously reset by a low level on the CLEAR input.

The CD40174B types are supplied in 16-lead dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

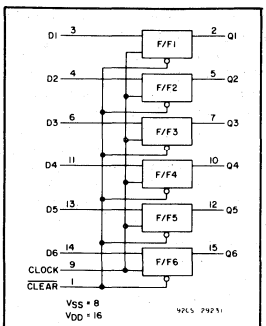
The CD40174B is similar to industry type 74174.

Features:

- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Shift Registers
- Buffer/Storage Registers
- Pattern Generators

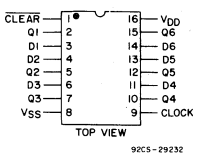


FUNCTIONAL DIAGRAM

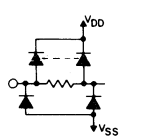
TRUTH TABLE FOR 1 OF 6 FLIP-FLOPS

INPUTS			OUTPUT
CLOCK	DATA	$\overline{\text{CLEAR}}$	Q
⌐‾	0	1	0
⌐‾	1	1	1
‾⌐	X	1	NC
X	X	0	0

1 = High Level X = Don't Care
0 = Low Level NC = No Change



TERMINAL ASSIGNMENT



ALL INPUTS (TERMS. 1, 3, 4, 6, 9, 11, 13, 14) PROTECTED BY COS/MOS INPUT PROTECTION NETWORK

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5, 13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5, 13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . –0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = –40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
PACKAGE TYPE E . . . . . –40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

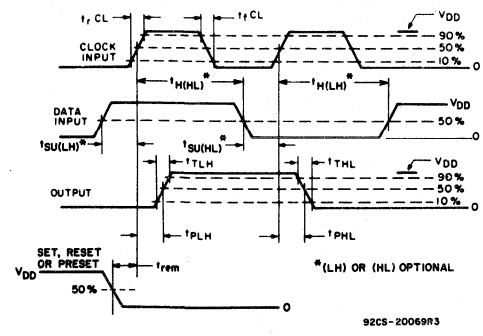


Fig. 1 – Definition of setup, hold, propagation delay, and removal times.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C;
Input t_r,t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	TYPICAL VALUES	UNITS
Propagation Delay Time, t_{PHL}, t_{PLH} Clock to Output	5	150	ns
	10	70	
	15	60	
Clear to Output	5	110	ns
	10	50	
	15	40	
Transition Time, t_{THL}, t_{TLH}	5	100	ns
	10	50	
	15	40	
Minimum Pulse Width, t_W Clock	5	50	ns
	10	35	
	15	30	
Clear	5	65	ns
	10	35	
	15	30	
Minimum Data Setup Time, t_{SU}	5	20	ns
	10	10	
	15	0	
Minimum Data Hold Time, t_H	5	30	ns
	10	15	
	15	5	
Maximum Clock Frequency, f_{CL}	5	7	MHz
	10	12	
	15	15.5	
Maximum Clock Rise or Fall Time, t_rCL, t_fCL	5	15	μs
	10	5	
	15	5	
Input Capacitance, C_{IN}	Any Input	5	pF

CD40181B Types

COS/MOS 4-Bit Arithmetic Logic Unit

High-Voltage Types (20-Volt Rating)

The RCA-CD40181B is a low-power four-bit parallel arithmetic logic unit (ALU) capable of providing 16 binary arithmetic operations on two four-bit words and 16 logical functions of two Boolean variables. The mode control input M selects logical (M = High) or arithmetic (M = Low) operation. The four select inputs (S0, S1, S2, and S3) select the desired logical or arithmetic functions, which include AND, OR, NAND, NOR, and exclusive–OR and–NOR in the logic mode, and addition, subtraction, decrement, left-shift and straight transfer in the arithmetic mode, according to the truth table. The CD40181B operation may be interpreted with either active-low or active-high data at the A and B word inputs and the function outputs F, by using the appropriate truth table.

The CD40181B contains logic for full look-ahead carry operation for fast carry generation using the carry-generate and carry-propagate outputs $\overline{G}$ and $\overline{P}$ for the four bits of the CD40181B. Use of the CD40182B look-ahead carry generator in conjunction with multiple CD40181B'S permits high-speed arithmetic operations on long words. A ripple carry output C_{n+4} is available for use in systems where speed is not of primary importance.

Also included in the CD40181B is a comparator output A = B, which assumes a high level whenever the two four-bit input words A and B are equal and the device is in the subtract mode. In addition, relative magnitude information may be derived from the carry-in input C_n and ripple carry-out output C_{n+4} by placing the unit in the subtract mode and externally decoding using the information in Table III.

The CD40181B types are supplied in hermetic ceramic 24-lead dual-in-line packages (D and F suffixes), 24-lead dual-in-line plastic packages (E suffix), 24-lead ceramic flat packages (K suffix), and in chip form (H suffix).

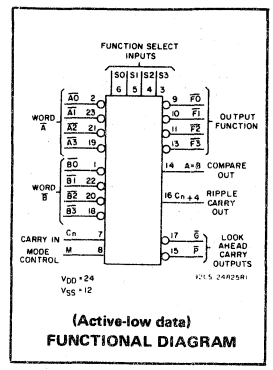
The CD40181B is similar to industry types MC14581 and 74181.

Features:

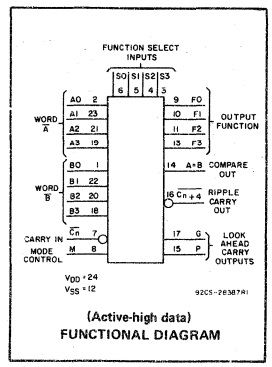
- Full look-ahead carry for speed operations on long words
- Generates 16 logic functions of two Boolean variables
- Generates 16 arithmetic functions of two 4-bit binary words
- A = B comparator output available
- Ripple-carry input and output available
- Typical addition time 200 ns @ V_{DD} = 10 V
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package temperature range)
  = 1 V at V_{DD} = 5 V
  = 2 V at V_{DD} = 10 V
  = 2.5 V at V_{DD} = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Parallel arithmetic units
- Process controllers
- Low-power minicomputers



(Active-low data)
FUNCTIONAL DIAGRAM



(Active-high data)
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, K)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)	3	18	V

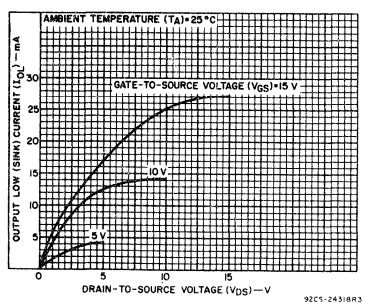


Fig. 1 — Typical output low (sink) current characteristics.

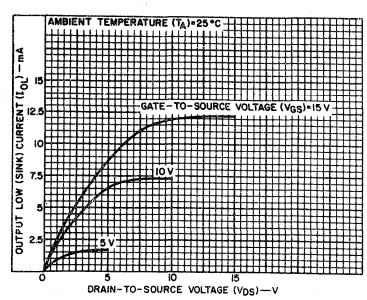


Fig. 2 — Minimum output low (sink) current characteristics.

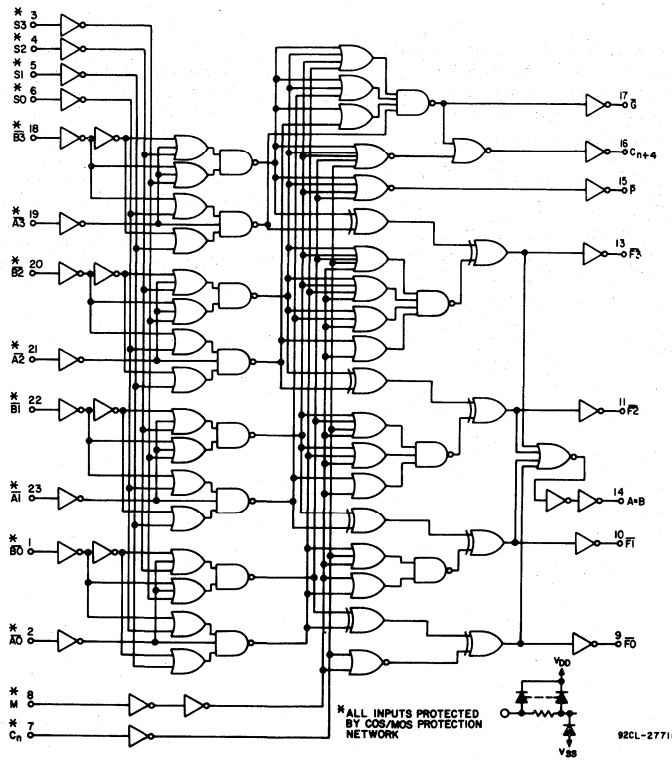


Fig. 3 – CD40181B logic diagram (active-low data).

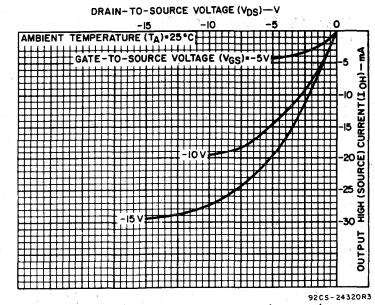


Fig. 4 – Typical output high (source) current characteristics.

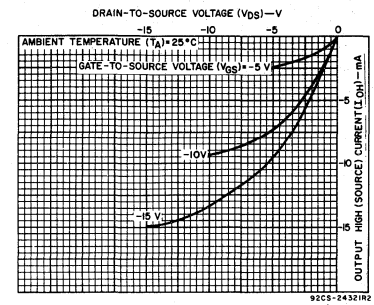


Fig. 5 – Minimum output high (source) current characteristics.

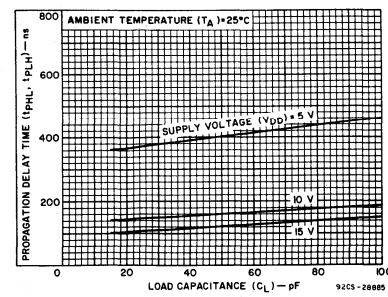


Fig. 6 – Typical propagation delay time as a function of load capacitance (for A or B to F, logic mode).

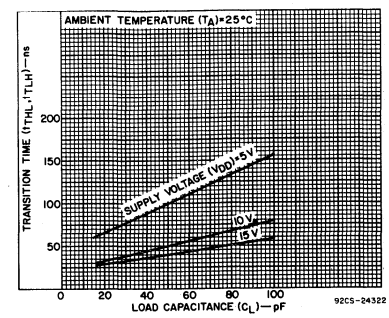


Fig. 7 – Typical transition time as a function of load capacitance.

TABLE I

TRUTH TABLE

FUNCTION SELECT				INPUTS/OUTPUTS ACTIVE LOW		INPUTS/OUTPUTS ACTIVE HIGH	
				LOGIC FUNCTION (M = H)	ARITHMETIC* FUNCTION (M = L, C_n = L)	LOGIC FUNCTION (M = H)	ARITHMETIC* FUNCTION (M = L, $\overline{C_n}$ = H)
S3	S2	S1	S0				
0	0	0	0	$\overline{A}$	A minus 1	$\overline{A}$	A
0	0	0	1	$\overline{AB}$	AB minus 1	$\overline{A+B}$	A + B
0	0	1	0	$\overline{A}+B$	$A\overline{B}$ minus 1	$\overline{A}B$	$A+\overline{B}$
0	0	1	1	Logic 1	minus 1	Logic 0	minus 1
0	1	0	0	$\overline{A}+\overline{B}$	A plus (A + $\overline{B}$)	$\overline{AB}$	A plus $A\overline{B}$
0	1	0	1	$\overline{B}$	AB plus (A + $\overline{B}$)	$\overline{B}$	(A + B) plus $A\overline{B}$
0	1	1	0	$A \oplus B$	A minus B minus 1	$A \oplus B$	A minus B minus 1
0	1	1	1	$A+\overline{B}$	$A+\overline{B}$	$A\overline{B}$	$A\overline{B}$ minus 1
1	0	0	0	$\overline{A}B$	A plus (A + B)	$\overline{A+B}$	A plus AB
1	0	0	1	$A \oplus B$	A plus B	$\overline{A \oplus B}$	A plus B
1	0	1	0	B	$A\overline{B}$ plus (A + B)	B	(A + $\overline{B}$) plus AB
1	0	1	1	A + B	A + B	AB	AB minus 1
1	1	0	0	Logic 0	A plus A	Logic 1	A plus A
1	1	0	1	$A\overline{B}$	AB plus A	A + $\overline{B}$	(A + B) plus A
1	1	1	0	AB	$A\overline{B}$ plus A	A + B	(A + $\overline{B}$) plus A
1	1	1	1	A	A	A	A minus 1

* Expressed as two's complement. For arithmetic function with C_n in the opposite state, the resulting function is as shown plus 1.

1 = HIGH LEVEL

0 = LOW LEVEL

CD40181B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	-	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		Typ.	Max.	
Propagation Delay Time: t_{PHL}, t_{PLH} A or B to F (logic mode), A or B to G or P,	5	400	800	ns
	10	160	320	
	15	120	240	
A or B to F, C_{n+4}, or A = B,	5	500	1000	ns
	10	200	400	
	15	140	280	
C_n to F	5	320	640	ns
	10	135	270	
	15	100	200	
C_n to C_{n+4}	5	200	400	ns
	10	100	200	
	15	70	140	
Transition Time: t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Input Capacitance, C_{IN} (Any Input)	–	5	7.5	pF

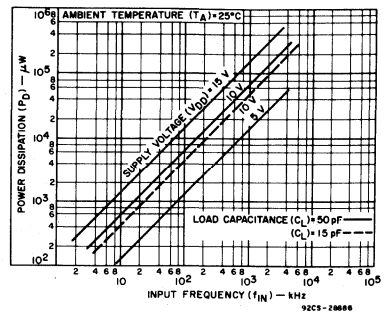


Fig. 8 – Typical dynamic dissipation as a function of input frequency (see Fig. 11 – dynamic power dissipation test circuit).

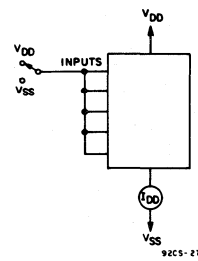


Fig. 9 – Quiescent-device-current test circuit.

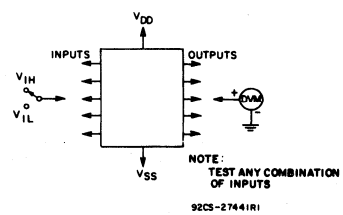


Fig. 10 – Input-voltage test circuit.

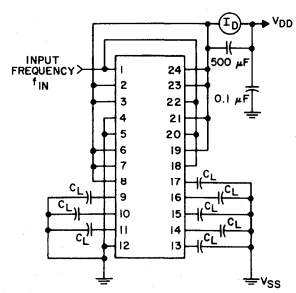


Fig. 11 – Dynamic power dissipation test circuit.

TABLE II

AC TEST SETUP REFERENCE (ACTIVE-LOW DATA)

TEST DELAY TIMES	AC PATHS		DC DATA INPUTS		MODE*
	INPUTS	OUTPUTS	TO V_{SS}	TO V_{DD}	
SUM_{IN} to SUM_{OUT}	$\overline{BO}$	Any $\overline{F}$	$\overline{B1}$, $\overline{B2}$, $\overline{B3}$, M, C_n	All $\overline{A}$'s	ADD
SUM_{IN} to $\overline{P}$	$\overline{AO}$	$\overline{P}$	$\overline{A1}$, $\overline{A2}$, $\overline{A3}$, M, C_n	All $\overline{B}$'s	ADD
SUM_{IN} to $\overline{G}$	$\overline{BO}$	$\overline{G}$	All $\overline{A}$'s M, C_n	$\overline{B1}$, $\overline{B2}$, $\overline{B3}$	ADD
SUM_{IN} to C_{n+4}	$\overline{BO}$	C_{n+4}	All $\overline{A}$'s, M, C_n	$\overline{B1}$, $\overline{B2}$, $\overline{B3}$	ADD
C_n to SUM_{OUT}	C_n	Any $\overline{F}$	All $\overline{A}$'s, M	All $\overline{B}$'s	ADD
C_n to C_{n+4}	C_n	C_{n+4}	All $\overline{A}$'s, M	All $\overline{B}$'s	ADD
SUM_{IN} to A = B	$\overline{BO}$	A = B	All A's, B1, B2, B3, M	C_n	SUBTRACT
SUM_{IN} to SUM_{OUT} (Logic Mode)	All $\overline{B}$'s	Any $\overline{F}$	All $\overline{A}$'s, C_n	M	EXCLUSIVE OR

* ADD Mode: SO, S3 = V_{DD}; S1, S2 = V_{SS}. SUBTRACT Mode: SO, S3 = V_{SS}; S1, S2 = V_{DD}.

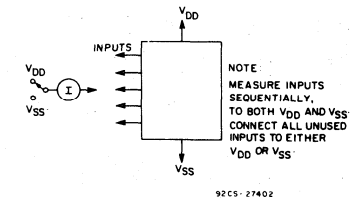
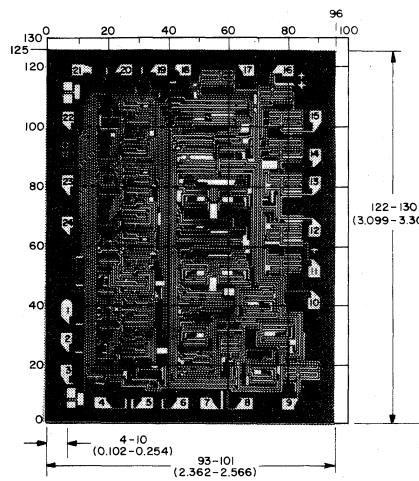


Fig. 12 – Input current test circuit.



Dimensions and pad layout for CD40181BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

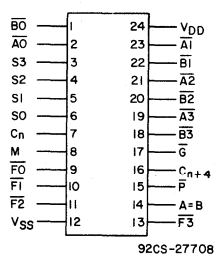
The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

TABLE III

MAGNITUDE COMPARISON

ACTIVE – HIGH DATA				ACTIVE – LOW DATA		
INPUT C_n	OUTPUT C_{n+4}	MAGNITUDE		INPUT C_n	OUTPUT C_{n+4}	MAGNITUDE
1	1	A ⩽ B		0	0	A ⩽ B
0	1	A < B		1	0	A < B
1	0	A > B		0	1	A > B
0	0	A ⩾ B		1	1	A ⩾ B

1 = HIGH LEVEL
0 = LOW LEVEL



Top View

Terminal Assignment (Active-low Data)

COS/MOS Look-Ahead Carry Generator

High-Voltage Types (20-Volt Rating)

The RCA-CD40182B is a high-speed look-ahead carry generator capable of anticipating a carry across four binary adders or groups of adders. The CD40182B is cascadable to perform full look-ahead across n-bit adders. Carry, propagate-carry, and generate-carry functions are provided as enumerated in the terminal designation below.

The CD40182B, when used in conjunction with the CD40181B arithmetic logic unit (ALU), provides full high-speed look-ahead carry capability for up to n-bit words. Each CD40182B generates the look-ahead (anticipated carry) across a group of four ALU's. In addition, other CD40182B's may be employed to anticipate the carry across sections of four look-ahead blocks up to n-bits. Carry inputs and outputs of the CD40181B are active-high logic, and carry-generate (G) and carry-propagate (P) outputs are active-low. Therefore the inputs and outputs of the CD40182B are compatible.

The CD40182B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

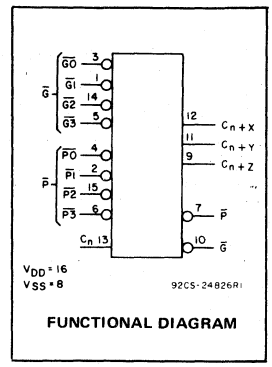
The CD40182B is similar to industry type MC14582.

Features:

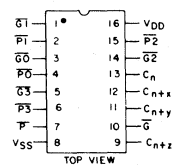
- Generates high-speed carry across four adders or adder groups
- High-speed operations: $t_{PHL} = t_{PLH}$ = 100 ns (typ.) @ V_{DD} = 10 V
- Cascadable for fast carries over N bits
- Designed for use with CD40181B ALU
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) = 1 V at V_{DD} = 5 V; 2 V at V_{DD} = 10 V; 2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

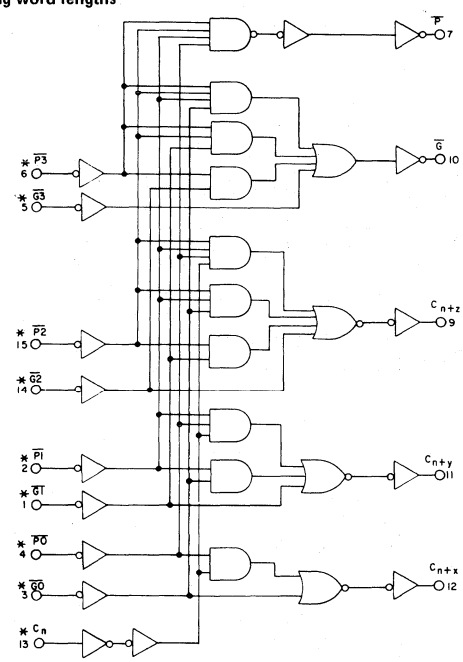
- High-speed parallel arithmetic units
- Multi-level look-ahead carry generation for long word lengths



FUNCTIONAL DIAGRAM



TERMINAL ASSIGNMENT



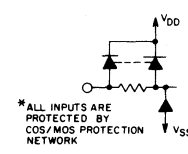


Fig. 1 – CD40182B logic diagram.

TERMINAL DESIGNATIONS

DESIGNATION	TERM.	FUNCTION
$\overline{G0}, \overline{G1}, \overline{G2}, \overline{G3}$	3, 1, 14, 5	Active-Low Carry-Generate Inputs
$\overline{P0}, \overline{P1}, \overline{P2}, \overline{P3}$	4, 2, 15, 6	Active-Low Carry-Propagate Inputs
C_n	13	Active-High Carry Input
$C_{n+x}, C_{n+y}, C_{n+z}$	12, 11, 9	Active-High Carry Outputs
$\overline{G}$	10	Active-Low Group Carry-Generate Output
$\overline{P}$	7	Active-Low Group Carry-Propagate Output

CD40182B Logic Equations:

$$C_{n+x} = G0 + P0 \cdot C_n$$

$$C_{n+y} = G1 + P1 \cdot G0 + P1 \cdot P0 \cdot C_n$$

$$C_{n+z} = G2 + P2 \cdot G1 + P2 \cdot P1 \cdot G0 + P2 \cdot P1 \cdot P0 \cdot C_n$$

$$\overline{G} = \overline{G3 + P3 \cdot G2 + P3 \cdot P2 \cdot G1 + P3 \cdot P2 \cdot P1 \cdot G0}$$

$$\overline{P} = \overline{P3 \cdot P2 \cdot P1 \cdot P0}$$

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . -0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . -55 to +125°C
PACKAGE TYPE E . . . . . -40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
									+25		
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	-	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

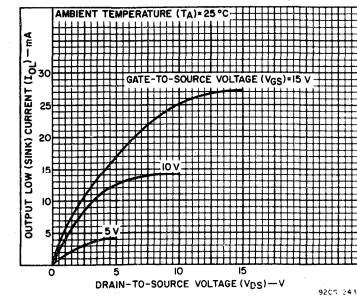


Fig. 2 – Typical output low (sink) current characteristics.

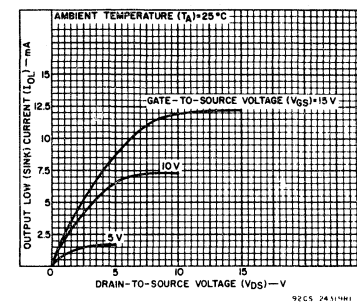


Fig. 3 – Minimum output low (sink) current characteristics.

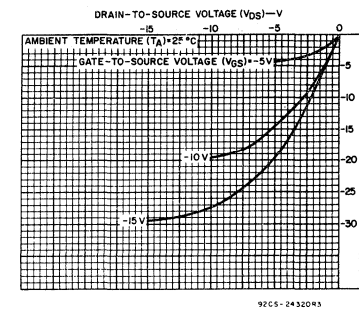


Fig. 4 – Typical output high (source) current characteristics.

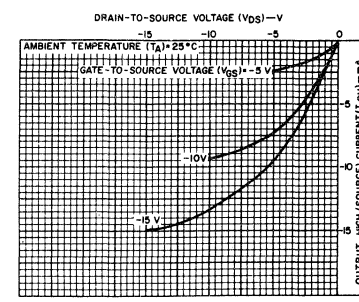


Fig. 5 – Minimum output high (source) current characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS Typ.	LIMITS Max.	UNITS
Propagation Delay Time: t_{PHL}, t_{PLH} P, G In to P, G Out and Carry Outs	5	200	400	ns
	10	100	200	
	15	75	150	
C_n to Carry Outs	5	240	480	ns
	10	120	240	
	15	90	180	
Transition Time: t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Input Capacitance C_{IN} (Any Input)	–	5	7.5	pF

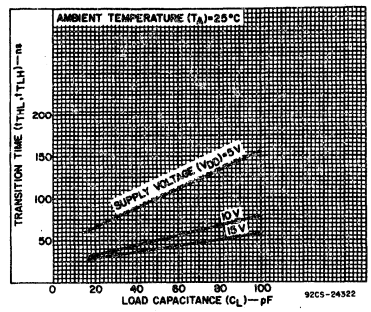


Fig. 6 – Typical transition time as a function of load capacitance.

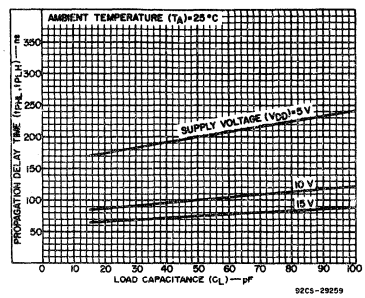


Fig. 7 – Typical propagation delay time as a function of load capacitance (P, G In to P, G Out and Carry-Outs).

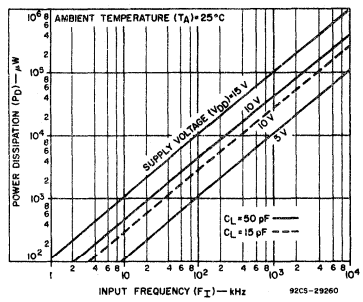


Fig. 8 – Typical power dissipation as a function of input frequency.

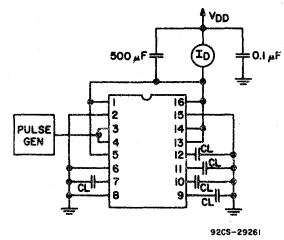


Fig. 9 – Power dissipation test circuit.

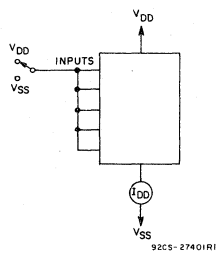


Fig. 10 – Quiescent device current test circuit.

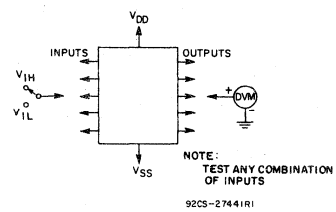


Fig. 11 – Input voltage test circuit.

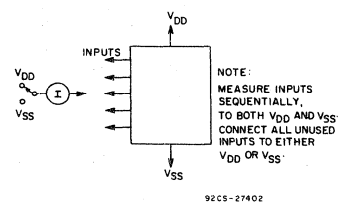


Fig. 12 – Input current test circuit.

Applications

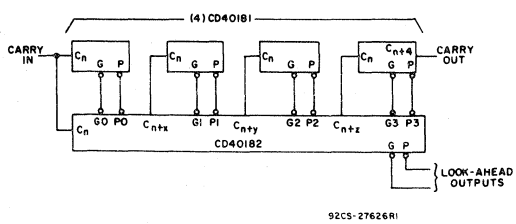


Fig. 13 – 16-Bit two-level look-ahead ALU.

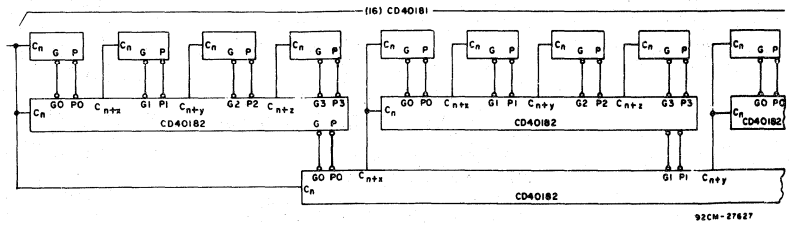


Fig. 14 – 64-Bit full carry look-ahead ALU in 3 levels.

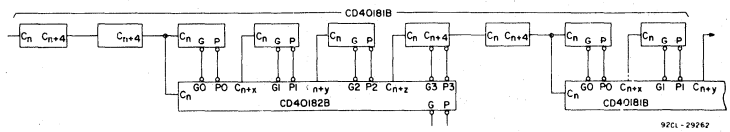
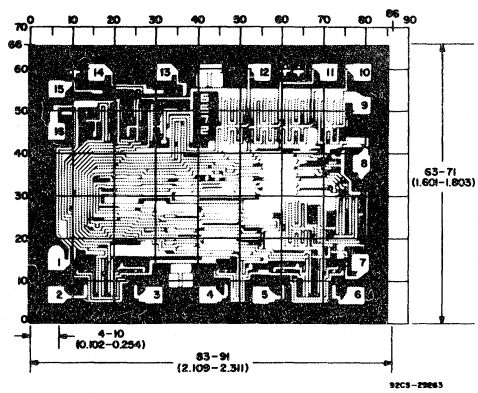


Fig. 15 – Combined two-level look-ahead and ripple-carry ALU.

DIMENSIONS AND PAD LAYOUT FOR CD40182BH



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS Presettable Up/Down Counters (Dual Clock With Reset)

High-Voltage Types (20-Volt Rating)
CD40192 – BCD Type
CD40193 – Binary Type

The RCA-CD40192B Presettable BCD Up/Down Counter and the CD40193B Presettable Binary Up/Down Counter each consist of 4 synchronously clocked, gated "D" type flip-flops connected as a counter. The inputs consist of 4 individual jam lines, a $\overline{\text{PRESET}}$ $\overline{\text{ENABLE}}$ control, individual CLOCK UP and CLOCK DOWN signals and a master RESET. Four buffered Q signal outputs as well as $\overline{\text{CARRY}}$ and $\overline{\text{BORROW}}$ outputs for multiple-stage counting schemes are provided.

The counter is cleared so that all outputs are in a low state by a high on the RESET line. A RESET is accomplished asynchronously with the clock. Each output is individually programmable asynchronously with the clock to the level on the corresponding jam input when the $\overline{\text{PRESET}}$ $\overline{\text{ENABLE}}$ control is low.

The counter counts up one count on the positive clock edge of the CLOCK UP signal provided the CLOCK DOWN line is high. The counter counts down one count on the positive clock edge of the CLOCK DOWN signal provided the CLOCK UP line is high.

The $\overline{\text{CARRY}}$ and $\overline{\text{BORROW}}$ signals are high when the counter is counting up or down. The $\overline{\text{CARRY}}$ signal goes low one-half clock cycle after the counter reaches its maximum count in the count-up mode. The $\overline{\text{BORROW}}$ signal goes low one-half clock cycle after the counter reaches its minimum count in the count-down mode. Cascading of multiple packages is easily accomplished without the need for additional external circuitry by tying the $\overline{\text{BORROW}}$ and $\overline{\text{CARRY}}$ outputs to the CLOCK DOWN and CLOCK UP inputs, respectively, of the succeeding counter package.

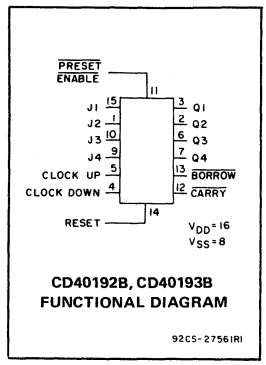
The CD40192B and CD40193B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- Individual clock lines for counting up or counting down
- Synchronous high-speed carry and borrow propagation delays for cascading
- Asynchronous reset and preset capability
- Medium-speed operation—f_{CL} = 8 MHz (typ.) @ 10 V
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin over full package temperature range:
  1 V at V_{DD} = 5 V 2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

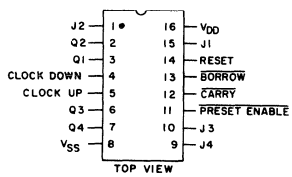
Applications:

- Up/down difference counting
- Multistage ripple counting
- Synchronous frequency dividers
- A/D and D/A conversion
- Programmable binary or BCD counting



CD40192B, CD40193B
FUNCTIONAL DIAGRAM

92CS-27561RI



92CS-27564R2

CD40192B, CD40193B
TERMINAL ASSIGNMENT

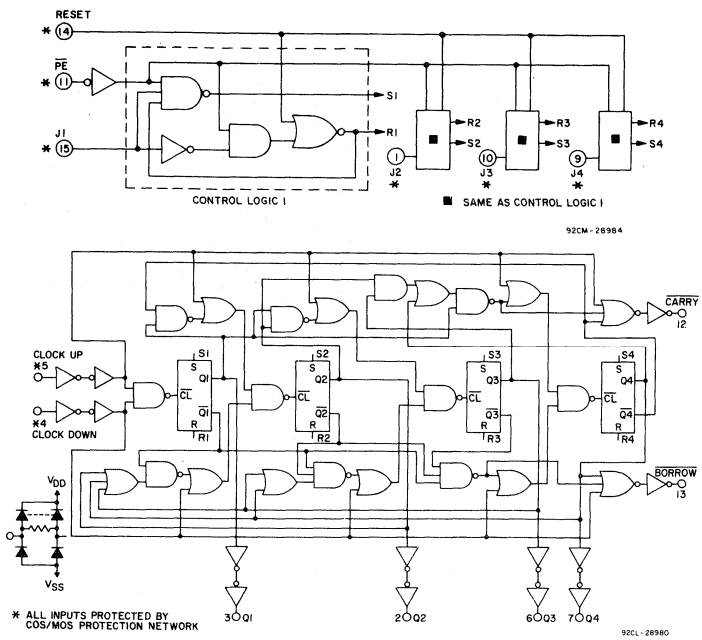


Fig. 1 – CD40192B logic diagram (BCD).

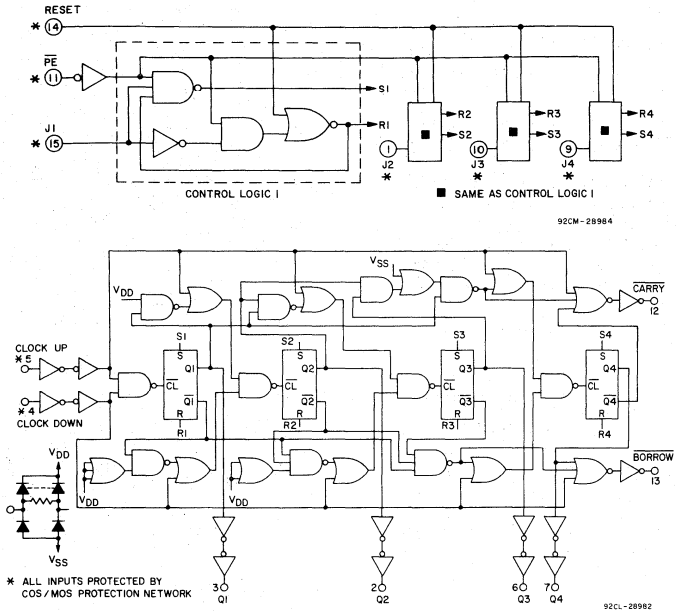


Fig. 2 — CD40193B logic diagram (binary).

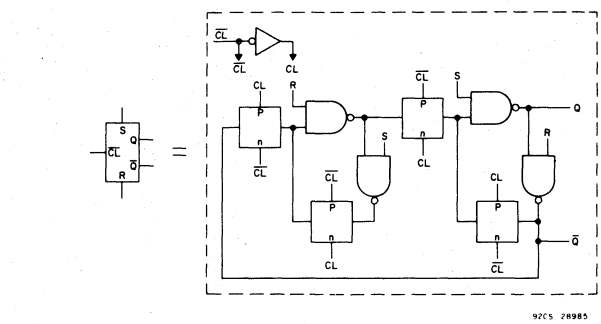


Fig. 4 — Internal logic of Flip-flop.

TRUTH TABLE

CLOCK UP	CLOCK DOWN	$\overline{\text{PRESET}}$ $\overline{\text{ENABLE}}$	RESET	ACTION
⌐	1	1	0	COUNT UP
¬	1	1	0	NO COUNT
1	⌐	1	0	COUNT DOWN
1	¬	1	0	NO COUNT
X	X	0	0	PRESET
X	X	X	1	RESET

1 = HIGH LEVEL 0 = LOW LEVEL X = DON'T CARE

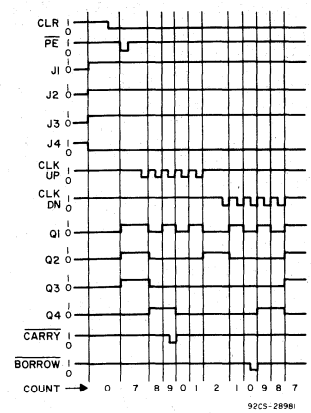


Fig. 3 — CD40192B timing diagram.

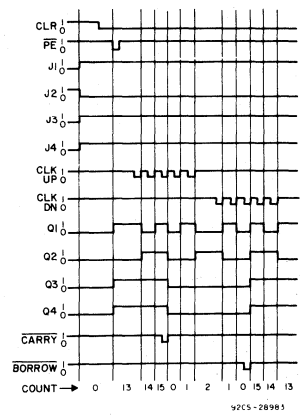


Fig. 5 — CD40193B timing diagram.

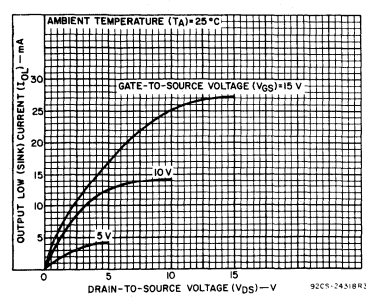


Fig. 6 — Typical output low (sink) current characteristics.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C (unless otherwise specified)

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply Voltage Range (For T_A = Full Temp. Range)	–	3	18	V
Removal Time: RESET or $\overline{PE}$	5	80	–	ns
	10	40	–	
	15	30	–	
Pulse Width: RESET	5	480	–	ns
	10	300	–	
	15	260	–	
$\overline{PE}$	5	240	–	ns
	10	170	–	
	15	140	–	
CLOCK	5	180	–	ns
	10	90	–	
	15	60	–	
Clock Input Frequency	5	DC	2	MHz
	10		4	
	15		5.5	
Clock Rise & Fall Time	5	–	15	μs
	10	–	15	
	15	–	5	

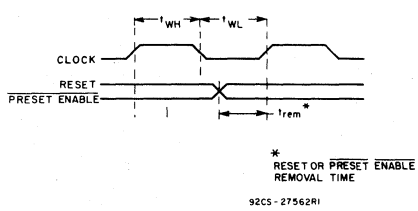


Fig. 10 — Timing diagram defining t_{rem}.

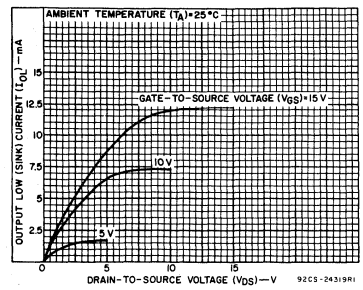


Fig. 7 — Minimum output low (sink) current characteristics.

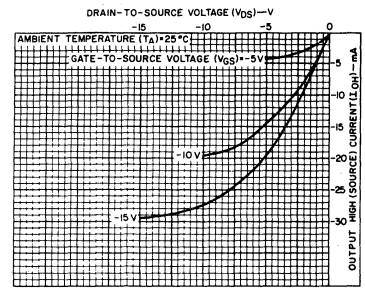


Fig. 8 — Typical output high (source) current characteristics.

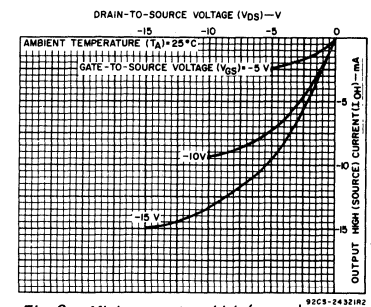


Fig. 9 — Minimum output high (source) current characteristics.

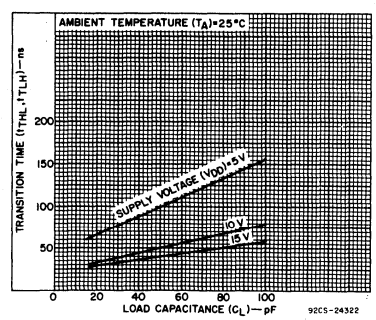


Fig. 11 — Typical transition time as a function of load capacitance.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	-	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

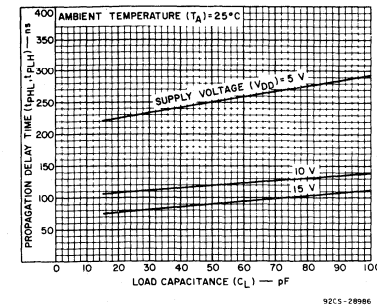


Fig. 12 – Typical propagation delay time as a function of load capacitance.

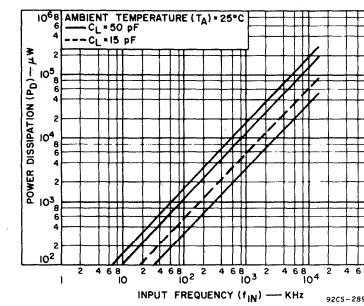


Fig. 13 – Dynamic power dissipation.

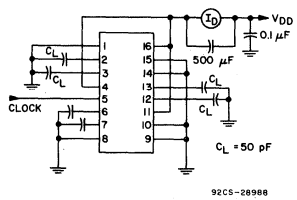


Fig. 14 – Dynamic power dissipation test circuit.

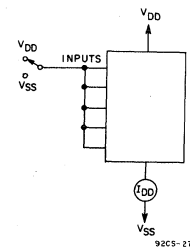


Fig. 15 – Quiescent-device-current test circuit.

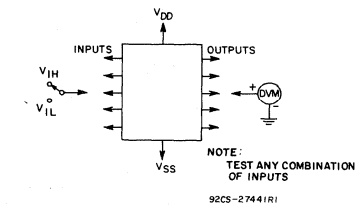


Fig. 16 – Input-voltage test circuit.

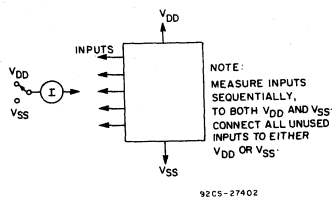


Fig. 17 – Input current test circuit.

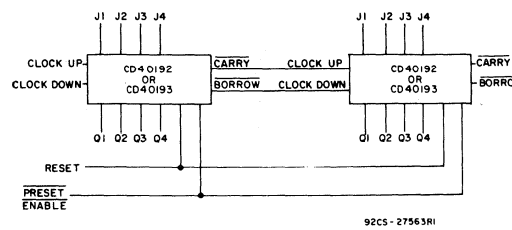
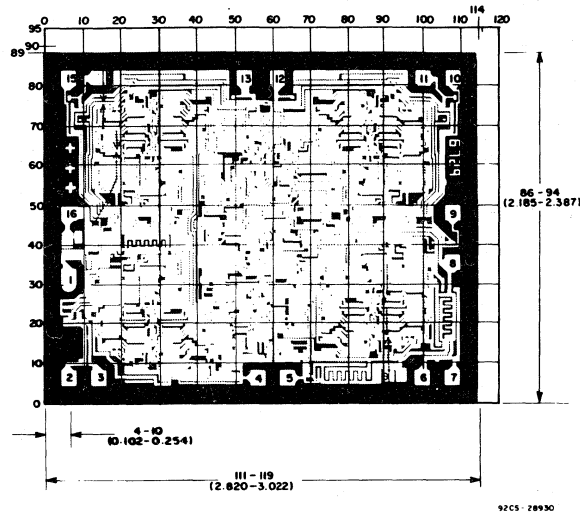


Fig. 18 – Cascaded counter packages.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C
Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	Typ.	Max.	UNITS
Propagation Delay Time t_{PHL}, t_{PLH}: CLOCK UP or CLOCK DOWN to Q, RESET to Q	5	–	250	500	ns
	10	–	120	240	
	15	–	90	180	
$\overline{PE}$ to Q	5	–	200	400	ns
	10	–	100	200	
	15	–	70	140	
CLOCK UP to $\overline{CARRY}$, CLOCK DOWN to $\overline{BORROW}$	5	–	160	320	ns
	10	–	80	160	
	15	–	60	120	
$\overline{RESET}$ or $\overline{PE}$ to $\overline{BORROW}$ or $\overline{CARRY}$	5	–	300	600	ns
	10	–	150	300	
	15	–	110	220	
Transition Time, t_{THL}, t_{TLH}	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Min. Removal Time, t_{rem}* RESET or $\overline{PE}$	5	–	40	80	ns
	10	–	20	40	
	15	–	15	30	
Min. Pulse Width, t_w RESET	5	–	240	480	ns
	10	–	150	300	
	15	–	130	260	
$\overline{PE}$	5	–	120	240	ns
	10	–	85	170	
	15	–	70	140	
CLOCK	5	–	90	180	ns
	10	–	45	90	
	15	–	30	60	
Max. Clock Input Frequency, f_{CL}	5	2	4	–	MHz
	10	4	8	–	
	15	5.5	11	–	
Clock Rise & Fall Time, t_r, t_f	5	–	–	15	μs
	10	–	–	15	
	15	–	–	5	
Input Capacitance, C_{IN}: RESET	–	–	10	15	pF
All Other Inputs	–	–	5	7.5	pF

* The time required for RESET or PRESET ENABLE control to be removed before clocking (see timing diagram, Fig. 10.



Dimensions and pad layout for the CD40192BH (dimensions and pad layout for the CD40193BH are identical).

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CD40194B Types

Preliminary Data

COS/MOS 4-Bit Bidirectional Universal Shift Register

High-Voltage Types (20-Volt Rating)

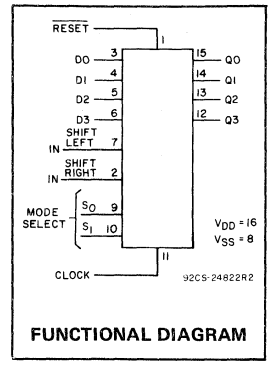
The RCA-CD40194B is a universal shift register featuring parallel inputs, parallel outputs, SHIFT RIGHT and SHIFT LEFT serial inputs, and a direct overriding clear input. In the parallel-load mode (S0 and S1 are high), data is loaded into the associated flip-flop and appears at the output after the positive transition of the CLOCK input. During loading, serial data flow is inhibited. Shift right and shift left are accomplished synchronously on the positive clock edge with data entered at the SHIFT RIGHT and SHIFT LEFT serial inputs, respectively. Clocking of the register is inhibited when both mode control inputs are low. The mode controls should be changed only when the CLOCK input is low. When low, the $\overline{\text{RESET}}$ input resets all stages and forces all outputs low.

The CD40194B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

The CD40194 is similar to industry type 340194.

Features:

- **Medium-speed operation: f_{CL} = 9 MHz (typ.) @ V_{DD} = 10 V**
- **Fully static operation**
- **Synchronous parallel or serial operation**
- **Asynchronous master reset**
- **100% tested for quiescent current at 20 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Standardized, symmetrical output characteristics**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**



FUNCTIONAL DIAGRAM

Applications:

- **Arithmetic unit registers**
- **Serial/parallel conversions**
- **General-purpose registers**

TRUTH TABLE

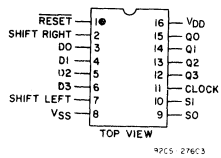
CL	S0	S1	$\overline{\text{RESET}}$	ACTION
X	0	0	1	Do-Nothing
⎍	1	0	1	Shift Right (Q0 toward Q3)
⎍	0	1	1	Shift Left (Q3 toward Q0)
⎍	1	1	1	Parallel Load
X	X	X	0	Reset

1 = HIGH LEVEL
0 = LOW LEVEL
X = DON'T CARE

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V



TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
									+25		
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A = 25° C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ*

CHARACTERISTIC	V_{DD} (V)	TYPICAL VALUES	UNITS
Propagation Delay Time: t_{PLH}, t_{PHL} Clock to Q	5	375	ns
	10	150	
	15	110	
$\overline{RESET}$ to Q, t_{PHL}	5	375	ns
	10	150	
	15	110	
Output Transition Time t_{TLH}, t_{THL}	5	100	ns
	10	50	
	15	40	
Minimum Setup Time: t_S D0, D1, D2, D3, SR, SL to Clock	5	60	ns
	10	25	
	15	20	
S0, S1 to Clock	5	170	ns
	10	70	
	15	50	
Minimum Hold Time: t_H D0, D1, D2, D3, SR, SL, S0, S1 to Clock	5	0	ns
	10	0	
	15	0	
Minimum Pulse Width: t_W Clock	5	85	ns
	10	35	
	15	25	
$\overline{RESET}$	5	160	ns
	10	65	
	15	45	
Maximum Clock Input Frequency, f_{CL}	5	4	MHz
	10	9	
	15	12	
Input Capacitance, C_{IN} (Any Input)	–	5	pF
Maximum Clock Input Rise or Fall Time, t_{rCL}, t_{fCL}	5	15	μs
	10	5	
	15	5	

COS/MOS 4 x 4 Multiport Register

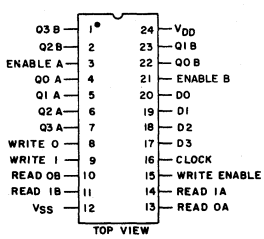
High-Voltage Types (20-Volt Rating)

The RCA-CD40208B is a 4 x 4 multiport register containing four 4-bit registers, write address decoder, two separate read address decoders, and two 3-state output buses.

When the ENABLE input is low, the corresponding output bus is switched, independently of the clock, to a high-impedance state. The high-impedance third state provides the outputs with the capability of being connected to the bus lines in a bus-organized system without the need for interface or pull-up components.

When the WRITE ENABLE input is high, all data input lines are latched on the positive transition of the CLOCK and the data is entered into the word selected by the write address lines. When WRITE ENABLE is low, the CLOCK is inhibited and no new data is entered. In either case, the contents of any word may be accessed via the read address lines independent of the state of the CLOCK input.

The CD40208B types are supplied in hermetic 24-lead dual-in-line ceramic packages (D and F suffixes), 24-lead dual-in-line plastic packages (E suffix), 24-lead ceramic flat packages (K suffix), and in chip form (H suffix).



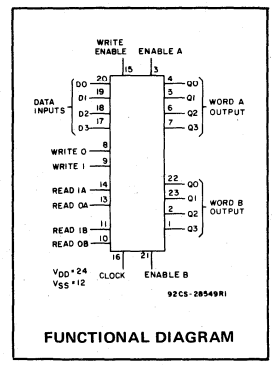
TERMINAL ASSIGNMENT

Features:

- Four 4-bit registers
- One input and two output buses
- Unlimited expansion in bit and word directions
- Data lines have latched inputs
- 3-state outputs
- Separate control of each bus, allowing simultaneous independent reading of any of four registers on Bus A and Bus B and independent writing into any of the four registers
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range):
  - 1 V at V_{DD} = 5 V
  - 2 V at V_{DD} = 10 V
  - 2.5 V at V_{DD} = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Scratch-pad memories
- Arithmetic units
- Data storage



FUNCTIONAL DIAGRAM

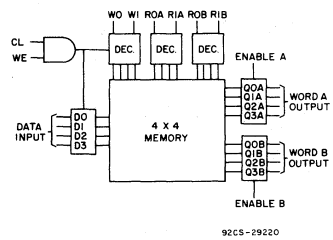


Fig. 1 — Block diagram.

TRUTH TABLE

CLOCK	WRITE ENABLE	WRITE 1	WRITE 0	READ 1A	READ 0A	READ 1B	READ 0B	ENABLE A	ENABLE B	D_n	Q_{nA}	Q_{nB}
⎍⎍	1	S1	S2	S1	S2	S1	S2	1	1	1	1	1
⎍⎍	1	S1	S2	S1	S2	S1	S2	1	1	0	0	0
X	X	X	X	X	X	X	X	0	0	X	Z	Z
⎍⎍	1	0	0	0	1	1	0	1	1	D_n to word 0	Word 1 out	Word 2 out
⎍⎍	0	0	0	0	1	1	0	1	1	Word 0 not altered	Word 1 out	Word 2 out
X	X	X	X	1	0	0	1	1	1	X	Word 2 out	Word 1 out
⎍⎍	X	X	X	X	X	X	X	1	1	X	NC	NC

1 = HIGH LEVEL; 0 = LOW LEVEL; X = DON'T CARE; Z= HIGH IMPEDANCE
S1 and S2 refer to input states of either 1 or 0

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . **−0.5 to +20 V**
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . **−0.5 to V_{DD} +0.5 V**
DC INPUT CURRENT, ANY ONE INPUT . . . . . **±10 mA**
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . **500 mW**
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . **Derate Linearly at 12 mW/°C to 200 mW**
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . **500 mW**
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . **Derate Linearly at 12 mW/°C to 200 mW**
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . **100 mW**
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . **−55 to +125°C**
PACKAGE TYPE E . . . . . **−40 to +85°C**
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . **−65 to +150°C**
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . **+265°C**

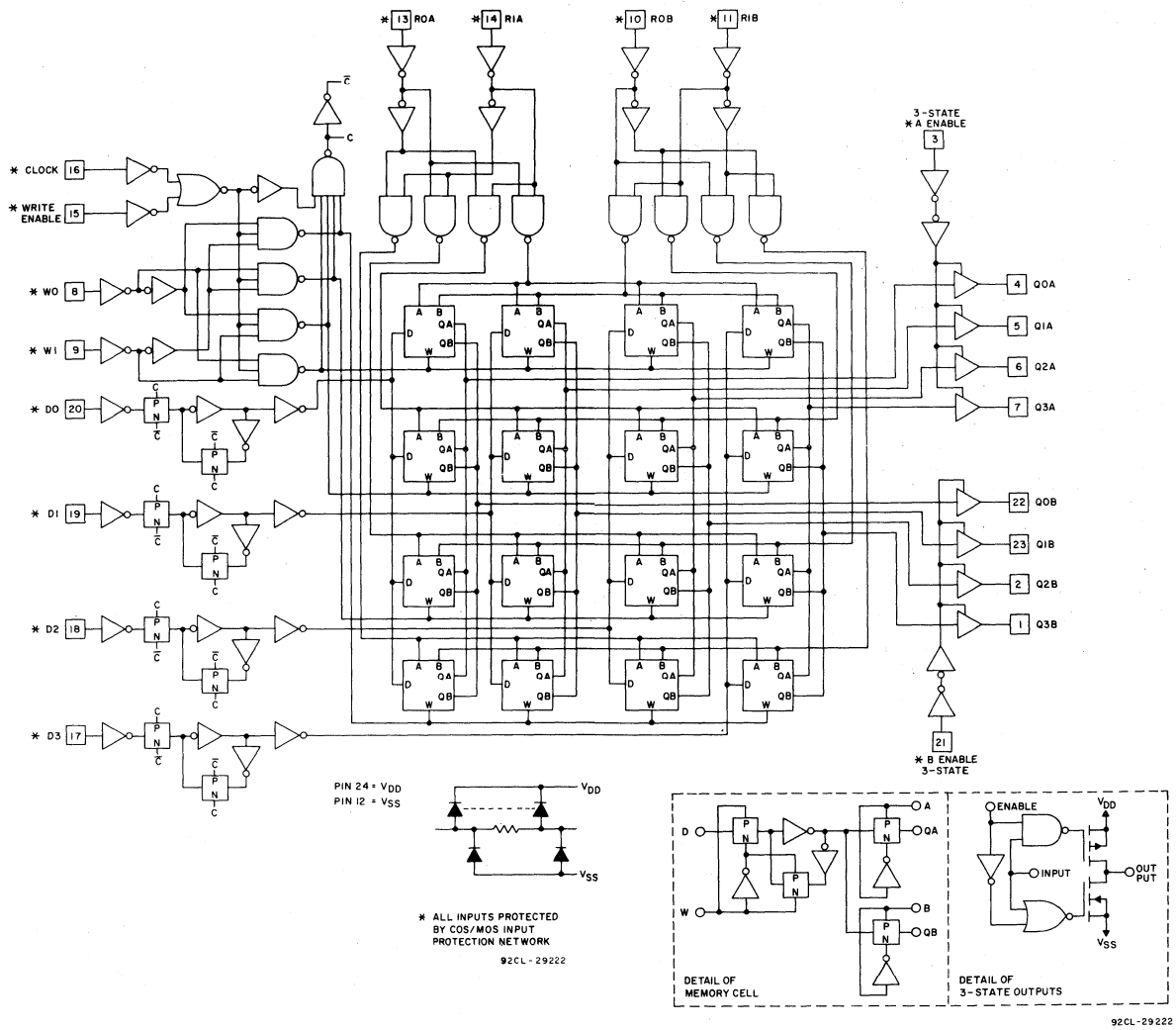


Fig. 2 – Logic diagram.

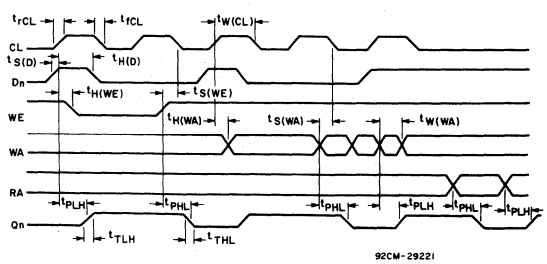


Fig. 3 – Timing diagram.

RECOMMENDED OPERATING CONDITIONS *at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:*

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		MIN.	MAX.	
Supply Voltage Range (For T_A = Full Package Temperature Range)	–	3	18	V
Set-Up Time: Data to Clock, $t_{S(D)}$	5	0	–	ns
	10	0	–	
	15	0	–	
Write Enable to $\overline{\text{Clock}}$, $t_{S(WE)}$	5	250	–	ns
	10	100	–	
	15	70	–	
Write Address to $\overline{\text{Clock}}$, $t_{S(WA)}$	5	250	–	ns
	10	100	–	
	15	70	–	
Hold Time: Data to Clock, $t_{H(D)}$	5	220	–	ns
	10	100	–	
	15	80	–	
Write Enable to Clock, $t_{H(WE)}$	5	270	–	ns
	10	130	–	
	15	80	–	
Write Address to Clock, $t_{H(WA)}$	5	330	–	ns
	10	140	–	
	15	90	–	
Clock Input Frequency, f_{CL}	5	–	1.5	MHz
	10	–	3.5	
	15	–	4.5	
Clock Pulse Width, CL or WE t_W	5	350	–	ns
	10	130	–	
	15	90	–	
Clock Rise or Fall Time, t_rCL or t_fCL	5	–	15	μs
	10	–	5	
	15	–	5	

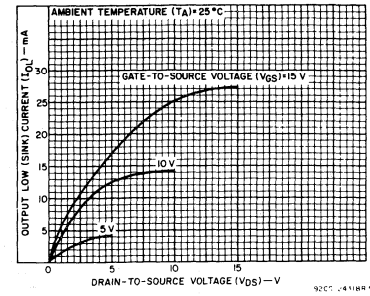


Fig. 4 – Typical output low (sink) current characteristics.

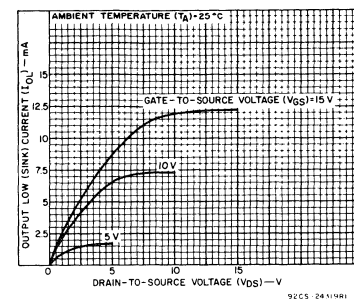


Fig. 5 – Minimum output low (sink) current characteristics.

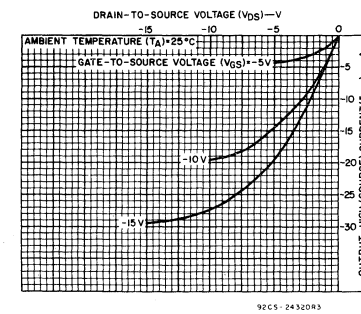


Fig. 6 – Typical output high (source) current characteristics.

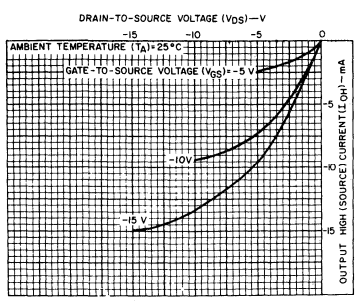


Fig. 7 – Minimum output high (source) current characteristics.

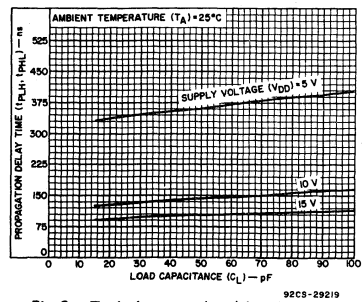


Fig. 8 – Typical propagation delay time as a function of load capacitance (CL or WE to Q).

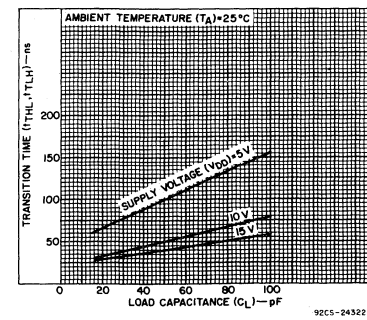


Fig. 9 – Typical transition time as a function of load capacitance.

CD40208B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	-	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

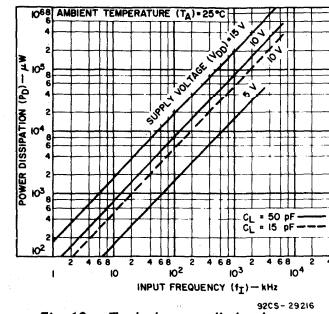


Fig. 10 — Typical power dissipation as a function of input frequency.

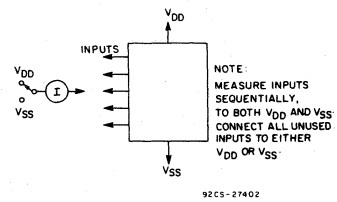


Fig. 11 — Input leakage current test circuit.

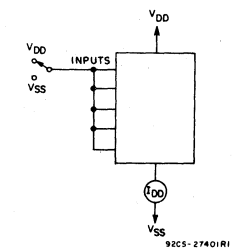
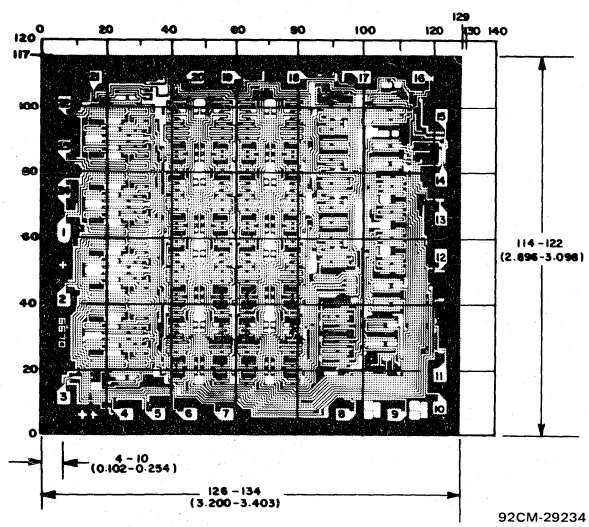


Fig. 12 — Quiescent-device-current test circuit.



Dimensions and Pad Layout for CD40208BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r,t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS			UNITS
		Min.	Typ.	Max.	
Propagation Delay Time:	5	–	360	720	
t_{PHL}, t_{PLH}	10	–	140	280	ns
Clock or Write Enable to Q	15	–	100	200	
Read or Write Address to Q	5	–	300	600	
	10	–	120	240	ns
	15	–	85	170	
3-State Disable Delay Time:	5	–	100	200	
	10	–	50	100	ns
t_{PZH}, t_{PHZ}	15	–	40	80	
t_{PZL}, t_{PLZ}	5	–	130	260	
	10	–	60	120	ns
	15	–	50	100	
Output Transition Time:	5	–	100	200	
t_{THL}, t_{TLH}	10	–	50	100	ns
	15	–	40	80	
Minimum Setup Time:	5	–	−95	0	
Data to Clock $t_{S(D)}$	10	–	−35	0	ns
	15	–	−20	0	
	5	–	125	250	
Write Enable to $\overline{\text{Clock}}$ $t_{S(WE)}$	10	–	50	100	ns
	15	–	35	70	
	5	–	125	250	
Write Address to $\overline{\text{Clock}}$ $t_{S(WA)}$	10	–	50	100	ns
	15	–	35	70	
Clock Rise and Fall Time:	5	–	–	15	
t_rCL, t_fCL	10	–	–	5	μs
	15	–	–	5	
Minimum Hold Time:	5	–	110	220	
Data to Clock $t_{H(D)}$	10	–	50	100	ns
	15	–	40	80	
	5	–	135	270	
Write Enable to Clock $t_{H(WE)}$	10	–	65	130	ns
	15	–	40	80	
	5	–	165	330	
Write Address to $\overline{\text{Clock}}$ $t_{S(WA)}$	10	–	70	140	ns
	15	–	45	90	
Maximum Clock Input Frequency,	5	1.5	3	–	
f_{CL}	10	3.5	7	–	MHz
	15	4.5	9	–	
Minimum Clock Pulse Width,	5	–	175	350	
Clock or Write Enable	10	–	65	130	ns
$t_{W(CL)}$	15	–	45	90	
Write Address	5	–	150	300	
$t_{W(WA)}$	10	–	75	150	ns
	15	–	45	90	
Average Input Capacitance, (Any Input) C_I	–	–	5	7.5	pF

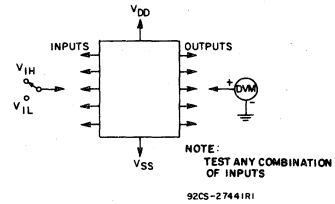
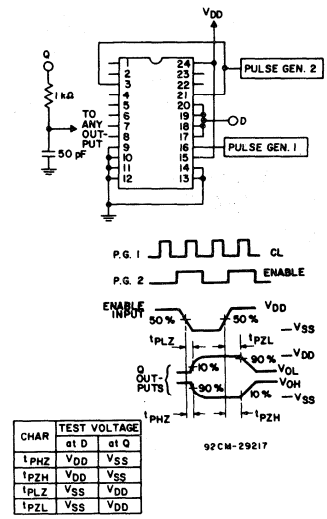


Fig. 13 – Input-voltage test circuit.



CHAR	TEST VOLTAGE	
	at D	at Q
t_{PHZ}	V_{DD}	V_{SS}
t_{PZH}	V_{DD}	V_{SS}
t_{PLZ}	V_{SS}	V_{DD}
t_{PZL}	V_{SS}	V_{DD}

Fig. 14 – Output-enable-delay-times test circuit and waveforms.

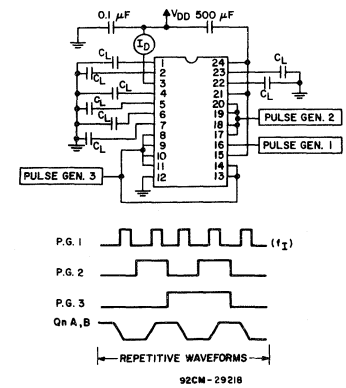


Fig. 15 – Power-dissipation test circuit and waveforms.

COS/MOS
Quad 2-Line-to-1-Line
Data Selector/Multiplexer

High-Voltage Types (20-Volt Rating)

The RCA-CD40257B is a Data Selector/Multiplexer featuring three-state outputs which can interface directly with and drive data lines of bus-oriented systems.

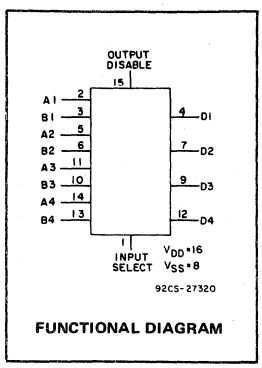
The CD40257B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Applications:

- **Digital Multiplexing**
- **Shift-right/shift-left registers**
- **True/complement selection**

Features:

- **3-state outputs**
- **Standardized, symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (over full package-temperature range):**
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**



FUNCTIONAL DIAGRAM

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)	3	18	V

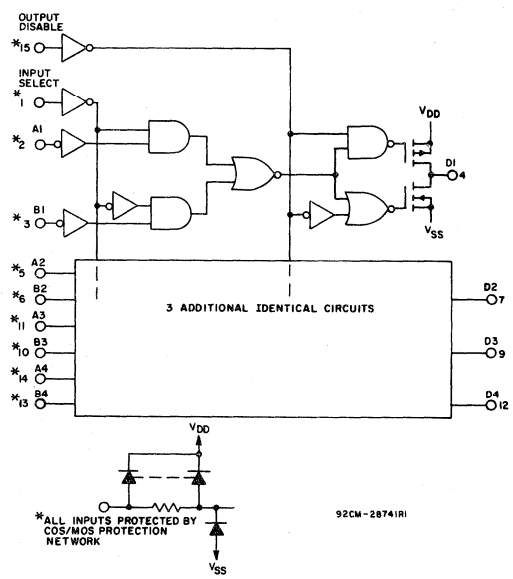


Fig. 1 – Logic diagram for CD40257B.

TRUTH TABLE

INPUTS				OUTPUT
3-STATE OUTPUT DISABLE	SELECT	A	B	D
1	X	X	X	Z
0	0	0	X	0
0	0	1	X	1
0	1	X	0	0
0	1	X	1	1

X = DON'T CARE LOGIC 1 = HIGH
LOGIC 0 = LOW Z = HIGH IMPEDANCE

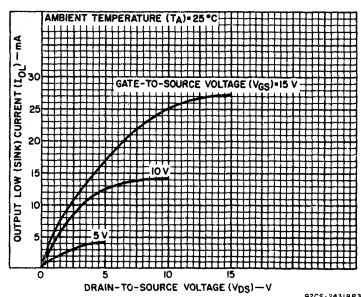


Fig. 2 – Typical output low (sink) current characteristics.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

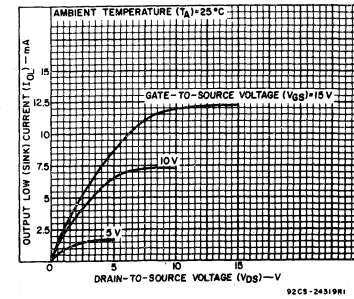


Fig.3 – Minimum output low (sink) current characteristics.

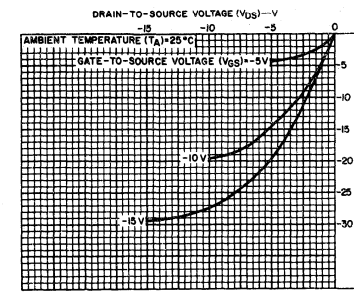


Fig.4 – Typical output high (source) current characteristics.

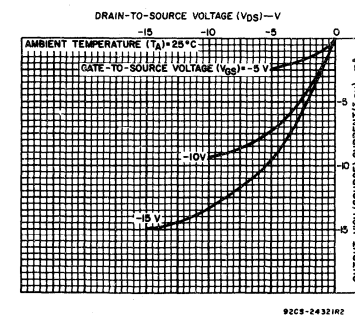


Fig.5 – Minimum output high (source) current characteristics.

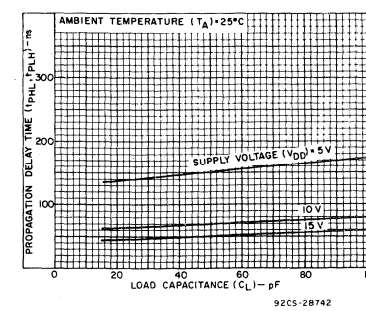


Fig.6 – Typical propagation delay time as a function of load capacitance (DATA INPUT to OUTPUT).

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at −55,+25,+125 Apply to D,K,F,H Pkgs. Values at −40,+25,+85 Apply to E Pkgs. −55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA
3-State Output Leakage Current I_{OUT} Max.	–	0,18	18	±0.4	±0.4	±12	±12	–	$±10^{-4}$	±0.4	μA

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		V_{DD}(V)	Typ.	Max.	
Propagation Delay Time: Data Input to Output, t_{PHL}, t_{PLH}		5	150	300	ns
		10	70	140	
		15	50	100	
Select to Output, t_{PHL}, t_{PLH}		5	190	380	ns
		10	85	170	
		15	65	130	
Output Disable to Output, t_{PHL}, t_{PLH}		5	95	190	ns
		10	50	100	
		15	40	80	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input	–	5	7.5	pF

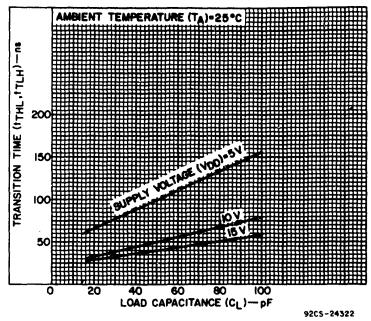


Fig.7 – Typical transition time as a function of load capacitance.

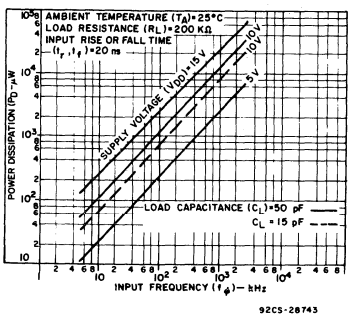


Fig.8 – Typical dynamic power dissipation as a function of input frequency (one INPUT to one OUTPUT).

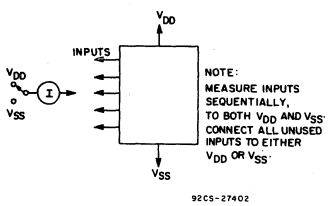


Fig.9 – Input current test circuit.

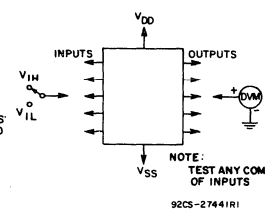


Fig.10 – Input voltage test circuit.

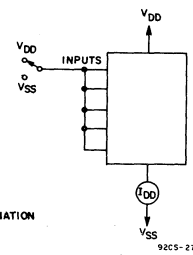
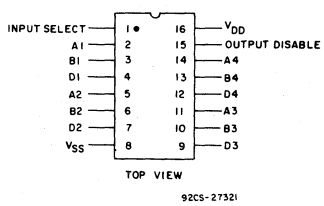
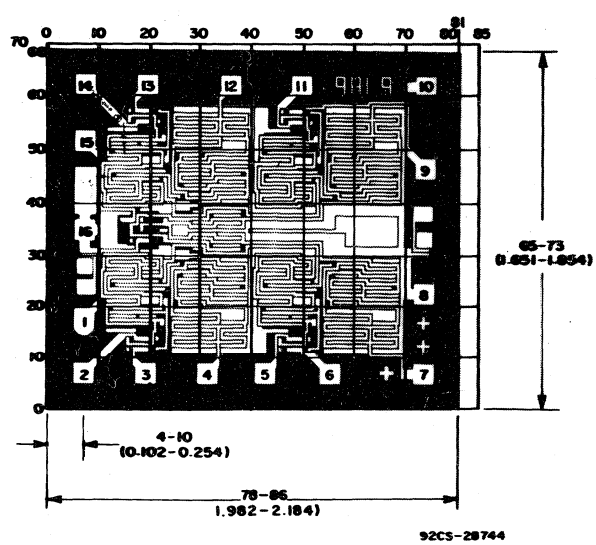


Fig.11 – Quiescent device current test circuit.



TERMINAL ASSIGNMENT

Dimensions and pad layout for CD40257BH.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS A-Series Integrated Circuits

Technical Data

COS/MOS NOR Gates

Dual 3 Input plus Inverter—CD4000A
Quad 2 Input—CD4001A
Dual 4 Input—CD4002A
Triple 3 Input—CD4025A

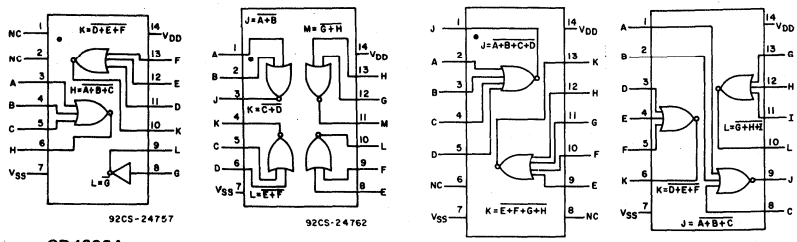
The RCA-CD4000A, CD4001A, CD4002A, and CD4025A NOR gates provide the system designer with direct implementation of the NOR function and supplement the existing family of COS/MOS gates.

These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

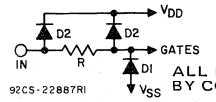
Features:

- **Quiescent current specified to 15 V**
- **Maximum input leakage of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

FUNCTIONAL DIAGRAMS



CD4000A CD4001A CD4002A CD4025A



ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . -65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . -55 to +125°C
PACKAGE TYPE E . . . . . -40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): . . . . . -0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):
FOR T_A = -40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = -55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . -0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	12	V

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A = 25°C, C_L = 15 pF, Input t_r, t_f = 20 ns*

CHARACTERISTIC	TEST CONDITIONS	LIMITS				UNITS
		D, F, K, H PACKAGES		E PACKAGE		
	V_{DD} (Volts)	TYP.	MAX.	TYP.	MAX.	
Propagation Delay Time: High-to-Low Level, t_{PHL}	5	35	50	35	80	ns
	10	25	40	25	55	
Low-to-High Level, t_{PLH}	5	35	95	35	120	ns
	10	25	45	25	65	
Transition Time: High-to-Low Level, t_{THL}	5	65	125	65	200	ns
	10	35	70	35	115	
Low-to-High Level, t_{TLH}	5	65	175	65	300	ns
	10	35	75	35	125	
Input Capacitance, C_I	Any Input	5	–	5	–	pF

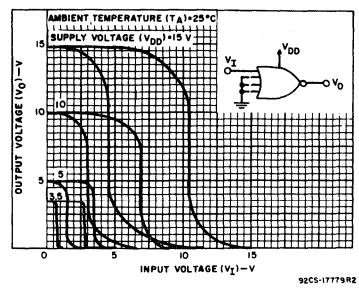


Fig. 1 — Minimum & maximum voltage transfer characteristics.

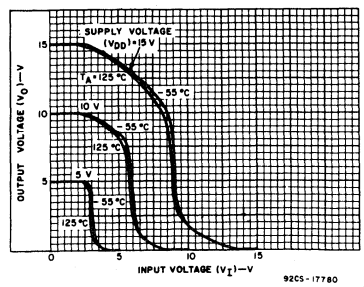


Fig. 2 — Typical voltage transfer characteristics as a function of temperature.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
				D, K, F, H PACKAGES				E PACKAGE				
					+25				+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	TYP.	LIMIT	+125	-40	TYP.	LIMIT	+85	
Quiescent Device Current, I_L Max.	–	–	5	0.05	0.001	0.05	3	0.5	0.005	0.5	15	μA
	–	–	10	0.1	0.001	0.1	6	5	0.005	5	30	
	–	–	15	2	0.02	2	40	50	0.5	50	500	
Output Voltage: Low Level, V_{OL}	–	0, 5	5	0 Typ., 0.05 Max								V
	–	0, 10	10	0 Typ., 0.05 Max								
High Level V_{OH}	–	0, 5	5	4.95 Min.; 5 Typ.								
	–	0, 10	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	3.6	–	5	1.5 Min.; 2.25 Typ.								V
	7.2	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	1.4	–	5	1.5 Min.; 2.25 Typ.								
	2.8	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink), I_DN Min.	0.4	–	5	0.5	1	0.4	0.28	0.35	1	0.3	0.24	mA
	0.5	–	10	1.1	2.5	0.9	0.65	0.72	2.5	0.6	0.48	
P-Channel (Source): I_DP Min.	2.5	–	5	-0.62	-2	-0.5	-0.35	-0.35	-2	-0.3	-0.24	
	9.5	–	10	-0.62	-1	-0.5	-0.35	-0.3	-1	-0.25	-0.2	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		15	$\pm 10^{-5}$ Typ., ±1 Max.								μA

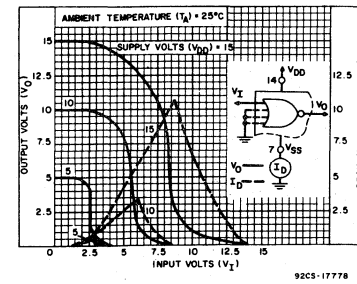


Fig. 3 – Typical current & voltage transfer characteristics.

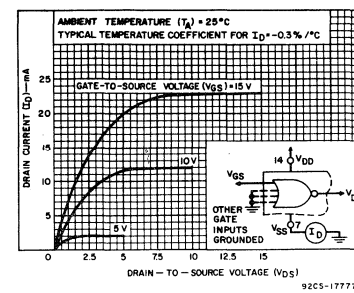


Fig. 4 – Typical n-channel drain characteristics.

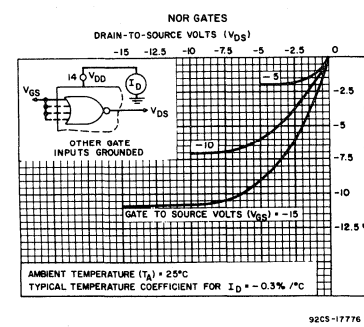


Fig. 5 – Typical p-channel drain characteristics.

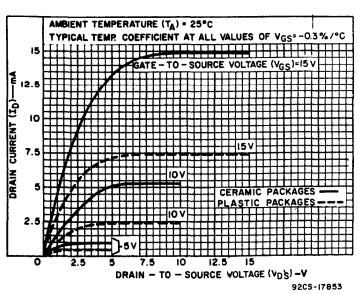


Fig. 6 – Minimum n-channel drain characteristics.

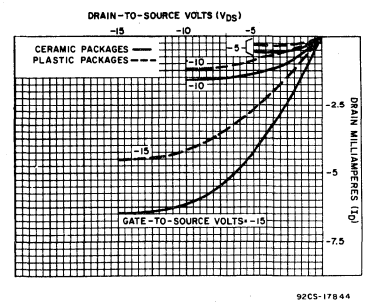


Fig. 7 – Minimum p-channel drain characteristics.

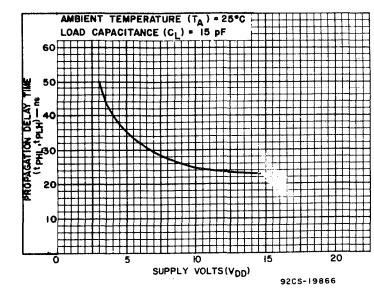


Fig. 8 – Typical propagation delay time vs. V_{DD}.

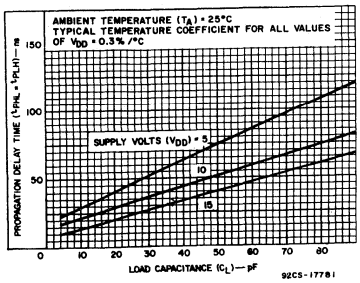


Fig. 9 — Typical propagation delay time vs. C_L.

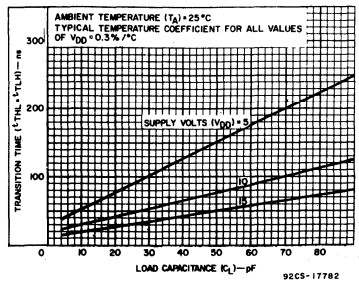


Fig. 10 — Typical transition time vs. C_L.

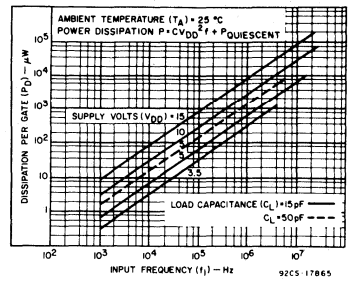


Fig. 11 — Typical dissipation characteristics.

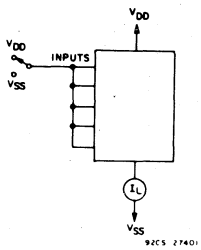
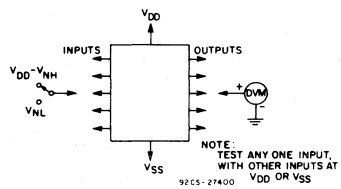


Fig. 12 — Quiescent device current test circuit.



NOTE:
CD4000, CD4002, CD4025 – TEST ANY ONE INPUT WITH OTHER INPUTS AT V_{DD} OR V_{SS}.

CD4001 – TEST ANY COMBINATION OF INPUTS.

Fig. 13 — Noise immunity test circuit.

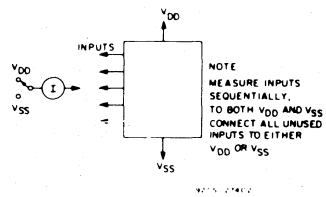


Fig. 14 — Input leakage current test circuit.

COS/MOS 18-Stage Static Shift Register

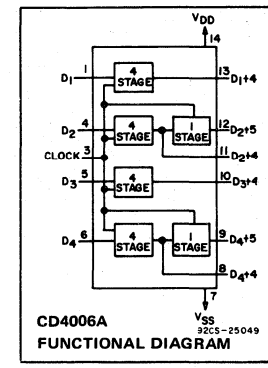
The RCA-CD4006A types are comprised of 4 separate shift register sections: two sections of four stages and two sections of five stages with an output tap at the fourth stage. Each section has an independent single-rail data path.

A common clock signal is used for all stages. Data are shifted to the next stage on negative-going transitions of the clock. Through appropriate connections of inputs and outputs, multiple register sections of 4, 5, 8, and 9 stages or single register sections of 10, 12, 13, 14, 16, 17 and 18 stages can be implemented using one CD4006A package. Longer shift register sections can be assembled by using more than one CD4006A.

Features:

- **Fully static operation**
- **Shifting rates up to 5 MHz**
- **Permanent register storage with clock line high or low – – no information recirculation required**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).



CD4006A FUNCTIONAL DIAGRAM

Applications:

- **Serial shift registers**
- **Time delay circuits**
- **Frequency division**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C

PACKAGE TYPE E . . . . . –40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal) . . . . . –0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = –40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = –55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max . . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D,F,K,H Packages		*E Package*		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Data Setup Time, t_S	5	80	–	100	–	ns
	10	40	–	50	–	
Clock Pulse Width, t_W	5	500	–	830	–	ns
	10	200	–	250	–	
Clock Input Frequency, f_{CL}	5	dc	1	dc	0.6	MHz
	10	dc	2.5	dc	2	
Clock Rise and Fall Time, t_rCL, t_fCL*	5	–	15	–	15	μs
	10	–	5	–	5	

* If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

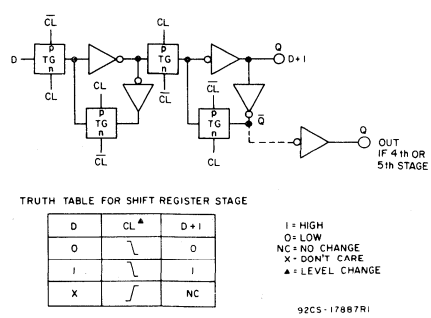


Fig. 1 – Logic diagram and truth table (one register stage).

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				E Package				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	0.5	0.01	0.5	30	5	0.03	5	70	μA
	–	–	10	1	0.01	1	60	10	0.05	10	140	
	–	–	15	25	0.5	25	1000	250	2.5	250	2500	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level, V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: n-Channel (Sink), I_DN Min.	0.5	–	5	0.155	0.25	0.125	0.085	0.072	0.25	0.06	0.048	mA
	0.5	–	10	0.31	0.5	0.25	0.175	0.15	0.5	0.125	0.1	
p-Channel (Source): I_DP Min.	4.5	–	5	-0.125	-0.15	-0.1	-0.07	-0.06	-0.15	-0.05	-0.04	
	9.5	–	10	-0.25	-0.3	-0.2	-0.14	-0.12	-0.3	-0.1	-0.08	
Input Leakage Current, I_{IL}, I_{IH}	Any Input											μA
	–	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								

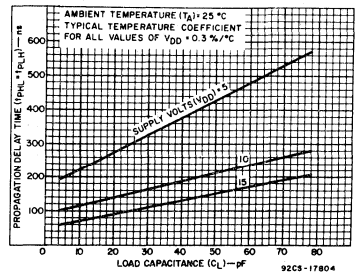


Fig. 2 – Typical propagation delay time vs. load capacitance.

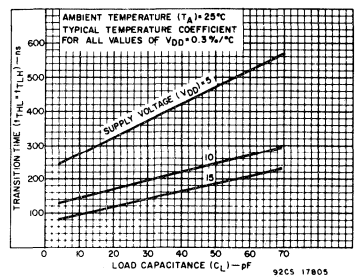


Fig. 3 – Typical transition time vs. load capacitance.

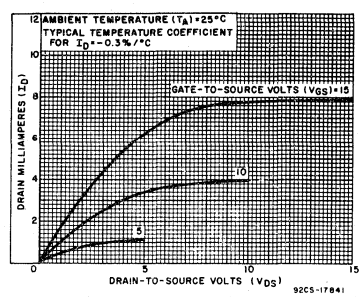


Fig. 5 – Typical output n-channel drain characteristics.

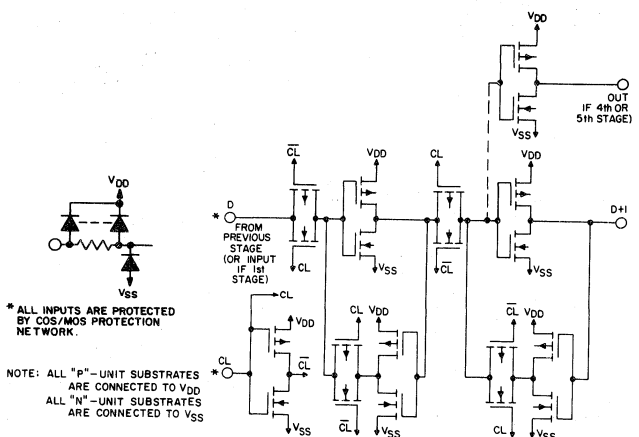


Fig. 4 – Schematic diagram (one register stage).

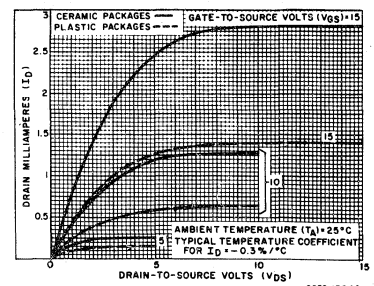


Fig. 6 – Minimum output n-channel drain characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
			D,F,K,H Packages			*E Package*			
		V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
Propagation Delay Time; t_{PLH}, t_{PHL}		5	–	250	400	–	250	500	ns
		10	–	125	200	–	125	250	
Transition Time; t_{THL}, t_{TLH}		5	–	250	400	–	250	500	ns
		10	–	125	200	–	125	250	
Maximum Clock Input Frequency, f_{CL}		5	1	2.5	–	0.6	2.5	–	MHz
		10	2.5	5	–	2	5	–	
Minimum Clock Pulse Width, t_W		5	–	200	500	–	200	830	ns
		10	–	100	200	–	100	250	
Clock Rise & Fall Time; t_rCL, t_fCL*		5	–	–	15	–	–	15	μs
		10	–	–	5	–	–	5	
Minimum Data Set Up Time, t_S		5	–	50	80	–	50	100	ns
		10	–	25	40	–	25	50	
Average Input Capacitance, C_I	Data Input		–	5	–	–	5	–	pF
	Clock Input		–	30	–	–	30	–	pF

* If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

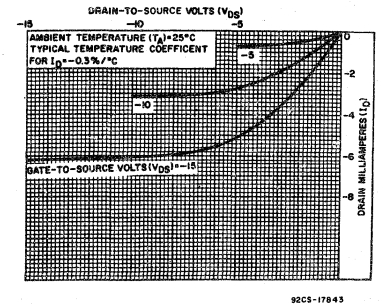


Fig. 7 – Typical output p-channel drain characteristics.

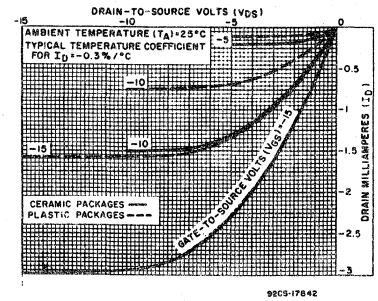


Fig. 8 – Minimum output p-channel drain characteristics.

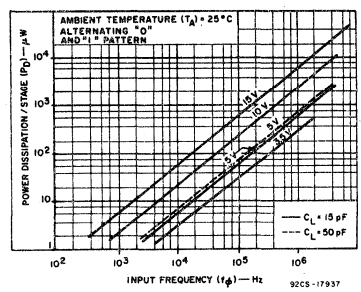


Fig. 9 – Typical dissipation characteristics.

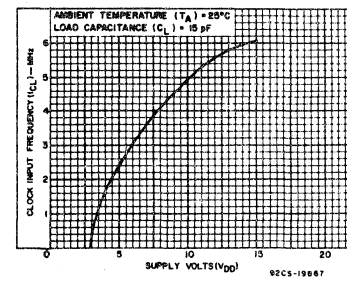


Fig. 10 – Typical clock input frequency vs. supply voltage.

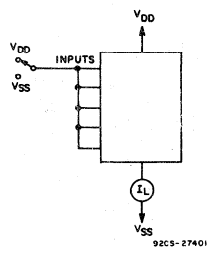


Fig. 11 – Quiescent-device-current test circuit.

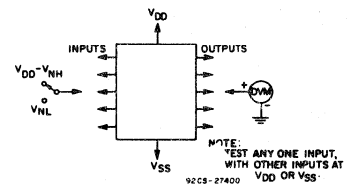


Fig. 12 – Noise-immunity test circuit.

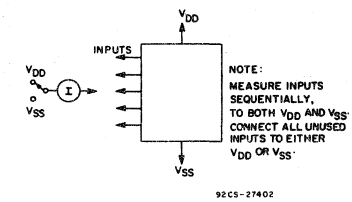


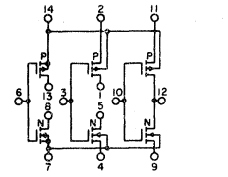
Fig. 13 – Input-leakage-current test circuit.

COS/MOS Dual Complementary Pair Plus Inverter

The RCA-CD4007A types are comprised of three n-channel and three p-channel enhancement-type MOS transistors. The transistor elements are accessible through the package terminals to provide a convenient means for constructing the various typical circuits as shown in Fig. 2.

More complex functions are possible using multiple packages. Numbers shown in parentheses indicate terminals that are connected together to form the various configurations listed.

These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).



Terminal No.14 – V_{DD}
Terminal No. 7 – V_{SS}

CD4007A
SCHEMATIC DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) ..... −65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H ..... −55 to +125°C
PACKAGE TYPE E ..... −40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... −0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A = −40 to +60°C (PACKAGE TYPE E) ..... 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) ..... 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	D,F,K,H Packages		E Package		
	Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	12	3	12	V

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		D,F,K,H Packages			E Package			
	V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
Propagation Delay Time; t_{PLH}, t_{PHL}	5	–	35	60	–	35	75	ns
	10	–	20	40		20	50	
Transition Time; t_{THL}, t_{TLH}	5	–	50	75	–	50	100	ns
	10	–	30	40		30	50	
Average Input Capacitance, C_I	Any Input	–	5	–	–	5	–	pF

Features:

- **Medium-speed operation. . . . t_{PHL} = t_{PLH} = 20 ns (typ.) at C_L = 15 pF, + V_{DD} = 10 V**
- **Low "high" and "low" output impedance. . 500 Ω (typ.) at V_{DD} – V_{SS} = 10 V**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Extremely high-input impedance amplifiers**
- **Shapers**
- **Inverters**
- **Threshold detector**
- **Linear amplifiers**

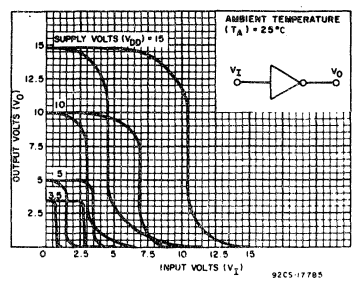


Fig. 1 – Minimum and maximum voltage-transfer characteristics for inverter.

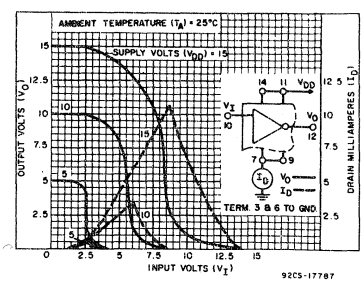


Fig. 2 – Typical current and voltage-transfer characteristics for inverter.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				E Package				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current: I_L Max.	–	–	5	0.05	0.001	0.05	3	0.5	0.005	0.5	15	μA
	–	–	10	0.1	0.001	0.1	6	1	0.005	1	30	
	–	–	15	2	0.02	2	40	50	0.5	50	500	
Output Voltage Low Level V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low V_{NL}	3.6	–	5	1.5 Min.; 2.25 Typ.								V
	7.2	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	1.4	–	5	1.5 Min.; 2.25 Typ.								
	2.8	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink) I_DN Min.	0.4*	V_I=	5	0.75	1	0.6	0.4	0.35	1	0.3	0.24	mA
	0.5	V_{DD}	10	1.6	2.5	1.3	0.95	1.2	2.5	1	0.8	
P-Channel (Source): I_DP Min.	2.5†	V_I=	5	−1.75	−4	−1.4	−1	−1.3	−4	−1.1	−0.9	
	9.5	V_{DD}	10	−1.35	−2.5	−1.1	−0.75	−0.65	−2.5	−0.55	−0.45	
Input Leakage Current: I_{IL}, I_{IH}	Any Input		15	$\pm 10^{-5}$ Typ., ±1 Max.								μA

*Maximum noise-free low-level bipolar output voltage. †Minimum noise-free high-level bipolar output voltage.

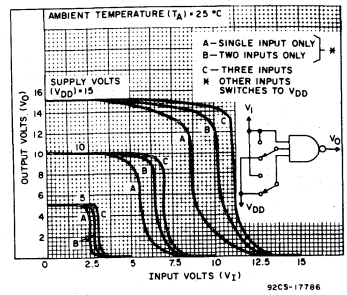


Fig. 3 – Typical voltage-transfer characteristics for NAND gate.

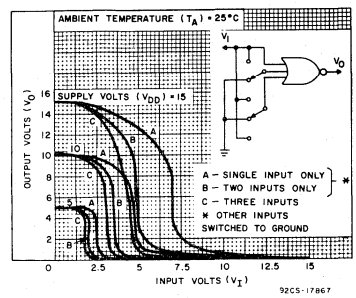


Fig. 4 – Typical voltage-transfer characteristics for NOR gate.

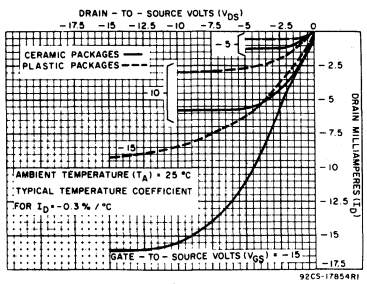


Fig. 5 – Minimum output p-channel drain characteristics.

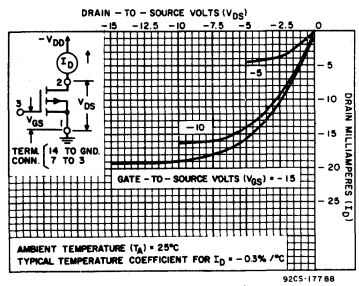


Fig. 6 – Typical output p-channel drain characteristics.

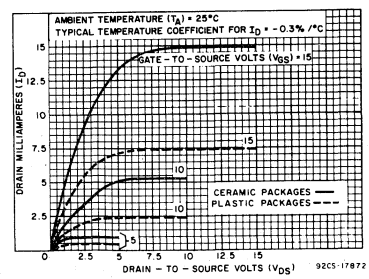


Fig. 7 – Minimum output n-channel drain characteristics.

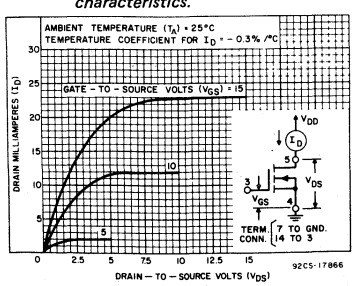


Fig. 8 – Typical output n-channel drain characteristics.

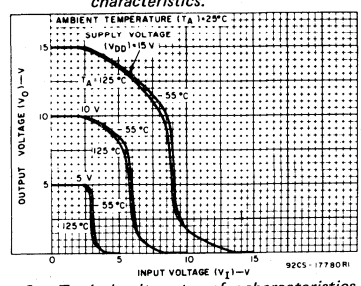


Fig. 9 – Typical voltage-transfer characteristics as a function of temperature.

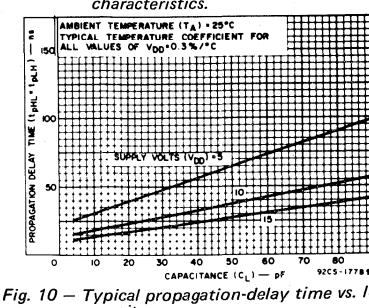


Fig. 10 – Typical propagation-delay time vs. load capacitance.

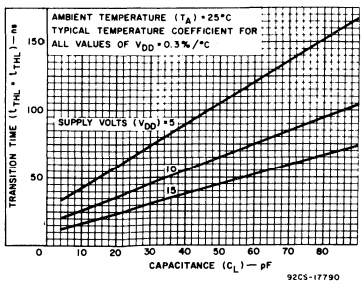


Fig. 11 — Typical transition time vs. load capacitance.

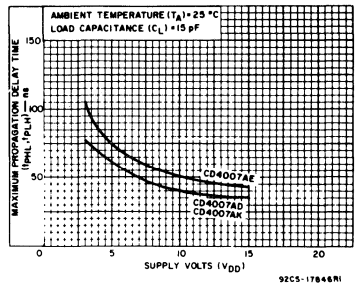


Fig. 12 — Maximum propagation-delay time vs. supply voltage.

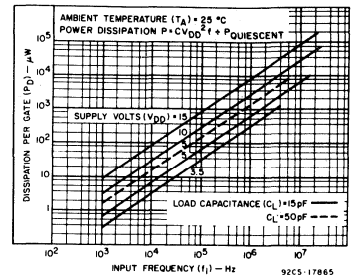
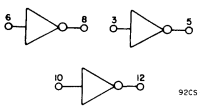
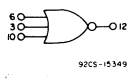


Fig. 13 — Typical dissipation characteristics.



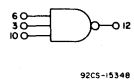
(14,2,11); (8,13); (1,5); (7,4,9)

a) Triple Inverters



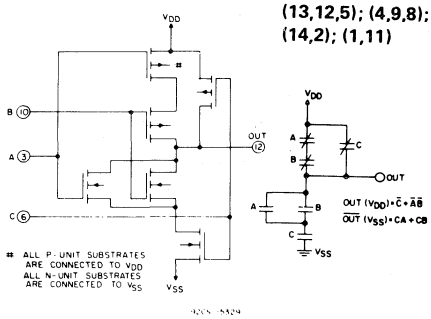
(13,2); (1,11); (12,5,8); (7,4,9)

b) 3-Input NOR Gate

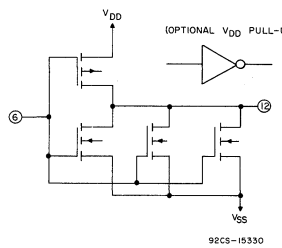


(1,12,13); (2,14,11); (4,8); (5,9)

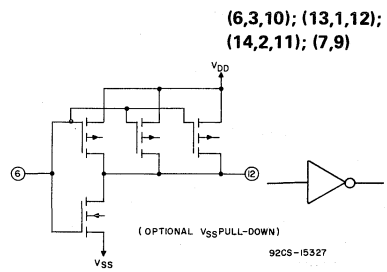
c) 3-Input NAND Gate



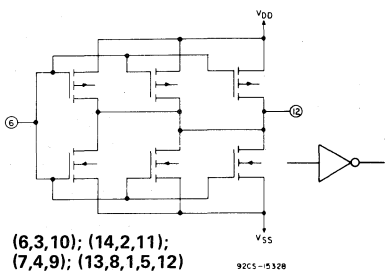
d) Tree (Relay) Logic



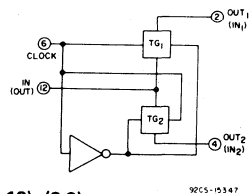
e) High Sink-Current Driver



f) High Source-Current Driver



g) High Sink- and Source-Current Driver



(1,5,12); (2,9); (11,4); (8,13,10); (6,3)

h) Dual Bi-Directional Transmission Gating

Fig. 14 — Sample COS/MOS logic circuit arrangements using type CD4007A.

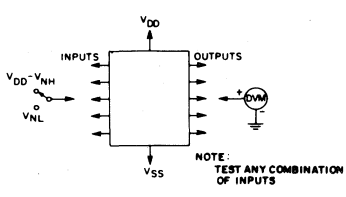


Fig. 15 — Noise-immunity test circuit.

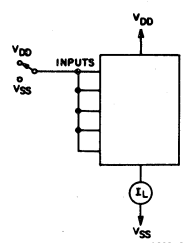


Fig. 16 — Quiescent-device-current test circuit.

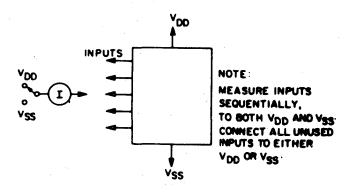


Fig. 17 — Input-leakage-current test circuit.

COS/MOS 4-Bit Full Adder

With Parallel Carry Out

The RCA-CD4008A types consist of four full-adder stages with fast look-ahead carry provision from stage to stage. Circuitry is included to provide a fast "parallel-carry-out" bit to permit high-speed operation in arithmetic sections using several CD4008A's. CD4008A inputs include the four sets of bits to be added, A_1 to A_4 and B_1 to B_4, in addition to the "Carry In" bit from a previous section. CD4008A outputs include the four sum bits, S_1 and S_4, in addition to the high-speed "parallel-carry-out" which may be utilized at a succeeding CD4008A section.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

Applications

- **Binary addition/arithmetic units**

Features:

- **4 sum outputs plus parallel look-ahead carry-output**
- **Quiescent current specified to 15 V**
- **Maximum input leakage of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H. . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): . . . . . −0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):
FOR T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max . . . . . +265°C

STATIC ELECTRICAL CHARACTERISTICS

Characteristic		Conditions V_O (V)	Conditions V_{IN} (V)	Conditions V_{DD} (V)	Limits at Indicated Temperatures (°C) D,K,F,H Packages −55	+25 Typ.	+25 Limit	D,K,F,H Packages +125	E Package −40	E Package +25 Typ.	E Package +25 Limit	E Package +85	Units
Quiescent Device Current, I_L Max.		–	–	5	5	0.3	5	300	50	0.5	50	700	μA
		–	–	10	10	0.5	10	600	500	1	100	1400	
		–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}		–	0,5	5	0 Typ.; 0.05 Max.								V
		–	0,10	10	0 Typ.; 0.05 Max.								
High Level, V_{OH}		–	0,5	5	4.95 Min.; 5 Typ.								
		–	0,10	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}		4.2	–	5	1.5 Min.; 2.25 Typ.								V
		9	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}		0.8	–	5	1.5 Min.; 2.25 Typ.								
		1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}		4.5	–	5	1 Min.								V
		9	–	10	1 Min.								
Inputs High, V_{NMH}		0.5	–	5	1 Min.								
		1	–	10	1 Min.								
Output Drive Current: n-Channel (Sink), I_DN Min.	*	0.5	–	5	0.31	0.5	0.25	0.175	0.155	0.5	0.13	0.105	mA
	*	0.5	–	10	0.93	1.5	0.75	0.53	0.6	1.5	0.5	0.4	
	▲	3	–	5	0.012	0.2	0.01	0.007	0.009	0.2	0.007	0.005	
	▲	3	–	10	0.31	0.5	0.25	0.175	0.24	0.5	0.2	0.16	
p-Channel (Source), I_DP Min.	*	4.5	–	5	-0.31	-0.5	-0.25	-0.175	-0.155	-0.5	-0.13	-0.105	
	*	9.5	–	10	-0.93	-1.5	-0.75	-0.53	-0.6	-1.5	-0.5	-0.4	
	▲	2	–	5	-0.012	-0.2	-0.01	-0.007	-0.008	-0.2	-0.007	-0.005	
	▲	7	–	10	-0.185	-0.3	-0.15	-0.105	-0.12	-0.3	-0.1	-0.08	
Input Leakage Current, I_{IL}, I_{IH} Max.		Any Input		15	$\pm 10^{-5}$ Typ.; ±1 Max.								μA

* Carry Output ▲Sum Output

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	Min.	Max.	Units
Supply-Voltage Range (T_A= Full Package-Temp. Range)	3	12	V

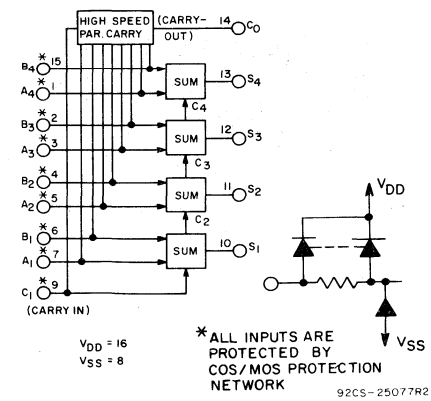


Fig. 1 — CD4008A logic diagram.

TRUTH TABLE

A_i	B_i	C_i	C_0	SUM
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

CD4008A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 KΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D,F,K,H Packages		*E Package*		
		Typ.	Max.	Typ.	Max.	
Propagation Delay Time: t_{PHL}, t_{PLH} Sum In to Sum Out	5	900	1300	900	2000	ns
	10	325	500	325	650	
Carry In to Sum Out	5	900	1300	900	2000	ns
	10	325	500	325	650	
Sum In to Carry Out	5	320	600	320	800	ns
	10	120	200	120	240	
Carry In to Carry Out	5	100	175	100	200	ns
	10	45	75	45	90	
Transition Time: t_{THL}, t_{TLH} At Sum Outputs	5	1250	2200	1250	2900	ns
	10	550	900	550	1100	
At Carry Output	5	125	225	125	290	ns
	10	45	75	45	90	
Input Capacitance, C_I (Any Input)	—	10	—	10	—	pF

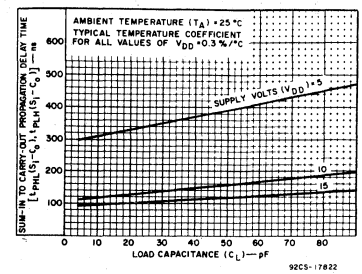


Fig. 2 – Typical sum-in to carry out propagation delay time vs. C_L.

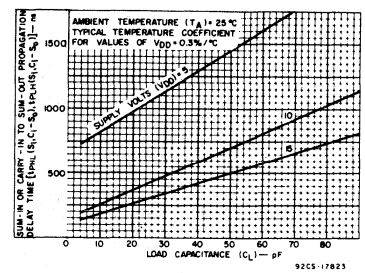


Fig. 3 – Typical sum-in or carry-in to sum-out propagation delay time vs. C_L.

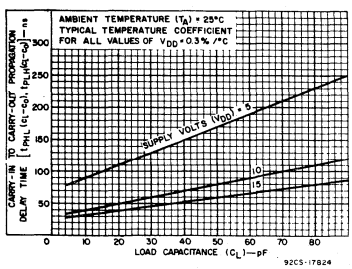


Fig. 4 – Typical carry-in to carry-out propagation delay time vs. C_L.

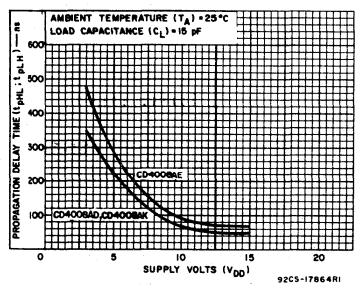


Fig. 5 – Typical maximum propagation delay time vs. V_{DD} for carry-in to carry-out.

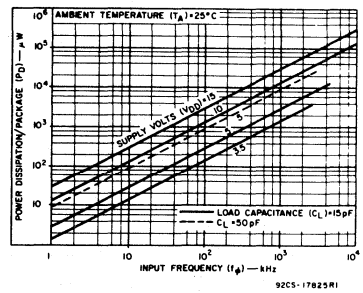


Fig. 6 – Typical dissipation characteristics.

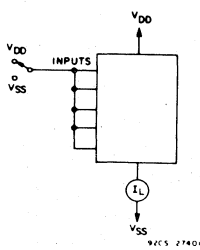


Fig. 7 – Quiescent device current test circuit.

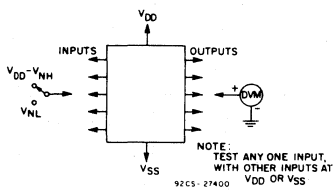


Fig. 8 – Noise immunity test circuit.

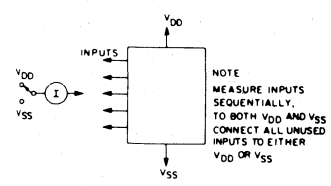


Fig. 9 – Input leakage current test circuit.

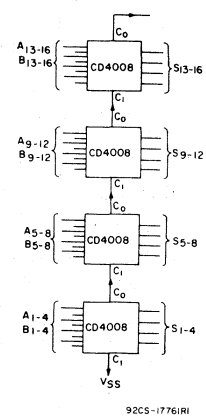
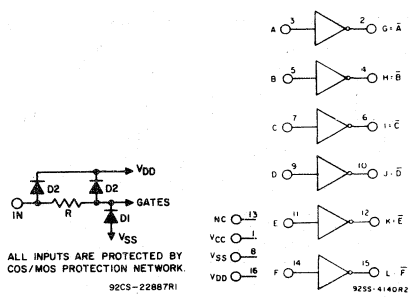


Fig. 10 – Typical connection for a 16-bit adder.

COS/MOS
Hex Buffers/Converters

Inverting Type: CD4009A
Non-Inverting Type: CD4010A

The RCA-CD4009A and CD4010A Hex Buffer/Converters may be used as COS/MOS to TTL or DTL logic-level converters or COS/MOS high sink-current drivers.
The CD4049A and CD4050A are preferred hex buffer replacements for the CD4009A and CD4010A, respectively, in all applications except multiplexers. For applications not requiring high sink current or voltage conversion, the CD4069B Hex Inverter is recommended.
These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).



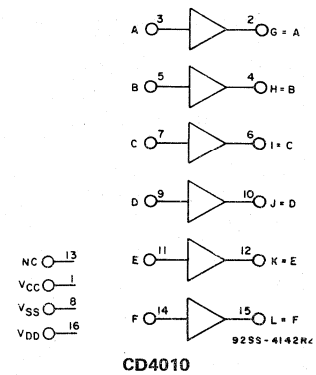


Fig. 1 — Logic diagrams.

Features:

- **Quiescent current specified to 15 V**
- **Maximum input leakage of 1 μA at 15 V (full package-temperature range)**
- **High sink current for driving 2 TTL loads**
- **High-to-low level logic conversion**

Applications:

- **COS/MOS to DTL/TTL hex converter**
- **COS/MOS current "sink" or "source" driver**
- **COS/MOS high-to-low logic-level converter**
- **Multiplexer — 1 to 6 or 6 to 1**

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range : V_{DD} , V_{CC})	3	12	V
Input Voltage Range (V_I)	V_{CC}*	12	V

* The CD4009 and CD4010 have high-to-low level voltage conversion capability but not low-to-high level, therefore it is recommended that $V_{DD} \geqslant V_I \geqslant V_{CC}$.

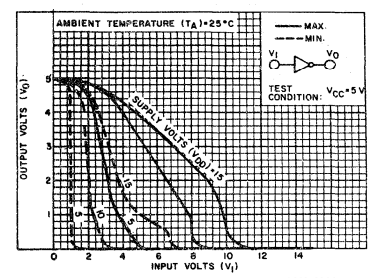


Fig. 2 — Minimum & maximum voltage transfer characteristics — CD4009A.

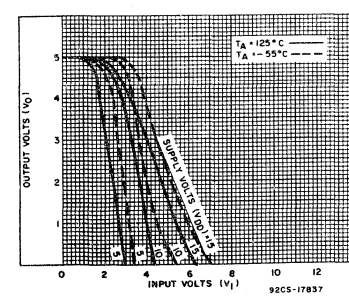


Fig. 3 — Typical voltage transfer characteristics as function of temp. — CD4009A.

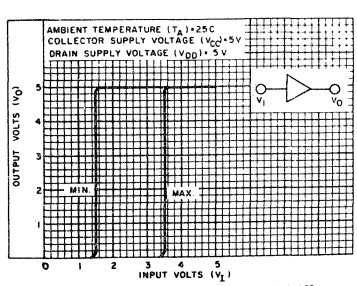


Fig. 4 — Minimum & maximum voltage transfer characteristics (V_{DD} = 5) — CD4010A.

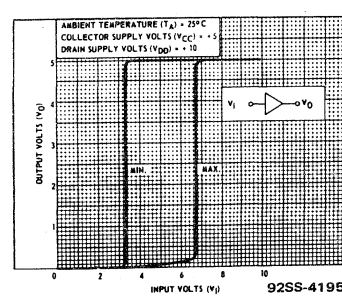


Fig. 5 — Minimum & maximum voltage transfer characteristics (V_{DD} = 10) — CD4010A.

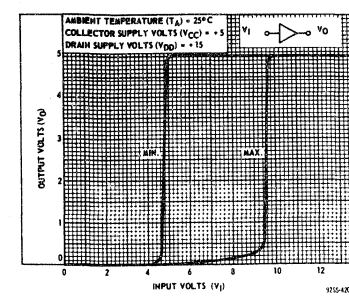


Fig. 6 — Minimum & maximum voltage transfer characteristics (V_{DD} = 15) — CD4010A.

CD4009A, CD4010A Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				E Package				
	V_O (V)	V_{IN} (V)	V_{CC}* (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	0.3	0.01	0.3	20	3	0.03	3	42	μA
	–	–	10	0.5	0.01	0.5	30	5	0.05	5	70	
	–	–	15	10	0.02	10	100	50	0.5	50	500	
Output Voltage: Low-Level, V_{OL}	–	0,5	5	0 Typ.; 0.05 Max.								V
	–	0,10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0,5	5	4.95 Min.; 5 Typ.								
	–	0,10	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	3.6	–	5	1.5 Min.; 2.25 Typ.								V
CD4010A	7.2	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH} All Types	1.4	–	5	1.5 Min.; 2.25 Typ.								
	2.8	–	10	3 Min.; 4.5 Typ.								
Inputs Low, V_{NL}	3.6	–	5	1 Min.; 1.5 Typ.								
CD4009A	7.2	–	10	2 Min.; 3 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
CD4010A	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
CD4010A	1	–	10	1 Min.								
Output Drive Current : N-Channel (Sink), I_DN Min.	0.4	–	5	3.75	4	3	2.1	3.6	4	3	2.4	mA
	0.5	–	10	10	10	8	5.6	9.6	10	8	6.4	
P-Channel (Source), I_DP Min.	4.6	–	5	-0.31	-0.5	-0.25	-0.175	-0.3	-0.5	-0.25	-0.2	
	2.5	–	5	-1.85	-1.75	-1.25	-0.9	-1.5	-1.75	-1.25	-1	
	9.5	–	10	-0.9	-0.8	-0.6	-0.4	-0.72	-0.8	-0.6	-0.48	
Input Leakage Current, I_{IL},I_{IH}	Any Input		15	$\pm 10^{-5}$ Typ.; ±1 Max.								μA

* $V_{CC} = V_{DD}$

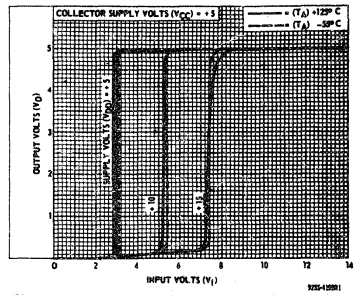


Fig. 7 — Typical voltage transfer characteristics as a function of temperature — CD4010A.

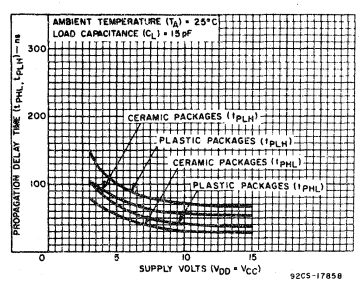


Fig. 8 — Maximum propagation delay time vs. V_{DD} — CD4010A.

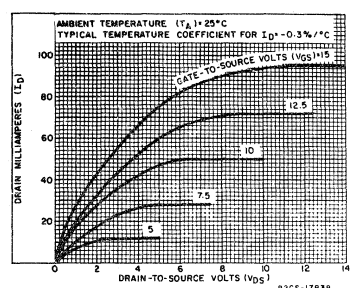


Fig. 9 — Typical n-channel drain characteristics,

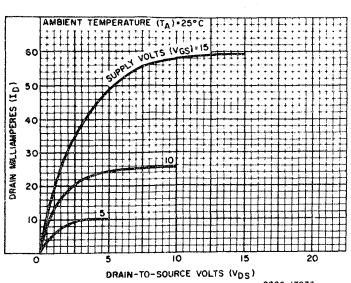


Fig. 10 — Minimum n-channel drain characteristics.

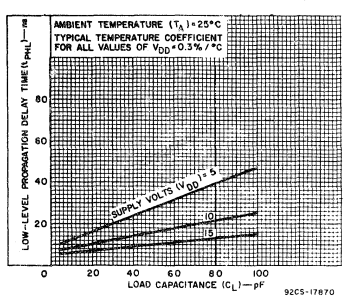


Fig. 11 — Typical high-to-low level propagation delay time vs. C_L.

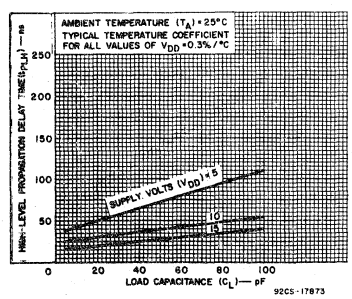


Fig. 12 — Typical low-to-high level propagation delay time vs. C_L.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 KΩ

CHARACTERISTIC	CONDITION			LIMIT		UNITS
	V_{DD} (V)	V_I (V)	V_{CC} (V)	Typ.	Max.	
D, F, K, H Packages						
Propagation Delay Time: Low-to-High, t_{PLH}	5	5	5	50	80	ns
	10	10	10	25	55	
	10	10	5	15	30	
High-to-Low, t_{PHL}	5	5	5	15	55	
	10	10	10	10	30	
	10	10	5	10	25	
Transition Time: Low-to-High, t_{TLH}	5	5	5	80	125	ns
	10	10	10	50	100	
High-to-Low, t_{THL}	5	5	5	20	45	
	10	10	10	16	40	
Input Capacitance, C_I CD4009	–	–	–	15	–	pF
CD4010	–	–	–	5	–	
E Package						
Propagation Delay Time: Low-to–high, t_{PLH}	5	5	5	50	100	ns
	10	10	10	25	70	
	10	10	5	15	40	
High-to-Low, t_{PHL}	5	5	5	15	70	
	10	10	10	10	40	
	10	10	5	10	35	
Transition Time: Low-to-High, t_{PLH}	5	5	5	80	160	ns
	10	10	10	50	120	
High-to-Low, t_{THL}	5	5	5	20	60	
	10	10	10	16	50	
Input Capacitance, C_I CD4009	–	–	–	15	–	pF
CD4010	–	–	–	5	–	

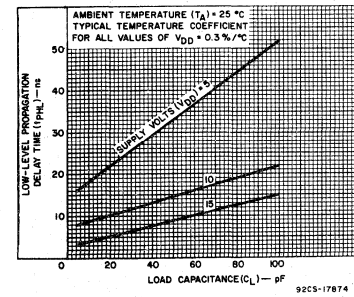


Fig. 13 – Typical high-to-low level propagation delay time vs. C_L (driving TTL, DTL).

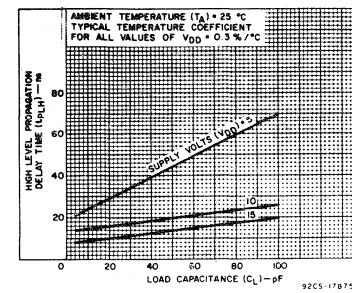


Fig. 14 – Typical low-to-high level propagation delay time vs. C_L (driving TTL, DTL)

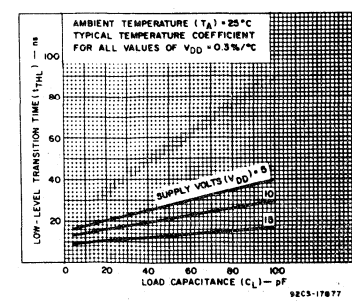


Fig. 15 – Typical high-to-low level transition time vs. C_L.

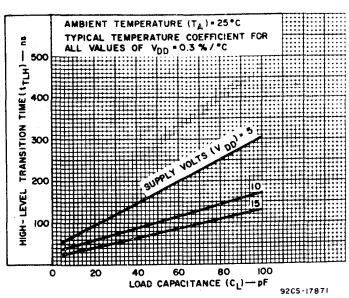


Fig. 16 – Typical low-to-high level transition time vs. C_L.

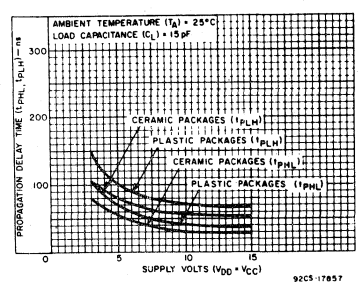


Fig. 17 – Maximum propagation delay time vs. V_{DD} – CD4009A.

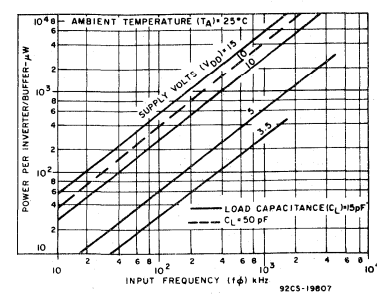


Fig. 18 – Typical dissipation characteristics.

COS/MOS NAND Gates

Quad 2 Input – CD4011A
Dual 4 Input – CD4012A
Triple 3 Input – CD4023A

The RCA-CD4011A, CD4012A, and CD-4023A NAND gates provide the system designer with direct implementation of the NAND function and supplement the existing family of COS/MOS gates.

These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- **Quiescent current specified to 15 V**
- **Maximum input leakage of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

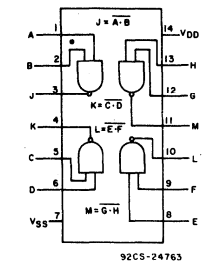
RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

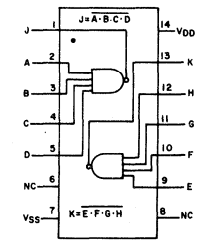
Characteristic	Min.	Max.	Units
Supply Voltage Range (over full package temperature range)	3	12	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

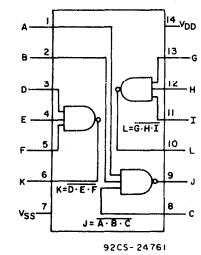
STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
PACKAGE TYPE E . . . . . –40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): . . . . . –0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):
FOR T_A = –40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = –55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max . . . . . +265°C



CD4011A

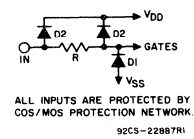


CD4012A



CD4023AH

Fig. 1 – Functional diagrams.



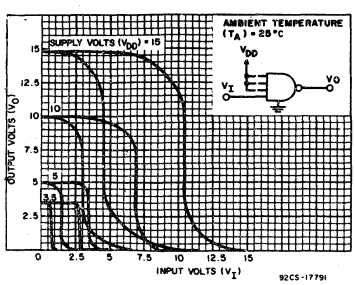


Fig. 2 – Minimum & maximum voltage transfer characteristics.

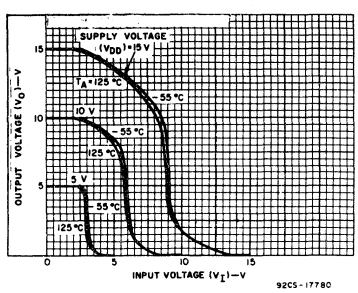


Fig. 3 – Typical voltage transfer characteristics as a function of temperature.

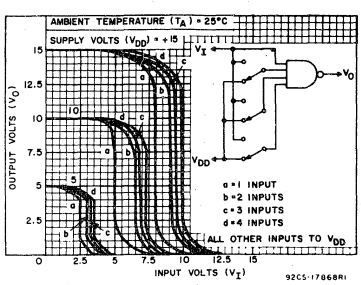


Fig. 4 – Typical multiple input switching transfer characteristics for CD4012A.

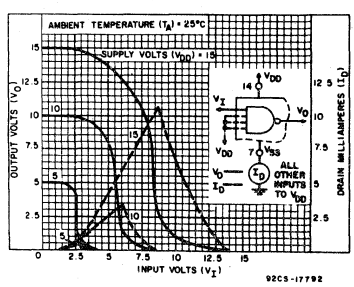


Fig. 5 – Typical current & voltage transfer characteristics.

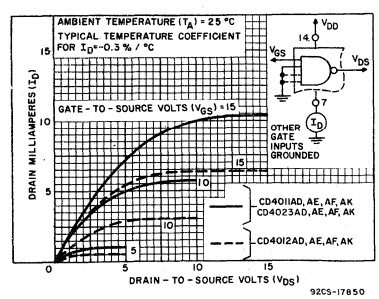


Fig. 6 – Typical n-channel drain characteristics.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				E Package				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	0.05	0.001	0.05	3	0.5	0.005	0.5	15	μA
	–	–	10	0.1	0.001	0.1	6	5	0.005	5	30	
	–	–	15	2	0.02	2	40	50	0.5	50	500	
Output Voltage: Low-Level V_{OL}	–	0,5	5	0 Typ.; 0.05 Max.								V
	–	0,10	10	0 Typ.; 0.05 Max.								
High Level, V_{OH}	–	0,5	5	4.95 Min.; 5 Typ.								
	–	0,10	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	3.6	–	5	1.5 Min.; 2.25 Typ.								V
	7.2	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}	1.4	–	5	1.5 Min.; 2.25 Typ.;								
	2.8	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink) I_DN Min. CD4011A	0.5	–	5	0.31	0.5	0.25	0.175	0.145	0.5	0.12	0.095	mA
CD4023A	0.5	–	10	0.62	0.6	0.5	0.35	0.3	0.6	0.25	0.2	
CD4012A	0.5	–	5	0.15	0.25	0.12	0.085	0.072	0.25	0.06	0.05	
	0.5	–	10	0.31	0.6	0.25	0.175	0.155	0.6	0.13	0.105	
P-Channel (Source), I_DP Min. All Types	4.5	–	5	-0.31	-0.5	-0.25	-0.175	-0.145	-0.5	-0.12	-0.095	
	9.5	–	10	-0.75	-1.2	-0.6	-0.4	-0.35	-1.2	-0.3	-0.24	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		15	$\pm 10^{-5}$ Typ.; ±1 Max.								μA

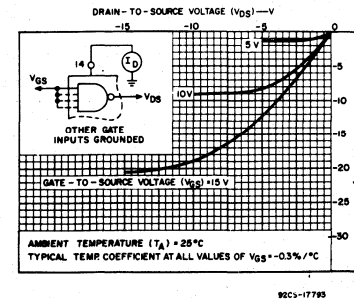


Fig. 7 — Typical p-channel drain characteristics.

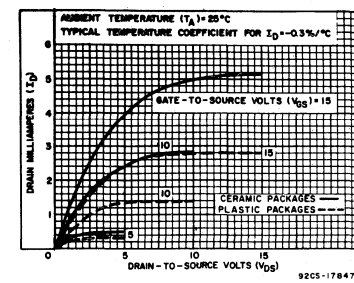


Fig. 8 — Minimum n-channel drain characteristics —CD4011A & CD4023A.

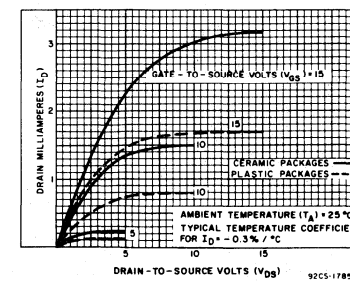


Fig. 9 — Typical n-channel drain characteristics.

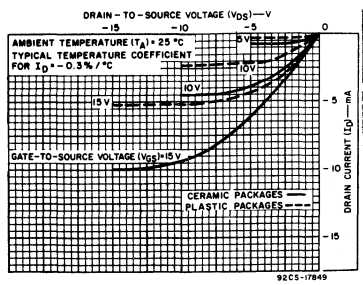


Fig. 10 — Minimum p-channel drain characteristics.

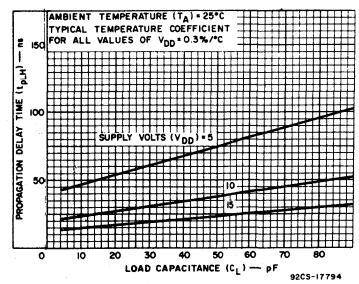


Fig. 11 — Typical low-to-high level propagation delay time vs. C_L.

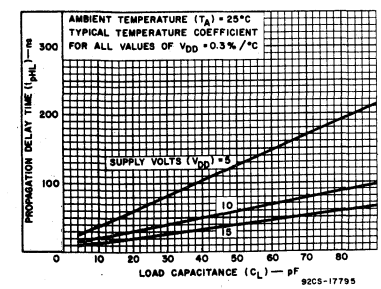


Fig. 12 — Typical high-to-low level propagation delay time vs. C_L — CD4011A, & CD4023A.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 15 pF, Input t_r, t_f = 20 ns, R_L = 200 KΩ

CHARACTERISTICS	TEST CONDITIONS		LIMITS				UNITS
			D,F,K,H Packages		E Package		
		V_{DD} (V)	Typ.	Max.	Typ.	Max.	
Propagation Delay Time: Low-to-High Level, t_{PLH}		5	50	75	50	100	ns
		10	25	40	25	50	
High-to-Low Level, t_{PHL} CD4011A and CD4023A		5	50	75	50	100	ns
		10	25	40	25	50	
CD4012A		5	100	150	100	200	ns
		10	50	75	50	100	
Transition Time: Low-to-High Level, t_{TLH}		5	75	100	75	125	ns
		10	40	60	40	75	
High-to-Low Level, t_{THL} CD4011A and CD4023A		5	75	125	75	150	ns
		10	50	75	50	100	
CD4012A		5	250	375	250	500	ns
		10	125	200	125	250	
Input Capacitance, C_I	Any Input		5	–	5	–	pF

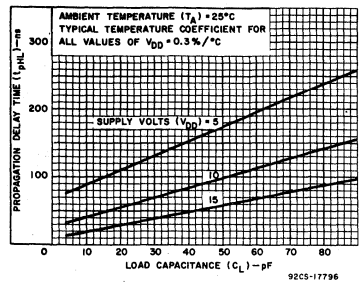


Fig. 13 – Typical high-to-low level propagation delay time vs. C_L – CD4012A.

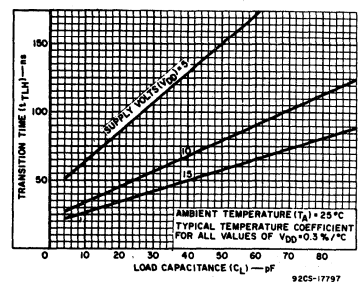


Fig. 14 – Typical low-to-high transition time vs. C_L.

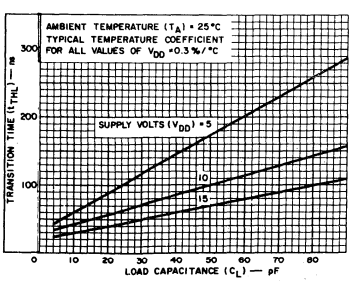


Fig. 15 – Typical high-to-low level transition time vs. C_L – CD4011A & CD4023A.

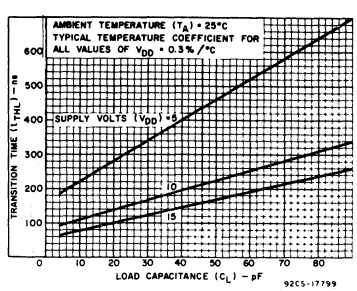


Fig. 16 – Typical high-to-low level transition time vs. C_L – CD4012A.

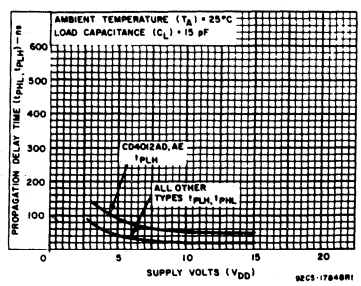


Fig. 17 – Minimum propagation delay time vs. V_{DD}.

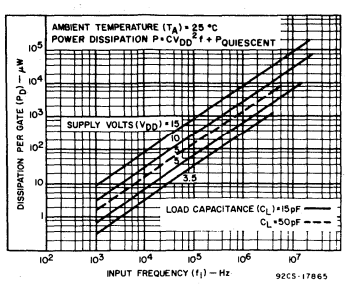


Fig. 18 – Typical dissipation characteristics.

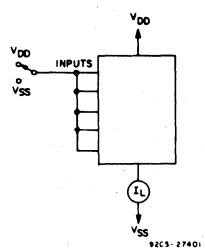


Fig. 19 – Quiescent device current test circuit.

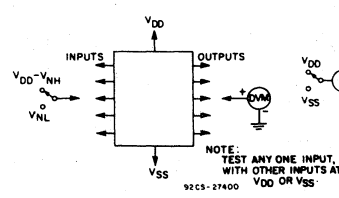


Fig. 20 – Noise immunity test circuit.

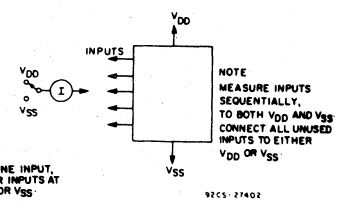


Fig. 21 – Input leakage current test circuit.

Dual 'D'-Type Flip-Flop

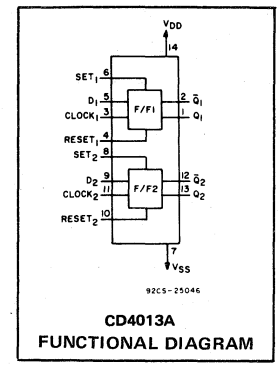
The RCA-CD4013A consists of two identical, independent data-type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs, and Q and $\overline{Q}$ outputs. These devices can be used for shift register applications, and by connecting $\overline{Q}$ output to the data input, for counter and toggle applications. The logic level present at the D input is transferred to the Q output during the positive-going transition of the clock pulse.

Setting or resetting is independent of the clock and is accomplished by a high level on the set (with low-level on reset) or reset (with low-level on set) line, respectively.

These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg})	−65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):	
FOR T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K)	500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C



CD4013A
FUNCTIONAL DIAGRAM

Features:

- **Set-Reset capability**
- **Static flip-flop operation — retains state indefinitely with clock level either "high" or "low"**
- **Medium-speed operation — 10 MHz (typ.) clock toggle rate at 10 V**
- **Quiescent current specified to 15 V**
- **Maximum input leakage of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Registers, counters, control circuits**

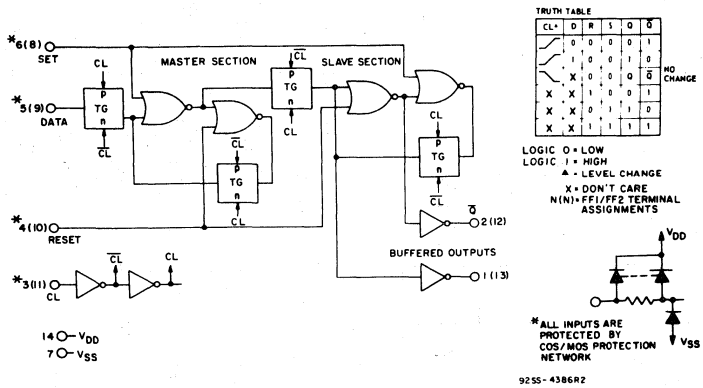


Fig. 1 — Logic diagram and truth table for CD4013A (one of two identical flip flops).

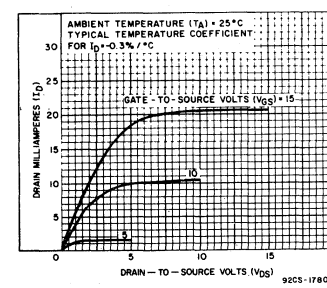


Fig.2 — Typical n-channel drain characteristics.

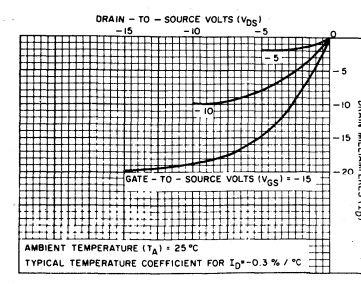


Fig.3 — Typical p-channel drain characteristics.

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges –

CHARACTERISTIC	V_{DD} (V)	LIMITS D,F,K,H Packages Min.	D,F,K,H Packages Max.	LIMITS E Package Min.	E Package Max.	UNITS
Supply-Voltage Range (For T_A = Full Package Temperature Range)	–	3	12	3	12	V
Data Setup Time t_S	5	40	–	50	–	ns
	10	20	–	25	–	
Clock Pulse Width t_W	5	200	–	500	–	ns
	10	80	–	100	–	
Clock Input Frequency f_{CL}	5		2.5		1	MHz
	10	dc	7	dc	5	
Clock Rise or Fall Time t_rCL^*, t_fCL	5	–	15	–	15	μs
	10	–	5	–	5	
Set or Reset Pulse Width	5	250	–	500	–	ns
	10	100	–	125	–	

* If more than one unit is cascaded in a parallel clocked operation, t_rCL should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

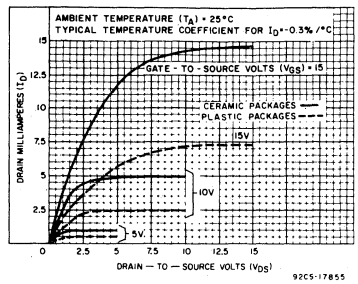


Fig.4 – Minimum n-channel drain characteristics.

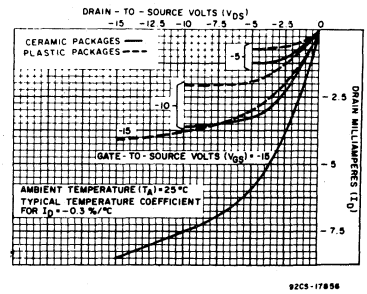


Fig.5 – Minimum p-channel drain characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS D,F,K,H Packages Min.	D,F,K,H Packages Typ.	D,F,K,H Packages Max.	LIMITS E Package Min.	E Package Typ.	E Package Max.	UNITS
Propagation Delay Time: Clock to Q or $\overline{Q}$ Outputs t_{PHL}, t_{PLH}	5	–	150	300	–	150	350	ns
	10	–	75	110	–	75	125	
Set to Q or Reset to $\overline{Q}$ t_{PLH}	5	–	175	300	–	175	350	ns
	10	–	75	110	–	75	125	
Set to $\overline{Q}$ or Reset to Q t_{PHL}	5	–	175	300	–	175	350	ns
	10	–	75	110	–	75	125	
Transition Time, t_{THL}, t_{TLH}	5	–	75	125	–	75	150	ns
	10	–	50	70	–	50	75	
Maximum Clock Input Frequency, f_{CL}	5	2.5	4	–	1	4	–	MHz
	10	7	10	–	5	10	–	
Minimum Clock Pulse Width, t_W	5	–	125	200	–	125	500	ns
	10	–	50	80	–	50	100	
Minimum Set or Reset Pulse Width, t_W	5	–	125	250	–	125	500	ns
	10	–	50	100	–	50	125	
Minimum Data Setup Time, t_S	5	–	20	40	–	20	50	ns
	10	–	10	20	–	10	25	
Clock Rise or Fall Time t_rCL, t_fCL	5	–	–	15	–	–	15	μs
	10	–	–	5	–	–	5	
Average Input Capacitance, C_I	Any Input	–	5	–	–	5	–	pF

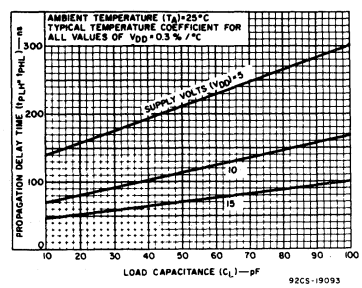


Fig.6 – Typical propagation delay time vs. C_L.

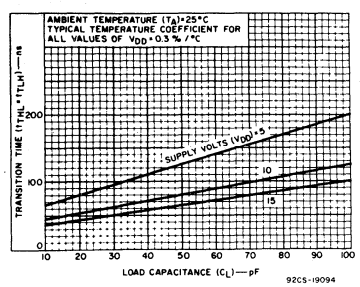


Fig.7 – Typical transition time vs. C_L.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				E Package				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	1	0.005	1	60	10	0.01	10	140	μA
	–	–	10	2	0.005	2	120	20	0.02	20	280	
	–	–	15	25	0.5	25	1000	250	2.5	250	2500	
Output Voltage: Low-Level, V_{OL}	–	0.5	5	0 Typ.; 0.05 Max.								V
	–	0.10	10	0 Typ.; 0.05 Max.								
High-Level V_{OH}	–	0.5	5	5 Typ.; 4.95 Min.								
	–	0.10	10	10 Typ.; 9.95 Min.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	2.25 Typ.; 1.5 Min.								V
	9	–	10	4.5 Typ.; 3 Min.								
Inputs High V_{NH}	0.8	–	5	2.25 Typ.; 1.5 Min.								
	1	–	10	4.5 Typ.; 3 Min.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink) I_{DN} Min.	0.5	–	5	0.65	1	0.5	0.35	0.35	1	0.3	0.24	mA
	0.5	–	10	1.25	2.5	1	0.75	0.72	2.5	0.6	0.5	
P-Channel (Source) I_{DP} Min.	4.5	–	5	−0.31	−0.5	−0.25	−0.175	−0.17	−0.5	−0.14	−0.12	
	9.5	–	10	−0.8	−1.3	−0.65	−0.45	−0.4	−1.3	−0.33	−0.27	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		15	$\pm 10^{-5}$ Typ.; ±1 Max.								μA

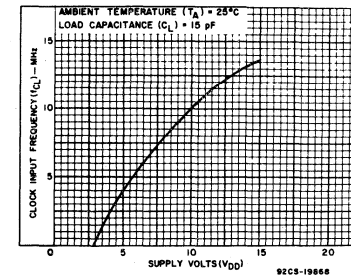


Fig.8 – Typical maximum clock input frequency vs. V_{DD}.

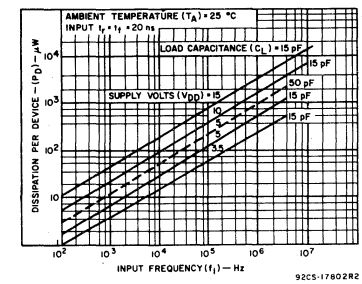


Fig.9 – Typical dissipation characteristics.

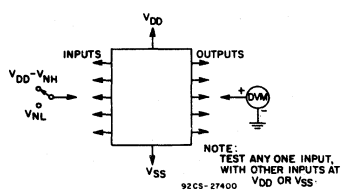


Fig.10 – Noise immunity test circuit.

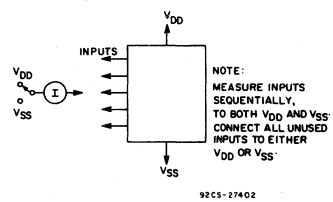


Fig.11 – Input leakage test circuit.

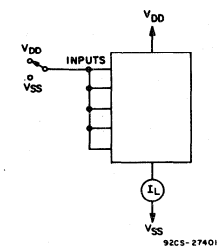


Fig.12 – Quiescent device-current test circuit.

COS/MOS 8-Stage Static Shift Register

Synchronous Parallel or Serial Input/Serial Output

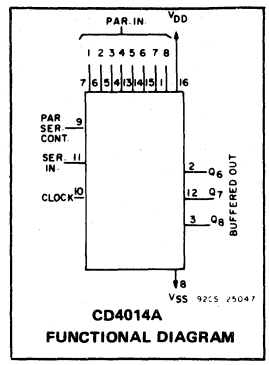
RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D,F,K,H Packages		*E Package*		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A= Full Package-Temperature Range)		3	12	3	12	V
Data Setup Time, t_S	5	350	–	500	–	ns
	10	80	–	100	–	
Clock Pulse Width, t_W	5	500	–	830	–	ns
	10	175	–	200	–	
Clock Input Frequency, f_{CL}	5	dc	1	dc	0.6	MHz
	10	dc	3	dc	2.5	
Clock Rise and Fall Time, t_rCL, t_fCL*	5	–	15	–	15	μs
	10	–	15	–	15	

* If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				*E Package*				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	+25 Typ.	+25 Limit	+125	–40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current I_L Max.	–	–	5	5	0.5	5	300	50	0.5	50	700	μA
	–	–	10	10	1	10	600	100	1	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min., 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min., 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: n-Channel (Sink), I_DN Min.	0.5	–	5	0.15	0.3	0.12	0.085	0.072	0.3	0.06	0.05	mA
	0.5	–	10	0.31	0.5	0.25	0.175	0.12	0.5	0.1	0.08	
p-Channel (Source): I_DP Min.	4.5	–	5	-0.1	-0.16	-0.08	-0.055	-0.06	-0.16	-0.05	-0.04	
	9.5	–	10	-0.25	-0.44	-0.20	-0.14	-0.12	-0.44	-0.1	-0.08	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		15	$\pm 10^{-5}$ Typ.; ±1 Max.								μA



CD4014A
FUNCTIONAL DIAGRAM

The RCA-CD4014A types are 8-stage parallel-input/serial output registers having common CLOCK and PARALLEL/SERIAL CONTROL INPUTS, a single SERIAL DATA INPUT, and individual parallel "JAM" INPUTS to each register stage. Each register stage is a D-type, master-slave flip-flop. In addition to an output from stage 8, "Q" outputs are also available from stages 6 and 7. Parallel as well as serial entry is made into the register synchronous with the positive clock line transition and under control of the PARALLEL/SERIAL CONTROL input. When the PARALLEL/SERIAL CONTROL input is low, data is serially shifted into the 8-stage register synchronously with the positive transition of the clock line. When the PARALLEL/SERIAL CONTROL input is high, data is jammed into the 8-stage register via the parallel input lines and synchronous with the positive transition of the clock line. Register expansion using multiple CD4014A packages is permitted.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

CL▲	SER. IN	PAR SER CONTROL	PI-1	PI-n	Q_1 (INTERNAL)	Q_n	
⌐	X	1	0	0	0	0	
⌐	X	1	1	0	1	0	
⌐	X	1	0	1	0	1	
⌐	X	1	1	1	1	1	
⌐	0	0	X	X	0	Q_n-1	
⌐	1	0	X	X	1	Q_n-1	
⌙	X	X	X	X	Q_1	Q_n	NC

X = DON'T CARE CASE ▲ = LEVEL CHANGE
NC = NO CHANGE

Fig. 1 – Truth table.

Features:

- Medium speed operation. . . . . 5 MHz (typ.) clock rate at $V_{DD} - V_{SS} = 10$ V
- Fully static operation
- 8 master-slave flip-flops plus output buffering and control gating
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications:

- Synchronous parallel input/serial output data queueing
- Parallel to serial data conversion
- General-purpose register

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, Input t_r, $t_f = 20$ ns, $C_L = 15$ pF, $R_L = 200$ kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
			D,F,K,H Packages			*E Package*			
		V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
Propagation Delay Time; t_{PLH}, t_{PHL}		5	–	300	750	–	300	1000	ns
		10	–	100	225	–	100	300	
Transition Time; t_{THL}, t_{TLH}		5	–	150	300	–	150	400	ns
		10	–	75	125	–	75	150	
Maximum Clock Input Frequency, f_{CL}		5	1	2.5	–	0.6	2.5	–	MHz
		10	3	5	–	2.5	5	–	
Minimum Clock Pulse Width, t_W		5	–	200	500	–	200	830	ns
		10	–	100	175	–	100	200	
Clock Rise & Fall Time; t_rCL, t_fCL*		5	–	–	15	–	–	15	μs
		10	–	–	15	–	–	15	
Minimum Data Set Up Time, t_S		5	–	100	350	–	100	500	ns
		10	–	50	80	–	50	100	
Average Input Capacitance, C_I	Any Input		–	5	–	–	5	–	pF

* If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

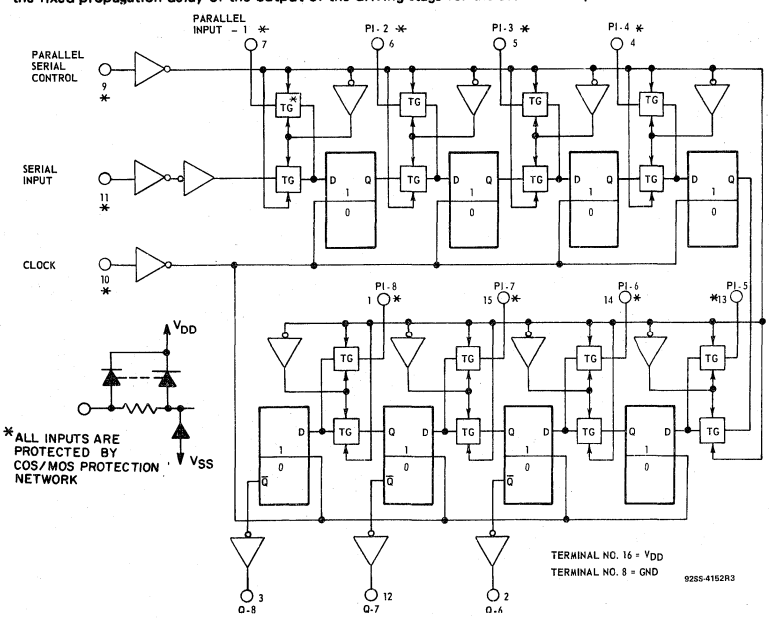


Fig. 5 – Logic block diagram.

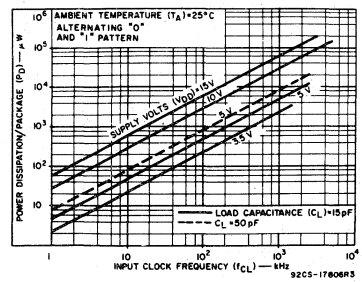


Fig. 2 – Typical dissipation characteristics.

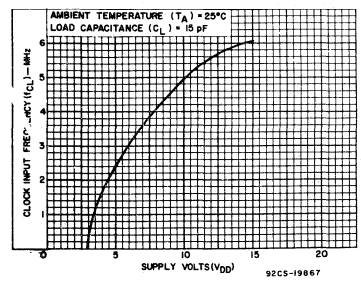


Fig. 3 – Typical clock input frequency vs. supply voltage.

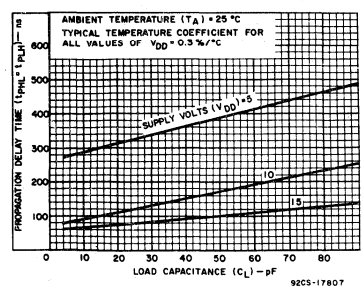


Fig. 4 – Typical propagation delay time vs. load capacitance.

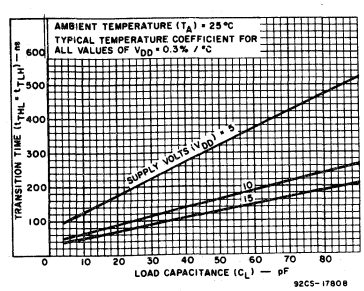


Fig. 6 – Typical transition time vs. load capacitance.

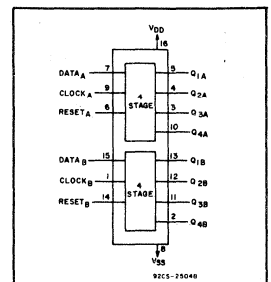
COS/MOS Dual 4-Stage Static Shift Register

With Serial Input/Parallel Output

The RCA-CD4015A consists of two identical, independent, 4-stage serial-input/parallel-output registers. Each register has independent CLOCK and RESET inputs as well as a single serial DATA input. "Q" outputs are available from each of the four stages on both registers. All register stages are D-type, master-slave flip-flops. The logic level present at the DATA input is transferred into the first register stage and shifted over one stage at each positive-going clock transition.

Resetting of all stages is accomplished by a high level on the reset line. Register expansion to 8 stages using one CD4015A package, or to more than 8 stages using additional CD4015A's is possible.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).



CD4015A
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . -65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H. . . . . -55 to +125°C

PACKAGE TYPE E . . . . . -40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal). . . . . -0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D)

FOR T_A = -40 to + 60°C (PACKAGE TYPE E) . . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12mW/°C to 200 mW

FOR T_A = -55 to + 100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW

FOR T_A = + 100 to +125°C (PACKAGE TYPES D, F, K) . . . .Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES). . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . -0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS *at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:*

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, K, H PACKAGES		E PACKAGE		
		MIN.	MAX.	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Data Setup Time, t_S	5 10	350 80	– –	500 100	– –	ns
Clock Pulse Width, t_W	5 10	500 175	– –	830 200	– –	ns
Clock Input Frequency, f_{CL}	5 10	dc dc	1 3	dc dc	0.6 2.5	MHz
Clock Rise and Fall Time, t_rCL, t_fCL*	5 10	– –	15 15	– –	15 15	μs
Clock Reset Pulse Width, t_W	5 10	500 175	– –	830 200	– –	ns

*If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

Features:

- **Medium speed operation. . . . . 5 MHz (typ.) clock rate at $V_{DD} - V_{SS}$ = 10V**
- **Fully static operation**
- **8 master-slave flip-flops plus output buffering**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Serial-input/parallel-output data queueing**
- **Serial to parallel data conversion**
- **General-purpose register**

TRUTH TABLE

CL▲	D	R	Q_1	Q_n	
⌐⌐	0	0	0	Q_{n-1}	
⌐⌐	1	0	1	Q_{n-1}	
⌐⌐	X	0	Q_1	Q_n	(NO CHANGE)
X	X	1	0	0	

▲= LEVEL CHANGE
X = DON'T CARE CASE

Fig. 1 – Truth table.

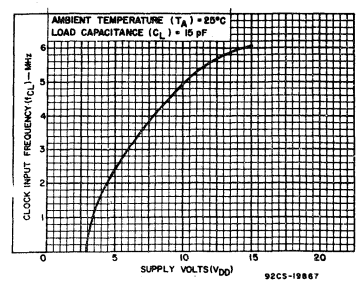


Fig. 2 – Typical clock input frequency vs. supply voltage.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
				D, K, F, H PACKAGES				E PACKAGE				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	+25 TYP.	+25 LIMIT	+125	-40	+25 TYP.	+25 LIMIT	+85	
Quiescent Device Current, I_L Max.	–	–	5	5	0.5	5	300	50	0.5	50	700	μA
	–	–	10	10	1	10	600	100	1	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max								V
	–	10	10	0 Typ.; 0.05 Max								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink),	0.5	–	5	0.15	0.3	0.12	0.085	0.072	0.3	0.06	0.05	mA
I_DN Min.	0.5	–	10	0.31	0.5	0.25	0.175	0.12	0.5	0.1	0.08	
P-Channel (Source):	4.5	–	5	-0.1	-0.16	-0.08	-0.055	-0.06	-0.16	-0.05	-0.04	
I_DP Min.	9.5	–	10	-0.25	-0.44	-0.20	-0.14	-0.12	-0.44	-0.1	-0.08	
Input Leakage Current,	Any Input											μA
I_{IL}, I_{IH}	–	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								

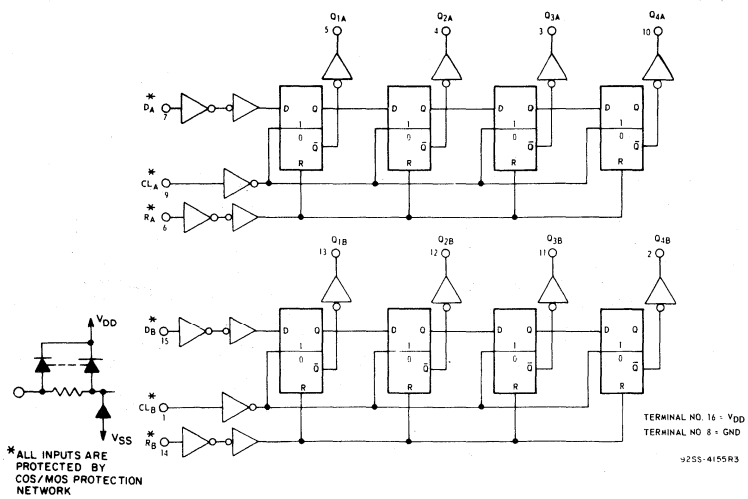


Fig. 6 – Logic diagram.

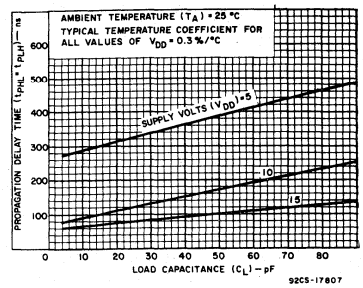


Fig. 3 – Typical propagation-delay time vs. load capacitance.

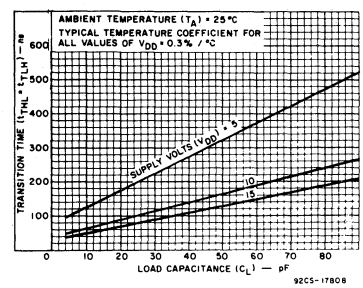


Fig. 4 – Typical transition time vs load capacitance.

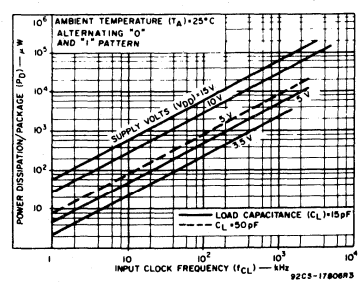


Fig. 5 – Typical dissipation characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS
at $T_A = 25°C$, Input t_r, $t_f = 20$ ns, $C_L = 15$ pF, $R_L = 200$ kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		D, F, K, H PACKAGES			E PACKAGE			
	V_{DD} (V)	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
CLOCKED OPERATION								
Propagation Delay Time; T_{PLH}, T_{PHL}	5	–	300	750	–	300	1000	ns
	10	–	100	225	–	100	300	
Transition Time; t_{THL}, t_{TLH}	5	–	150	300	–	150	400	ns
	10	–	75	125	–	75	150	
Minimum Clock Pulse Width, t_W	5	–	200	500	–	200	830	ns
	10	–	100	175	–	100	200	
Clock Rise & Fall Time; t_rCL, t_fCL*	5	–	–	15	–	–	15	μs
	10	–	–	15	–	–	15	
Minimum Data Set-up Time, t_S	5	–	100	350	–	100	500	ns
	10	–	50	80	–	50	100	
Maximum Clock Input Frequency, f_{CL}	5	1	2.5	–	0.6	2.5	–	MHz
	10	3	5	–	2.5	5	–	
Average Input Capacitance, C_I		–	5	–	–	5	–	pF
RESET OPERATION								
Propagation Delay Time, T_{PLH}, T_{PHL}	5	–	300	750	–	300	1000	ns
	10	–	100	225	–	100	300	
Minimum Reset Pulse Width t_W	5	–	200	500	–	200	830	ns
	10	–	100	175	–	100	200	

*If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitve load.

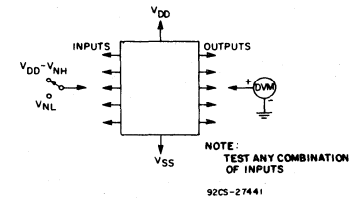


Fig. 7 – Noise-immunity test circuit.

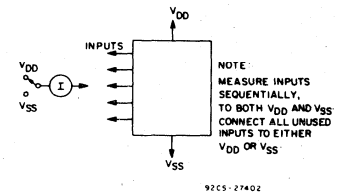
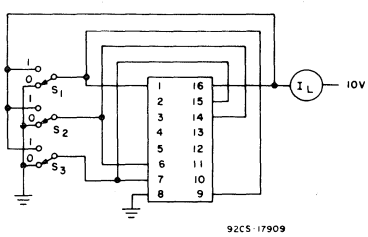


Fig. 8 – Input-leakage-current test circuit.

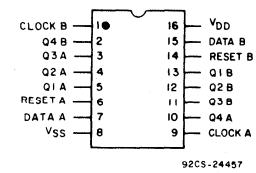


Test performed with the following sequence of "1's" and "0's"

	S_1	S_2	S_3
Test	0	1	0
Don't Test	0	0	1
Don't Test	1	0	1
Don't Test	0	0	0
Don't Test	1	0	0
Don't Test	0	0	1
Test	1	0	1
Don't Test	0	0	0
Test	1	0	0

Fig. 9 – Quiescent-device-current test circuit.

TERMINAL DIAGRAM
Top View



COS/MOS Quad Bilateral Switch

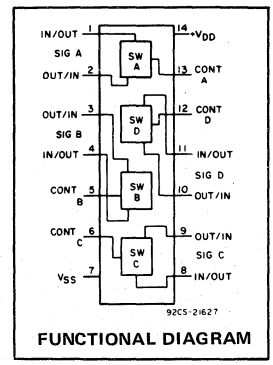
For Transmission or Multiplexing of Analog or Digital Signals

The RCA-CD4016A Series types are quad bilateral switches intended for the transmission or multiplexing of analog or digital signals. Each of the four independent bilateral switches has a single control signal input which simultaneously biases both the p and n device in a given switch ON or OFF.

These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- **15-V digital or ± 7.5-V peak-to-peak switching**
- **280-Ω typical ON resistance for 15-V operation**
- **Switch ON resistance matched to within 10 Ω typ. over 15-V signal-input range**
- **High ON/OFF output-voltage ratio: 65 dB typ. @ f_{is} = 10 kHz, R_L = 10 kΩ**
- **High degree of linearity: <0.5% distortion typ. @ f_{is} = 1 kHz, V_{is} = 5 V_{p-p}, $V_{DD}-V_{SS} \geq$ 10 V, R_L = 10 kΩ**
- **Extremely low OFF switch leakage resulting in very low offset current and high effective OFF resistance: 100 pA typ. @ $V_{DD}-V_{SS}$ = 10 V, T_A = 25°C**
- **Extremely high control input impedance (control circuit isolated from signal circuit: 10^{12} Ω typ.**
- **Low crosstalk between switches: −50 dB typ. @ f_{is} = 0.9 MHz, R_L = 1 kΩ**
- **Matched control-input to signal-output capacitance: Reduces output signal transients**
- **Frequency response, switch ON = 40 MHz (typ.)**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**



FUNCTIONAL DIAGRAM

Applications:

- **Analog signal switching/multiplexing**
  Signal gating ■ **Modulator**
  Squelch control ■ **Demodulator**
  Chopper ■ **Commutating switch**
- **Digital signal switching/multiplexing**
- **COS/MOS logic implementation**
- **Analog-to-digital & digital-to-analog conversion**
- **Digital control of frequency, impedance, phase, and analog-signal gain**

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply Voltage Range (For T_A = Full Package Temperature Range)	3	12	V

TYPICAL "ON" RESISTANCE CHARACTERISTICS

CHARACTERISTIC*	SUPPLY CONDITIONS		LOAD CONDITIONS					
			R_L = 1kΩ		R_L = 10kΩ		R_L = 100kΩ	
	V_{DD} (V)	V_{SS} (V)	VALUE (Ω)	V_{is} (V)	VALUE (Ω)	V_{is} (V)	VALUE (Ω)	V_{is} (V)
R_{ON}	+15	0	200	+15	200	+15	180	+15
			200	0	200	0	200	0
R_{ON}(max.)	+15	0	300	+11	300	+9.3	320	+9.2
R_{ON}	+10	0	290	+10	250	+10	240	+10
			290	0	250	0	300	0
R_{ON}(max.)	+10	0	500	+7.4	560	+5.6	610	+5.5
R_{ON}	+ 5	0	860	+ 5	470	+ 5	450	+ 5
			600	0	580	0	800	0
R_{ON}(max.)	+ 5	0	1.7k	+4.2	7k	+2.9	33k	+2.7
R_{ON}	+7.5	−7.5	200	+7.5	200	+7.5	180	+7.5
			200	−7.5	200	−7.5	180	−7.5
R_{ON}(max.)	+7.5	−7.5	290	±0.25	280	±25	400	±0.25
R_{ON}	+ 5	− 5	260	+ 5	250	+ 5	240	+ 5
			310	− 5	250	− 5	240	− 5
R_{ON}(max.)	+ 5	− 5	600	±0.25	580	±0.25	760	±0.25
R_{ON}	+2.5	−2.5	590	+2.5	450	+2.5	490	+2.5
			720	−2.5	520	−2.5	520	−2.5
R_{ON}(max.)	+2.5	−2.5	232k	±0.25	300k	±0.25	870k	±0.25

* Variation from a perfect switch, R_{ON} = 0Ω.

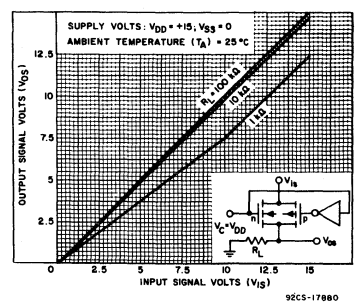


Fig. 1 — Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +15 V, V_{SS} = 0 V.

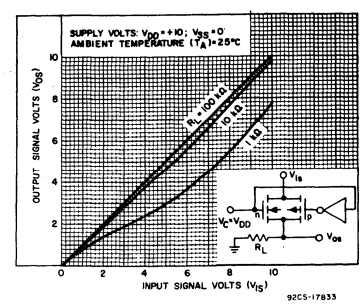


Fig. 2 — Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +10 V, V_{SS} = 0 V.

ELECTRICAL CHARACTERISTICS (All inputs. . . . . $V_{SS} \leq V_I \leq V_{DD}$)

Recommended DC Supply Voltage ($V_{DD}-V_{SS}$). .3 to 15 V)

Characteristic	Test Conditions (All Voltage Values are in Volts)			Limits (Values at −55°C,+25°C,+125°C Apply to D,F,K,H Packages; Values at −40°C,+25°C,+85°C Apply to E Package)						Unit
			V_{DD} (V)	−55°	−40°	+85°	+125°	+25°C Typ.	+25°C Max.	
Quiescent Device Current, I_L max (All switches ON or all Switches OFF) D,F,K,H Pkgs.			5	0.25	–	–	10	0.01	0.25	μA
			10	0.5	–	–	20	0.01	0.5	
			15	2	–	–	40	0.01	2	
E,Y Pkgs.			5	–	0.25	5	–	–	0.25	μA
			10	–	0.5	10	–	–	0.5	
			15	–	2	20	–	–	2	
Signal Inputs (V_{is}) and Outputs (V_{os})										
ON Resistance, R_{ON}	$V_C=V_{DD}$	V_{SS}	V_{is}	Typ/Max	Typ/Max	Typ/Max	Typ/Max			Ω
	R_L = 10 kΩ●									
	+7.5	−7.5	+7.5	120/360	130/370	260/520	300/600	200	400	
			−7.5	120/360	130/370	260/520	300/600	200	400	
			±0.25	130/775	160/790	400/1080	470/1230	280	850	
	+5	−5	+5	130/600	150/610	340/840	400/960	250	660	
			−5	130/600	150/610	340/840	400/960	250	660	
			±0.25	325/1870	370/1900	770/2380	900/2600	580	2000	
	+15	0	+15	120/360	130/370	260/520	300/600	200	400	
			+0.25	120/360	130/370	260/520	300/600	200	400	
			+9.3	150/775	180/790	400/1080	490/1230	300	850	
	+10	0	+10	130/600	150/610	340/840	400/960	250	660	
			+0.25	130/600	150/610	340/840	400/960	250	660	
			+5.6	300/1870	350/1900	750/2380	880/2600	560	2000	
ΔON Resistance Between Any 2 of 4 Switches ΔR_{ON}	R_L = 10 kΩ●									Ω
	+7.5	−7.5	±7.5	–	–	–	–	10	–	
	+5	−5	±5	–	–	–	–	15	–	
Sine Wave Response (Distortion)	+5	−5	5 p-p▲							%
	R_L = 10 kΩ, f_{is} = 1 kHz			–	–	–	–	0.4	–	
Frequency Response Switch ON (Sine-Wave Input)	V_{DD}=+5, V_C=V_{SS}=−5		−5 p-p							MHz
	R_L = 1 kΩ, $20 \log_{10} \frac{V_{os}}{V_{is}}$ = −3 dB			–	–	–	–	40	–	
Feedthrough Switch OFF	+5	−5	−5 p-p							MHz
	R_L = 1 kΩ, $20 \log_{10} \frac{V_{os}}{V_{is}}$ = −50 dB			–	–	–	–	1.25	–	
Input or Output Leakage Current Switch OFF (Effective OFF Resistance)	V_{DD}	V_C=V_{SS}	±7.5	–	–	–	–	±100	–	pA
	+7.5	−7.5								
	+5	−5	±5	–	–	–	–	$\pm 10 \times 10^{-3}$	±125*	nA

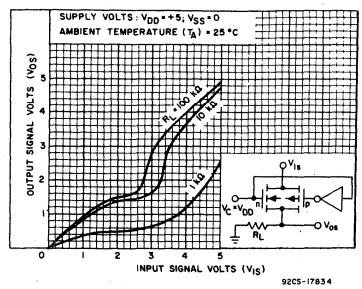


Fig. 3 — Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +5 V, V_{SS} = 0 V.

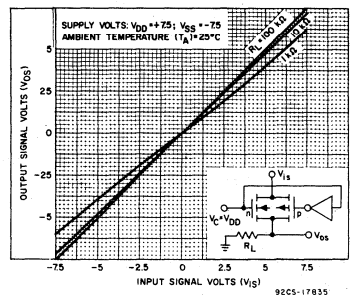


Fig. 4 — Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +7.5 V, V_{SS} = -7.5 V.

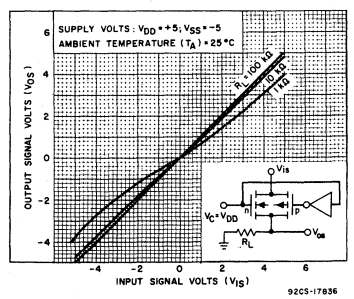


Fig. 5 — Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +5 V, V_{SS} = -5 V.

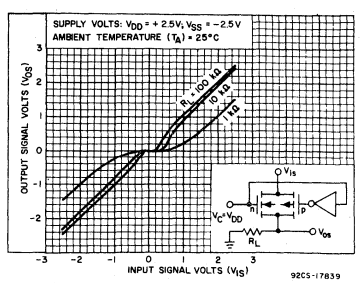


Fig. 6 — Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +2.5 V, V_{SS} = -2.5 V.

ELECTRICAL CHARACTERISTICS (Cont'd) . . . . . $V_{SS} \leq V_I \leq V_{DD}$)

Recommended DC Supply Voltage ($V_{DD}-V_{SS}$). .3 to 15 V)

Characteristic	Test Conditions *All Voltage Values are in Volts*	V_{DD} (V)	Limits *Values at −55°C,+25°C,+125°C Apply to D,F,K,H Packages; Values at −40°C,+25°C,+85°C Apply to E Package* −55°	−40°	+85°	+125°	+25°C Typ.	+25°C Max.	Unit
Crosstalk Between Any 2 of 4 Switches (f = −50 dB)	$V_C(A)=V_{DD}=+5$; $V_C(B)=V_{SS}=-5$; $V_{is}(A)$ = 5 p-p; R_L=1 kΩ; $20\log_{10}\frac{V_{os}(B)}{V_{is}(A)}$ = −50 dB		–	–	–	–	0.9	–	MHz
Propagation Delay (Signal Input to Signal Output) t_{pd}	$V_C = V_{DD}$ = 10; V_{SS} = GND; C_L = 50 pF; V_{is} = 10 Sq. Wave; t_r, t_f = 20 ns	5					20	50	ns
		10					10	25	
Capacitance: Input, C_{is}	V_{DD}=+5		–	–	–	–	4	–	pF
Output, C_{os}	$V_{CC}=V_{SS}=-5$		–	–	–	–	4	–	
Feedthrough, C_{ios}			–	–	–	–	0.2	–	
Control (V_C)†									
Switch Threshold Voltage, V_{TH}	$V_{is} \leq V_{DD}$, I_{is}=10μA; $V_{DD}-V_{SS}$=15,10,5		0.7min 2.9max	–	–	0.2min 2.4max	0.5min 2.7	1.5	V
Input Leakage Current, I_{IL} max	$V_{is} \leq V_{DD}$	V_{DD} =15	$\pm 10^{-5}$ typ; ±1 max.						μA
Crosstalk (Control Input to Signal Output)	V_C=10 (Sq.Wave); t_r,t_f=20 ns; R_L=10 kΩ	V_{DD} =10	–	–	–	–	50	–	mV
Turn-On Propagation Delay, t_p dc	$V_{DD}-V_{SS}$=10; V_C =10 (See Fig.25); t_r,t_f=20 ns; C_L=15 pF; R_L= 1 kΩ	5	–	–	–	–	20	40	ns
		10	–	–	–	–	10	20	
Maximum Allowable Control Input Repetition Rate	V_{DD}=10, V_{SS}=GND; R_L=1 kΩ, C_L=15 pF; V_{CC}=10(Sq.Wave); t_r,t_f = 20 ns		–	–	–	–	10	–	MHz
Av. Input Capacitance, C_I			–	–	–	–	5	–	pF

* Limit determined by minimum feasible leakage current measurement for automatic testing.

▲ Symmetrical about 0 volts.

● For all test conditions.

† All control inputs protected by COS/MOS protection network.

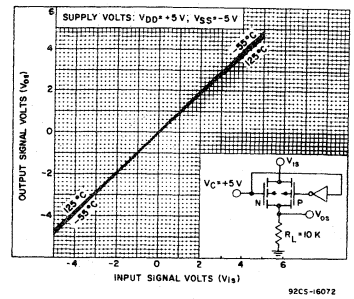


Fig. 7 — Typ. "ON" characteristics as a function of temp. for 1 of 4 switches with V_{DD} = +5 V, V_{SS} = -5 V.

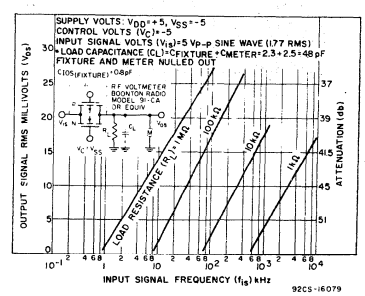


Fig. 8 — Typ. feedthru vs. frequency — switch "OFF".

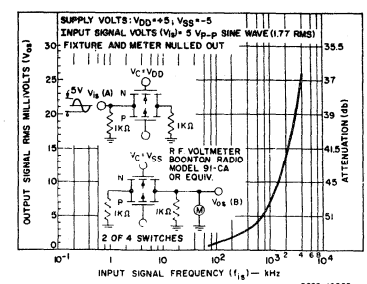


Fig. 9 — Typical crosstalk between switch circuits in the same package.

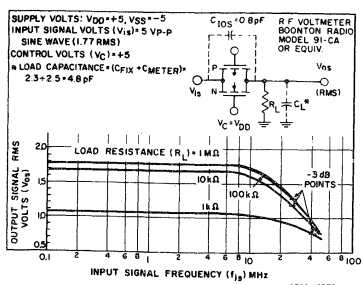


Fig. 10 — Typical switch frequency response — switch "ON".

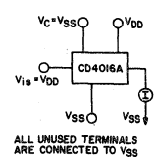


Fig. 11 — "OFF" switch input or output leakage current test circuit.

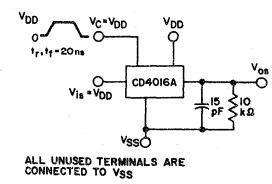


Fig. 12 — Test circuit for square-wave response.

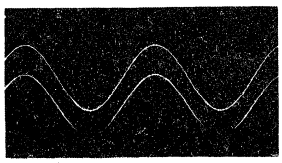


Fig.14 – Typical sine wave response of V_{DD} = +7.5 V, V_{SS} = –7.5 V.

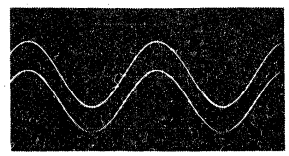


Fig.15 – Typical sine wave response of V_{DD} = +5 V, V_{SS} = –5 V.

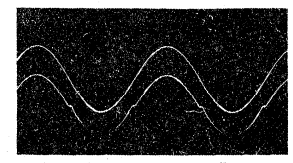


Fig.16 – Typical sine wave response of V_{DD} = +2.5 V, V_{SS} = –2.5 V.

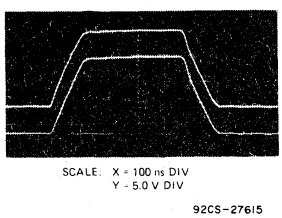


Fig.17 – Typical square wave response at V_{DD} = V_C = +15 V, V_{SS} = Gnd.

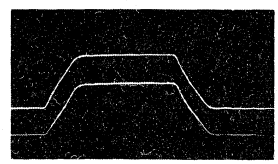


Fig.18 – Typical square wave response at V_{DD} = V_C = +10 V, V_{SS} = Gnd.

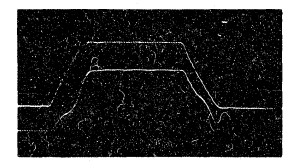


Fig.19 – Typical square wave response at V_{DD} = V_C = +5 V, V_{SS} = Gnd.

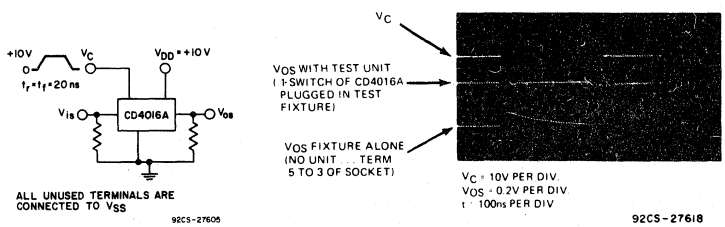


Fig.20 – Crosstalk-control input to signal output.

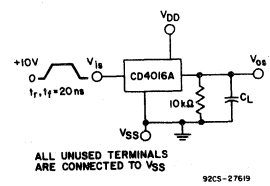


Fig.21 – Propagation delay time signal input (V_{IS}) to signal output (V_{OS}).

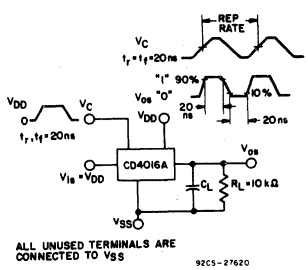


Fig.22 – Max. allowable control-input repetition rate.

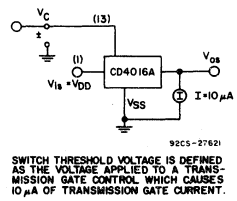


Fig.23 – Switch threshold voltage.

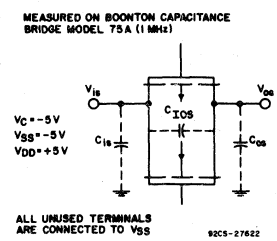


Fig.24 – Capacitance C_{IOS} and C_{OS}.

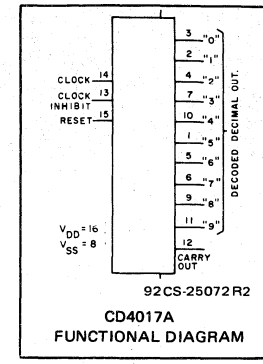
COS/MOS Decade Counter/Divider

Plus 10 Decoded Decimal Outputs

The RCA-CD4017A consists of a 5-stage Johnson decade counter and an output decoder which converts the Johnson binary code to a decimal number. Inputs include a CLOCK, a RESET, and a CLOCK INHIBIT signal.

The decade counter is advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the clock INHIBIT signal is high. A high reset signal clears the decade counter to its zero count. Use of the Johnson decade counter configuration permits high speed operation, 2-input decimal decode gating, and spike-free decoded outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The 10 decoded outputs are normally low and go high only at their respective decimal time slot. Each decoded output remains high for one full clock cycle. A CARRY-OUT (C_{OUT}) signal completes one cycle every 10 clock input cycles and is used to clock the succeeding decade directly in a multi-decade counting chain.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).



CD4017A
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg})	−65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	−55 to +125°C
PACKAGE TYPE E	−40 to + 85°C
DC SUPPLY-VOLTAGE RANGE (V_{DD})	
(Voltages referenced to V_{SS} Terminal)	−0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):	
FOR T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = −55 to 100°C (PACKAGE TYPES D, F, K)	500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

Features:

- Synchronous decade counter plus 10 decoded outputs
- Fully static operation
- Medium speed operation. . . . . 5 MHz (typ.) at $V_{DD} - V_{SS}$ = 10 V
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μA at 15 V (full package-temperature range range)
- 1-V noise margin (full package-temperature range)

Applications:

- Decade counter/decimal decode display
- Frequency division
- Counter control/timers
- Divide by N counting
  N = 2 − 10 with one CD4017A and one one CD4001A
  N > 10 with multiple CD4017A's
- For further application information, see ICAN-6166 "COS/MOS MSI Counter and Register Design & Applications"

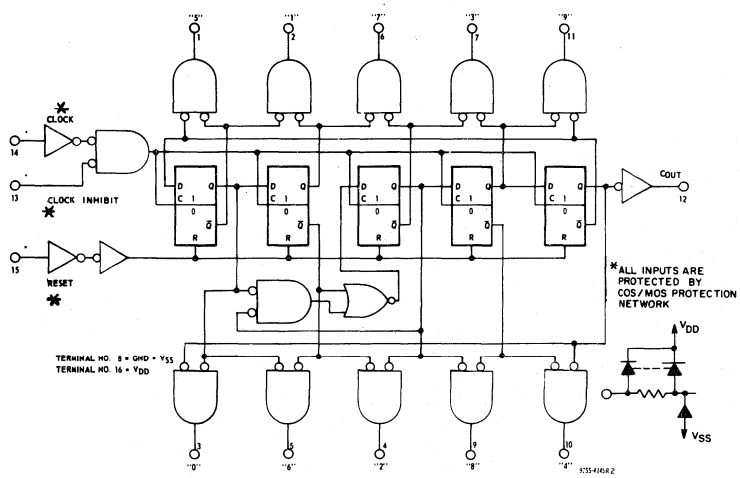


Fig. 1 — Logic diagram.

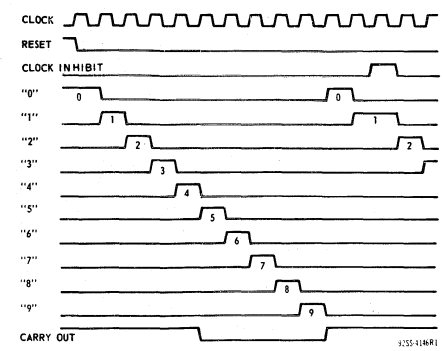


Fig. 2 — Timing diagram.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
				D, K, F, H PACKAGES				E PACKAGE				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	+25 TYP.	+25 LIMIT	+125	-40	+25 TYP.	+25 LIMIT	+85	
Quiescent Device Current, I_L Max.	–	–	5	5	0.3	5	300	50	0.5	50	700	μA
	–	–	10	10	0.5	10	600	100	1	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin Inputs Low V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink)												mA
I_{DN} Min Decoded Outputs	0.5	–	5	0.06	0.1	0.05	0.035	0.03	0.1	0.025	0.02	
	0.5	–	10	0.12	0.4	0.1	0.07	0.085	0.4	0.07	0.055	
I_{DN} Min Carry Output	0.5	–	5	0.185	0.4	0.15	0.105	0.095	0.4	0.08	0.065	
	0.5	–	10	0.45	1	0.35	0.25	0.3	1	0.25	0.2	
P-Channel (Source)												
I_{DP} Min Decoded Outputs	4.5	–	5	−0.0375	−0.075	−0.03	−0.021	−0.018	−0.075	−0.015	−0.012	
	9.5	–	10	−0.12	−0.2	−0.1	−0.07	−0.085	−0.2	−0.07	−0.055	
I_{DP} Min Carry Output	4.5	–	5	−0.185	−0.4	−0.15	−0.105	−0.095	−0.4	−0.08	−0.065	
	9.5	–	10	−0.45	−1	−0.35	−0.25	−0.3	−1	−0.24	−0.20	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		15	$\pm 10^{-5}$ Typ., ±1 Max.								μA

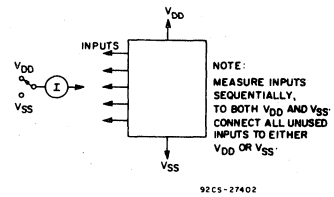


Fig. 10 – Input-leakage-current test circuit.

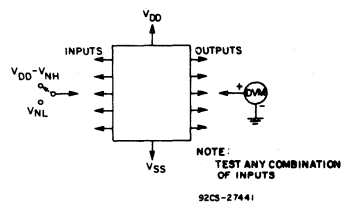


Fig. 11 – Noise-immunity test circuit.

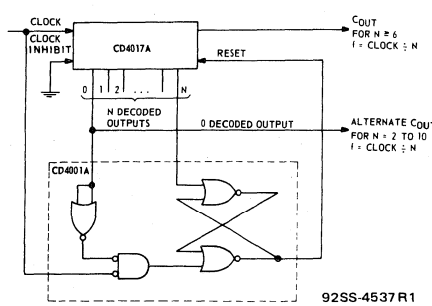


Fig. 12 – Divide by N counter ($N \leq 10$) with N decoded outputs.

When the N^{th} decoded output is reached (N^{th} clock pulse) the S-R flip flop (constructed from two NOR gates of the CD4001A) generates a reset pulse which clears the CD4017A to its zero count. At this time, if the N^{th} decoded output is greater than or equal to 6, the C_{OUT} line goes high to clock the next CD4017A counter section. The "0" decoded output also goes high at this time. Coincidence of the clock low and decoded "0" output low resets the S-R flip flop to enable the CD4017A. If the N^{th} decoded output is less than 6, the C_{OUT} line will not go high and, therefore, cannot be used. In this case "0" decoded output may be used to perform the clocking function for the next counter.

RECOMMENDED OPERATING CONDITIONS *at T_A = 25°C, Except as Noted.*
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, K, H PACKAGES		E PACKAGE		
		MIN.	MAX.	MIN.	MAX.	
Supply Voltage Range (For T_A=Full Package-Temperature Range)		3	12	3	12	V
Clock Inhibit Setup Time, t_S	5 10	500 200	– –	700 300	– –	ns
Clock Pulse Width, t_W	5 10	500 170	– –	830 250	– –	ns
Clock Input Frequency, f_{CL}	5 10	dc dc	1 3	dc dc	0.6 2	MHz
Clock Rise or Fall Time, t_rCL, t_fCL	5 10	– –	15 15	– –	15 15	μs
Reset Pulse Width, t_W	5 10	500 165	– –	830 250	– –	ns
Reset Removal Time	5 10	750 225	– –	1000 275	– –	ns

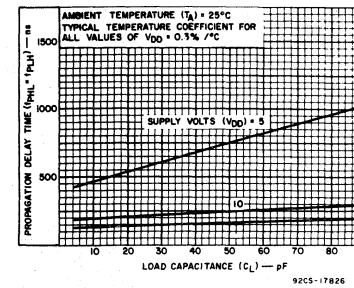


Fig. 3 – Typical propagation delay time vs. C_L for decoded outputs.

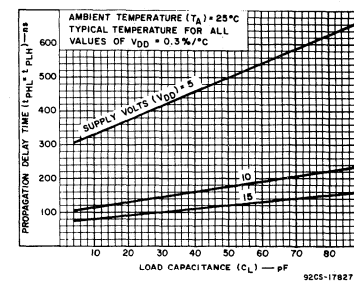


Fig. 4 – Typical propagation delay time vs. C_L for carry output.

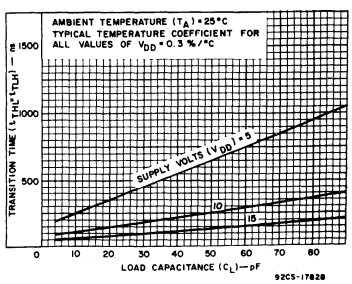


Fig. 5 – Typical transition time vs. C_L for decoded outputs.

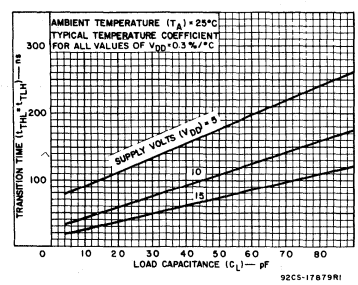


Fig. 6 – Typical transition time vs. C_L for carry output.

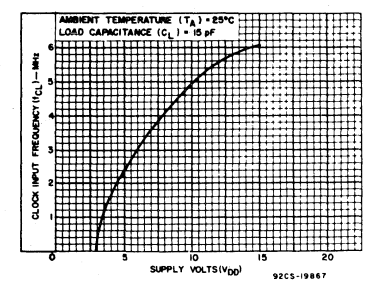


Fig. 7 – Typical clock input frequency vs. V_{DD}.

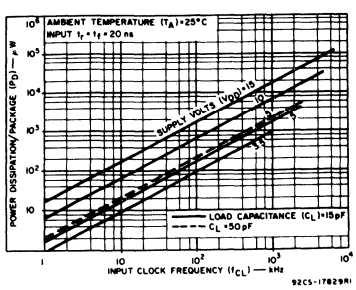
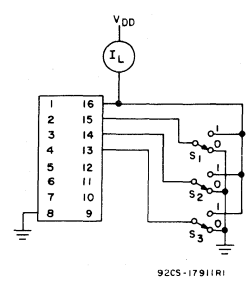


Fig. 8 – Typical dissipation characteristics.



Test performed with the following sequence of "1's and "0's" at each switch.

S_1	S_2	S_3	S_1	S_2	S_3
1	1	1	0	1	0
0	0	0	0	0	0
0	1	0	0	1	0
0	0	0	0	0	0
0	1	0	0	1	0
0	0	0	0	0	0
			0	1	0

Fig. 9 – Quiescent device current test circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25^oC$, Input $t_r, t_f = 20$ ns, $C_L = 15$ pF, $R_L = 200$ kΩ

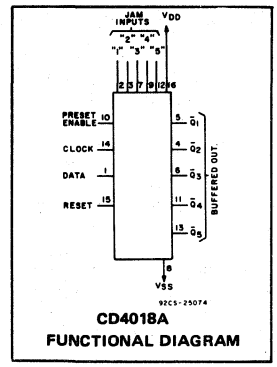
CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS D, F, K, H PACKAGES MIN.	TYP.	MAX.	LIMITS E PACKAGE MIN.	TYP.	MAX.	UNITS
CLOCKED OPERATION								
Propagation Delay Time; t_{PHL} t_{PLH} Carry Out Line	5	–	350	1000	–	350	1300	ns
	10	–	125	250	–	125	300	
Decode Out Lines	5	–	500	1200	–	500	1600	
	10	–	200	400	–	200	500	
Transition Time; t_{THL}, t_{TLH} Carry Out Line	5	–	100	300	–	100	350	ns
	10	–	50	150	–	50	200	
Decode Out Lines	5	–	300	900	–	300	1200	
	10	–	125	350	–	125	450	
Maximum Clock Input Frequency, f_{CL}*	5	1	2.5	–	0.6	2.5	–	MHz
	10	3	5	–	2	5	–	
Minimum Clock Pulse Width, t_W	5	–	200	500	–	200	830	ns
	10	–	100	170	–	100	250	
Clock Rise & Fall Time; t_rCL, t_fCL	5	–	–	15	–	–	15	μs
	10	–	–	15	–	–	15	
Minimum Clock Inhibit Set-Up Time, t_s	5	–	175	500	–	175	700	ns
	10	–	75	200	–	75	300	
Average Input Capacitance, C_I	Any Input	–	5	–	–	5	–	pF
RESET OPERATION								
Propagation Delay Time; t_{PHL} To Carry Out Line	5	–	350	1000	–	350	1300	ns
	10	–	125	250	–	125	300	
To Decode Out Lines	5	–	450	1200	–	450	1600	
	10	–	200	400	–	200	500	
Minimum Reset Pulse Width, t_W	5	–	200	500	–	200	830	ns
	10	–	100	165	–	100	250	
Minimum Reset Removal Time	5	–	300	750	–	300	1000	ns
	10	–	100	225	–	100	275	

*Measured with respect to carry output line

COS/MOS Presettable Divide-By-'N' Counter

The RCA-CD4018A types consist of 5 Johnson-Counter stages, buffered $\overline{Q}$ outputs from each stage, and counter preset control gating. CLOCK, RESET, DATA, PRESET ENABLE, and 5 individual JAM inputs are provided. Divide by 10, 8, 6, 4, or 2 counter configurations can be implemented by feeding the $\overline{Q}5$, $\overline{Q}4$, $\overline{Q}3$, $\overline{Q}2$, $\overline{Q}1$ signals, respectively, back to the DATA input. Divide-by-9, 7, 5, or 3 counter configurations can be implemented by the use of a CD4011A gate package to properly gate the feedback connection to the DATA input. Divide-by functions greater than 10 can be achieved by use of multiple CD4018A units. The counter is advanced one count at the positive clock-signal transition. A high RESET signal clears the counter to an all-zero condition. A high PRESET-ENABLE signal allows information on the JAM inputs to preset the counter. Anti-lock gating is provided to assure the proper counting sequence.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).



CD4018A
FUNCTIONAL DIAGRAM

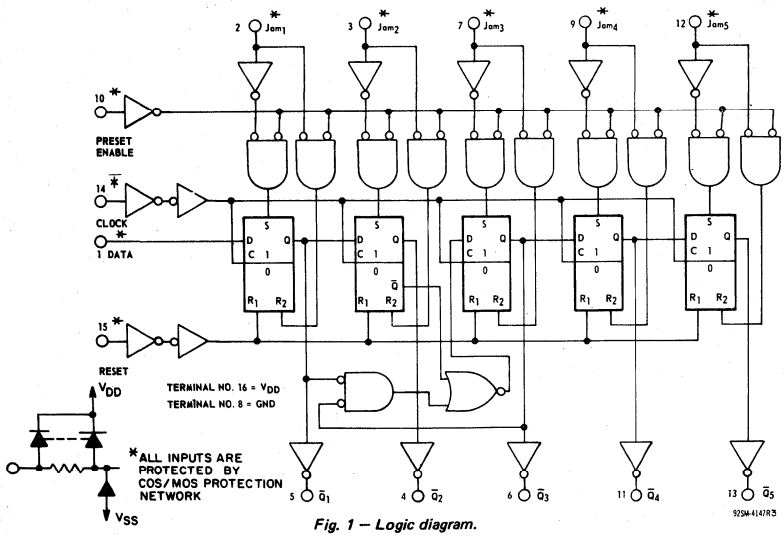


Fig. 1 – Logic diagram.

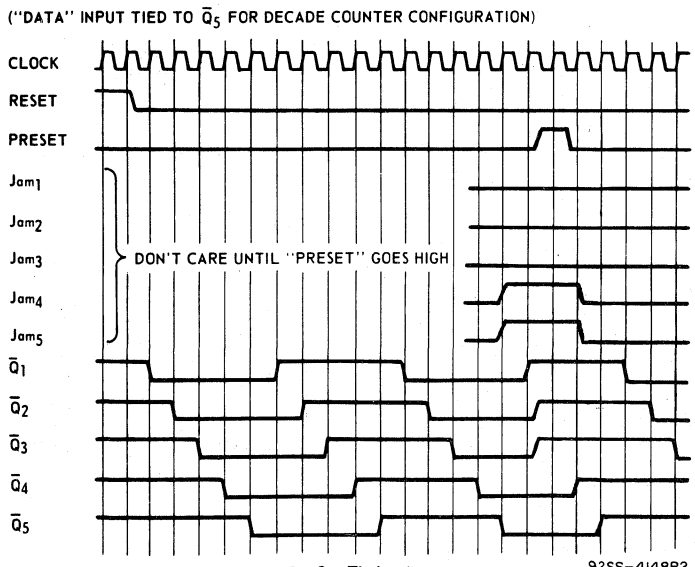


Fig. 2 – Timing diagram.

Features:

- Medium speed operation . . . . 5 MHz (typ.) at $V_{DD} - V_{SS} = 10$ V
- Fully static operation
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications:

- Fixed and programmable divide-by-10, 9, 8, 7, 6, 5, 4, 3, 2 counters
- Fixed and programmable counters greater than 10
- Programmable decade counters
- Divide-by-"N" counters/frequency synthesizers
- Frequency division
- Counter control/timers

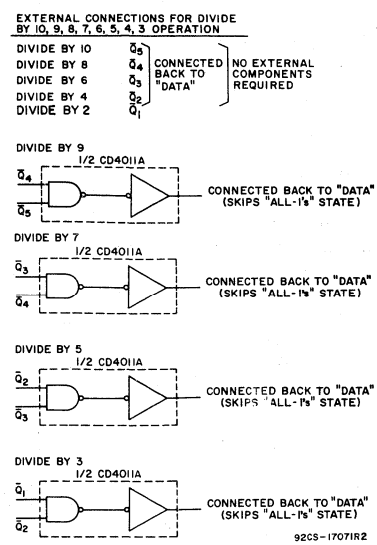


Fig. 3 – External connections for divide by 10, 9, 8, 7, 6, 5, 4, 3, 2 operation.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
PACKAGE TYPE E . . . . . –40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): . . . . . –0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A= –40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
FOR T_A= +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A= –55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
FOR T_A= +100 to +125°C (PACKAGE TYPES D, F, K) . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A= FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max . . . . . +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		D,F,K,H Packages			*E Package*			
	V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
CLOCKED OPERATION								
Propagation Delay Time; t_{PLH}, t_{PHL} To $\overline{Q}_5$ Output	5	–	350	1000	–	350	1300	ns
	10	–	125	250	–	125	300	
To Other Outputs	5	–	500	1200	–	500	1600	
	10	–	200	400	–	200	500	
Transition Time; t_{THL}, t_{TLH} To $\overline{Q}_5$ Output	5	–	100	300	–	100	350	ns
	10	–	50	150	–	50	200	
To Other Outputs	5	–	300	900	–	300	1200	ns
	10	–	125	350	–	125	450	
Maximum Clock Input Frequency, f_{CL}	5	1	2.5	–	0.6	2.5	–	MHz
	10	3	5	–	2	5	–	
Min. Clock Pulse Width, t_W	5	–	200	500	–	200	830	ns
	10	–	100	170	–	100	250	
Clock Rise & Fall Time; t_rCL, t_fCL	5	–	–	15	–	–	15	μs
	10	–	–	15	–	–	15	
Min. Data Input Set-Up Time, t_S	5	–	175	500	–	175	700	ns
	10	–	75	200	–	75	300	
Average Input Capacitance, C_I	Any Input	–	5	–	–	5	–	pF
PRESET* OR RESET OPERATION								
Propagation Delay Time: t_{PLH}, t_{PHL} To $\overline{Q}_5$ Output	5	–	350	1000	–	350	1300	ns
	10	–	125	250	–	125	300	
To Other Outputs	5	–	500	1200	–	500	1600	
	10	–	200	400	–	200	500	
Min. Preset or Reset Pulse Width t_W	5	–	200	500	–	200	830	ns
	10	–	100	165	–	100	250	
Min. Preset or Reset Removal Time	5	–	300	750	–	300	1000	
	10	–	100	225	–	100	275	

* At PRESET ENABLE OR JAM Inputs.

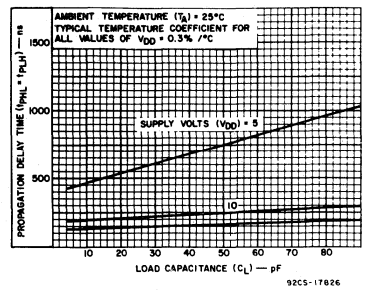


Fig. 4 – Typical propagation delay time vs. load capacitance for decoded outputs.

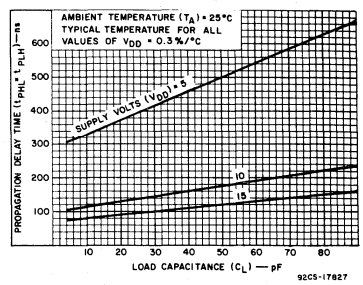


Fig. 5 – Typical propagation delay time vs. load capacitance for $\overline{Q}_5$ output.

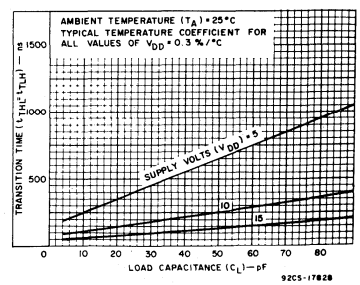


Fig. 6 – Typical transition time vs. load capacitance for decoded outputs.

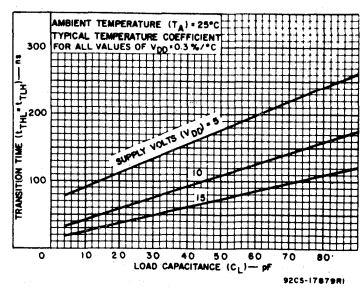


Fig. 7 – Typical transition time vs. load capacitance for $\overline{Q}_5$ output.

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D,F,K,H Packages		*E Package*		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Data Setup Time, t_S	5	500	–	700	–	ns
	10	200	–	300	–	
Clock Pulse Width, t_W	5	500	–	830	–	ns
	10	170	–	250	–	
Clock Input Frequency, f_{CL}	5	dc	1	dc	0.6	MHz
	10	dc	3	dc	2	
Clock Rise and Fall Time, t_rCL, t_fCL	5	–	15	–	15	μs
	10	–	15	–	15	
Preset or Reset Pulse Width, t_W	5	500	–	830	–	ns
	10	165	–	250	–	
Preset or Reset Removal Time	5	750	–	1000	–	ns
	10	225	–	275	–	

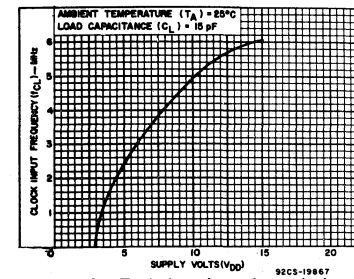


Fig. 8 – Typical maximum input clock frequency vs. supply voltage.

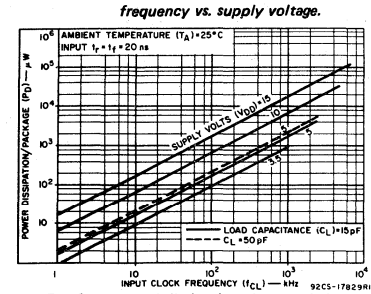


Fig. 9 – Typical dissipation characteristics

STATIC ELECTRICAL CHARACTERISTICS

Characteristic		Conditions			Limits at Indicated Temperatures (°C)								Units
					D,K,F,H packages				*E Package*				
		V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	+25 Typ.	+25 Limit	+125	–40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current I_L Max.		–	–	5	5	0.3	5	300	50	0.5	50	700	μA
		–	–	10	10	0.5	10	600	100	1	100	1400	
		–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low Level, V_{OL}		–	5	5	0 Typ.; 0.05 Max.								V
		–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}		–	0	5	4.95 Min.; 5 Typ.								
		–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}		4.2	–	5	1.5 Min.; 2.25 Typ.								V
		9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}		0.8	–	5	1.5 Min.; 2.25 Typ.								
		1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}		4.5	–	5	1 Min.								V
		9	–	10	1 Min.								
Inputs High, V_{NMH}		0.5	–	5	1 Min.								
		1	–	10	1 Min.								
Output Drive Current: n-Channel (Sink) I_DN Min.	$\overline{Q}_5$	0.5	–	5	0.18	0.4	0.15	0.105	0.095	0.4	0.08	0.065	mA
		0.5	–	10	0.45	1	0.35	0.25	0.3	1	0.25	0.2	
	$\overline{Q}_1,\overline{Q}_2$	0.5	–	5	0.06	0.1	0.05	0.035	0.03	0.1	0.025	0.02	
	$\overline{Q}_3,\overline{Q}_4$	0.5	–	10	0.25	0.4	0.2	0.14	0.18	0.4	0.15	0.12	
p-Channel (Source) I_DP Min.	$\overline{Q}_5$	4.5	–	5	-0.185	-0.4	-0.15	-0.105	-0.095	-0.4	-0.08	-0.065	
		9.5	–	10	-0.45	-1	-0.35	-0.25	-0.3	-1	-0.25	-0.2	
	$\overline{Q}_1,\overline{Q}_2$	4.5	–	5	-0.075	-0.15	-0.06	-0.04	-0.035	-0.15	-0.03	-0.024	
	$\overline{Q}_3,\overline{Q}_4$	9.5	–	10	-0.25	-0.4	-0.2	-0.14	-0.18	-0.4	-0.15	-0.12	
Input Leakage Current, I_{IL}, I_{IH} Max.		Any Input			±10^{-5} Typ., ±1 Max.								μA
		–	–	15									

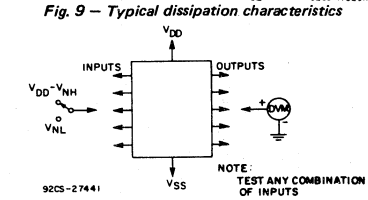
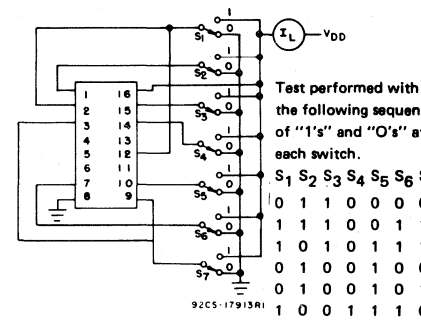


Fig. 10 – Noise-immunity test circuit



Test performed with the following sequence of "1's" and "0's" at each switch.

S_1	S_2	S_3	S_4	S_5	S_6	S_7
0	1	1	0	0	0	0
1	1	1	0	0	1	1
1	0	1	0	1	1	1
0	1	0	0	1	0	0
0	1	0	0	1	0	1
1	0	0	1	1	1	0
0	0	0	1	0	0	0
0	0	0	0	0	0	0
1	0	0	0	1	0	0
0	0	0	0	0	1	0
0	0	0	0	0	0	0

Fig. 11 – Quiescent-device-current test circuit.

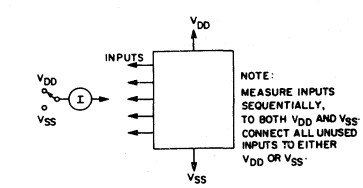
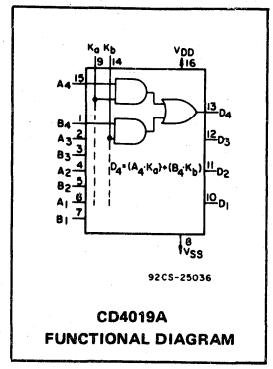


Fig. 12 – Input-leakage-current test circuit.

COS/MOS Quad AND/OR Select Gate

The RCA-CD4019A types are comprised of four AND/OR select gate configurations, each consisting of two 2-input AND gates driving a single 2-input OR gate. Selection is accomplished by control bits K_a and K_b. In addition to selection of either channel A or channel B information, the control bits can be applied simultaneously to accomplish the logical A + B function.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).



CD4019A FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): . . . . . −0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max . . . . . +265°C

RECOMMENDED OPERATING CONDITIONS
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D,F,K,H Packages		*E Package*		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	

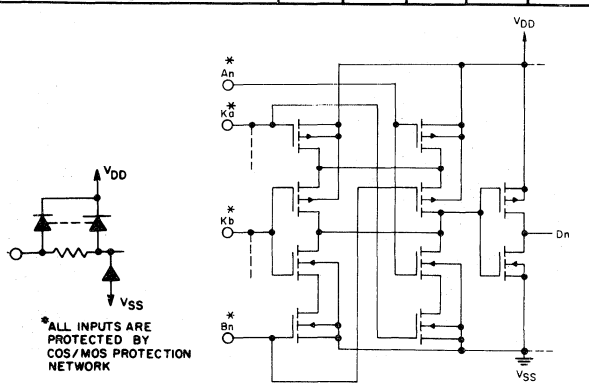


Fig. 1 — Schematic diagram for 1 of 4 identical stages.

Features:

- **Medium-speed operation . . . . . $t_{PHL} = t_{PLH}$ = 50 ns (typ.) at C_L = 15 pF, V_{DD} = 10 V**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **AND-OR select gating**
- **Shift-right/shift-left registers**
- **True/complement selection**
- **AND/OR/Exclusive-OR selection**

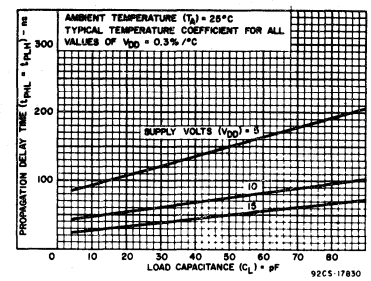


Fig. 2 — Typical propagation delay time vs. load capacitance.

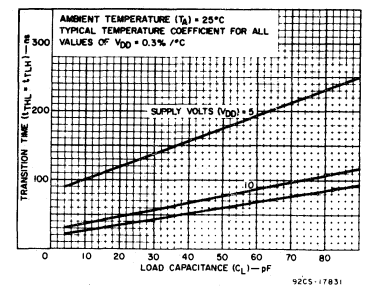


Fig. 3 — Typical transition time vs. load capacitance.

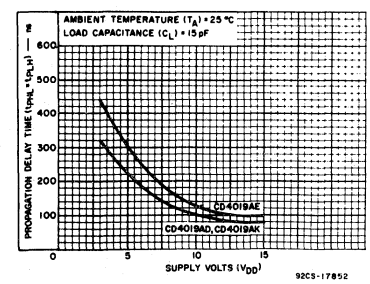


Fig. 4 — Maximum propagation delay time vs. supply voltage.

STATIC ELECTRICAL CHARACTERISTCS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				E Package				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	5	0.03	5	300	50	0.1	50	700	μA
	–	–	10	10	0.05	10	600	100	0.2	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	3.6	–	5	1.5 Min.; 2.25 Typ.								V
	7.2	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	1.4	–	5	1.5 Min.; 2.25 Typ.								
	2.8	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: n-Channel (Sink) I_{DN} Min.	0.5	–	5	0.6	0.9	0.45	0.3	0.37	1	0.3	0.23	mA
	0.5	–	10	0.9	1.5	0.75	0.55	0.8	1.5	0.65	0.5	
p-Channel (Source): I_{DP} Min.	4.5	–	5	-0.31	-0.5	-0.25	-0.175	-0.145	-0.5	-0.12	-0.095	
	9.5	–	10	-0.95	-1.5	-0.7	-0.5	-0.6	-1.5	-0.5	-0.4	
Input Leakage Current, I_{IL}, I_{IH}	Any Input	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								μA

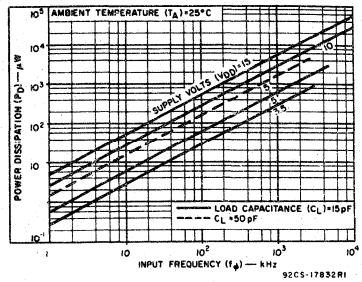


Fig. 5 — Typical dissipation characteristics. (per output).

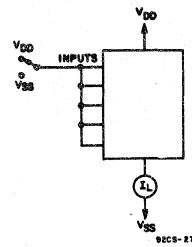


Fig. 6 — Quiescent-device-current test circuit.

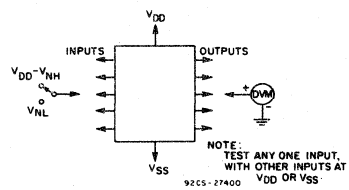


Fig. 7 — Noise-immunity test circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
			D,F,K,H Packages			E Package			
		V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
Propagation Delay Time; t_{PLH}, t_{PHL}		5	–	100	225	–	100	300	ns
		10	–	50	100	–	50	125	
Transition Time; t_{THL}, t_{TLH}		5	–	100	200	–	100	275	ns
		10	–	40	65	–	40	80	
Average Input Capacitance, C_I	All A and B Inputs		–	5	–	–	5	–	pF
	K_a and K_b Inputs		–	12	–	–	12	–	pF

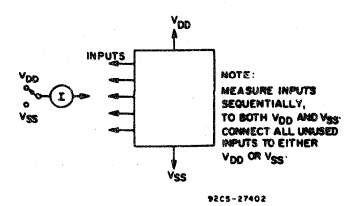
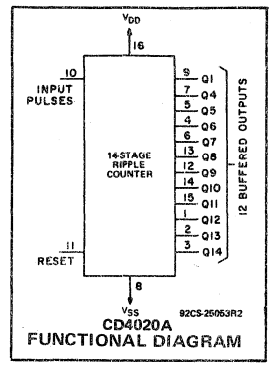


Fig. 8 — Input-leakage-current test circuit.

COS/MOS 14-Stage Ripple-Carry Binary Counter/Divider

The RCA-CD4020 consists of a PULSE INPUT shaping circuit, RESET line driver circuitry, and 14 ripple-carry binary counter stages. Buffered outputs are externally available from stages 1 and 4 through 14. The counter is reset to its all-zeroes state by a high level on the RESET inverter input line. Each counter stage is a static master-slave flip-flop. The counter is advanced one count on the negative-going transition of each INPUT PULSE.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).



CD4020A
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) ..... −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H ..... −55 to +125°C

PACKAGE TYPE E ..... −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal) ..... −0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = −40 to +60°C (PACKAGE TYPE E) ..... 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) ..... Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) .... 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS D,F,K,H Packages Min.	LIMITS D,F,K,H Packages Max.	LIMITS E Package Min.	LIMITS E Package Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Input Pulse Width, t_W	5	335	–	500	–	ns
	10	125	–	165	–	
Input Pulse Frequency, f_ϕ	5	dc	1.5	dc	1.5	MHz
	10	dc	4	dc	4	
Input Pulse Rise or Fall Time, $t_{r\phi}$,$t_{f\phi}$	5	–	15	–	15	μs
	10	–	15	–	15	
Reset Pulse Width, t_W	5	2500	–	3000	–	ns
	10	475	–	550	–	

Features:

- Medium speed operation . . . 7 MHz (typ.) at $V_{DD}-V_{SS}$ = 10 V
- Low output impedance
- Common reset
- Fully static operation
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications:

- Frequency-dividing circuits
- Time-delay circuits
- Counter control
- Counting functions

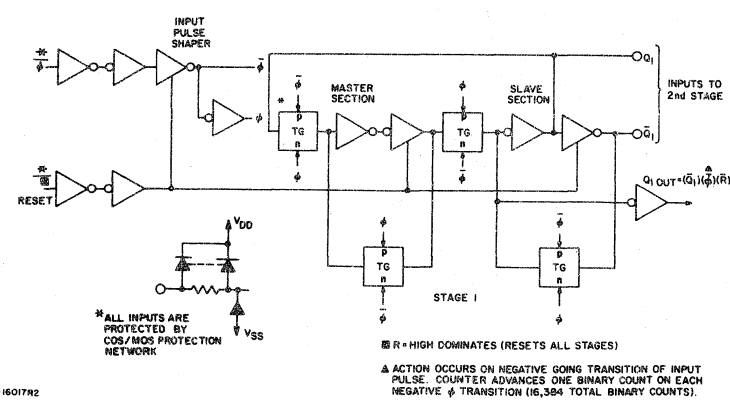


Fig. 1—Logic diagram for 1 of 14 binary stages.

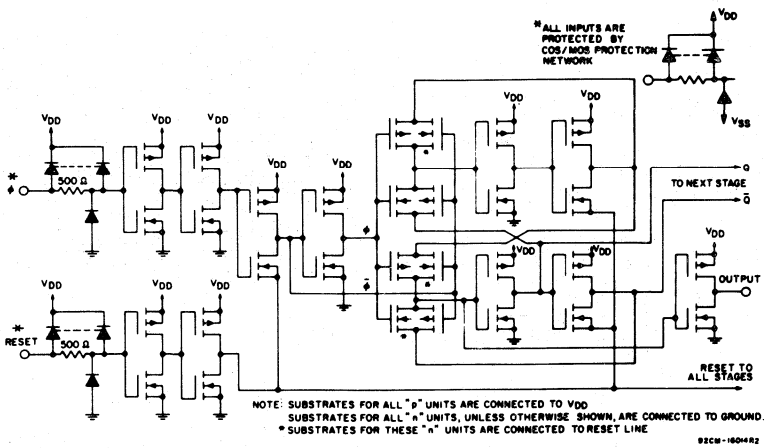


Fig. 2 – Schematic diagram of pulse shapers and 1 of 14 binary stages.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				E Package				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	15	0.5	15	900	50	1	50	700	μA
	–	–	10	25	1	25	1500	100	2	100	1400	
	–	–	15	50	2.5	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High-Level, V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink), I_DN Min.	0.5	–	5	0.09	0.2	0.075	0.05	0.09	0.33	0.08	0.065	mA
	0.5	–	10	0.185	0.4	0.15	0.105	0.16	0.5	0.10	0.10	
P-Channel (Source) I_DP Min.	4.5	–	5	−0.11	−0.25	−0.09	−0.065	−0.09	−0.25	−0.06	−0.05	
	9.5	–	10	−0.25	−0.5	−0.20	−0.14	−0.18	−0.5	−0.15	−0.12	
Input Leakage Current, I_{IL}, I_{IH}	Any Input			±10^{-5} Typ., ±1 Max.								μA
	–	–	15									

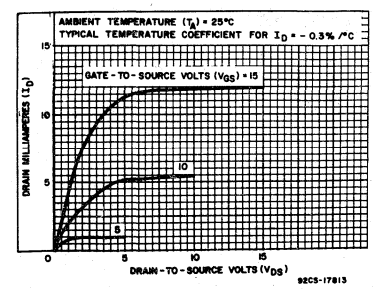


Fig. 3—Typical output n-channel drain characteristics.

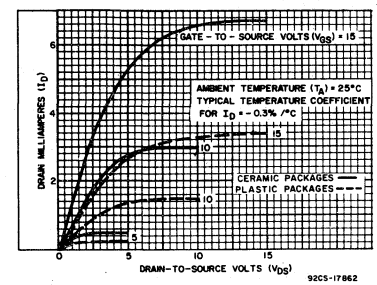


Fig. 4—Minimum output n-channel drain characteristics.

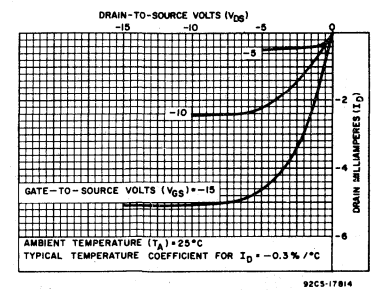


Fig. 5—Typical output p-channel drain characteristics.

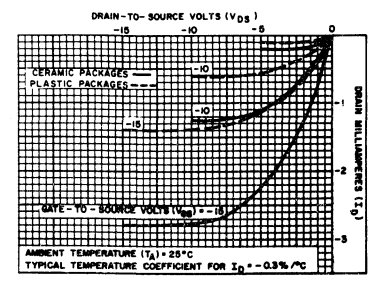


Fig. 6—Minimum output p-channel drain characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r,t_f = 20 ns, C_L = 15 pF, R_L 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
			D,F,K,H Packages			E Package			
		V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
Clocked Operation									
Propagation Delay Time,* t_{PLH}, t_{PHL}		5	–	450	600	–	450	650	ns
		10	–	150	225	–	150	250	
Transition Time, t_{THL}, t_{TLH}		5	–	450	600	–	450	650	ns
		10	–	200	300	–	200	350	
Maximum Input Pulse Frequency, f_ϕ		5	1.5	2.5	–	1.5	2.5	–	MHz
		10	4	6	–	4	6	–	
Minimum Input Pulse Width, t_W		5	–	200	335	–	200	500	ns
		10	–	70	125	–	70	165	
Input Pulse Rise & Fall Time, $t_{r\phi}$,$t_{f\phi}$		5	–	–	15	–	–	15	μs
		10	–	–	15	–	–	15	
Average Input Capacitance, C_I	Any Input		–	–	5	–	–	5	pF
Reset Operation									
Propagation Delay Time,* t_{PHL}		5	–	2000	3000	–	2000	3500	ns
		10	–	500	775	–	500	300	
Minimum Reset Pulse Width, t_W		5	–	1800	2500	–	1800	3000	ns
		10	–	300	475	–	300	550	

* Propagation delay is from input pulse to Q_1 output.

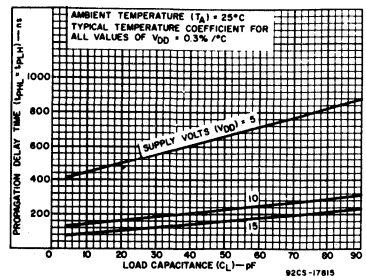


Fig. 7—Typical propagation delay time vs. C_L.

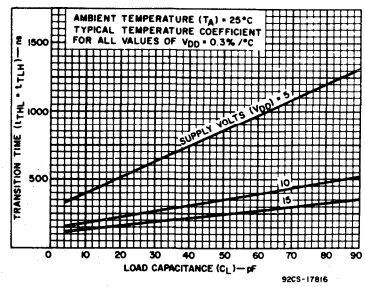


Fig. 8—Typical transition time vs. C_L.

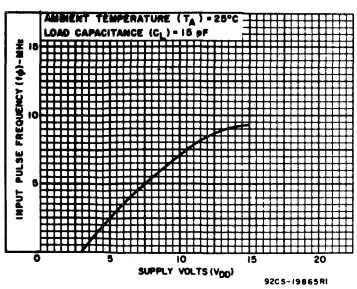


Fig. 9—Typical clock input frequency vs. V_{DD}.

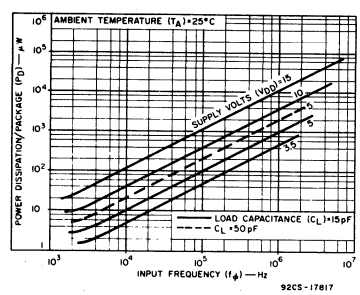


Fig. 10—Typical dissipation characteristics.

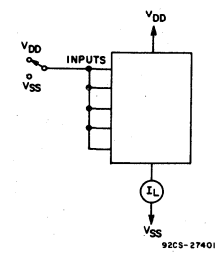


Fig. 11—Quiescent-device-current test circuit.

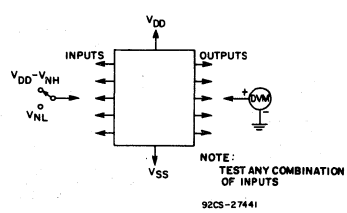


Fig. 12—Noise-immunity test circuit.

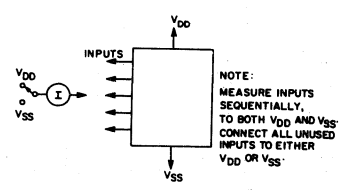


Fig. 13—Input-leakage-current test circuit.

COS/MOS 8-Stage Static Shift Register

Asynchronous Parallel Input/Serial Output,
Synchronous Serial Input/Serial Output

The RCA-CD4021A types are 8-stage parallel or serial-input/serial-output shift registers having common CLOCK and PARALLEL/SERIAL CONTROL inputs, a single SERIAL DATA input, and individual parallel Jam inputs to each register stage. Each register stage is a D-type, master-slave flip-flop. Q outputs are available from the sixth, seventh, and eighth stages.

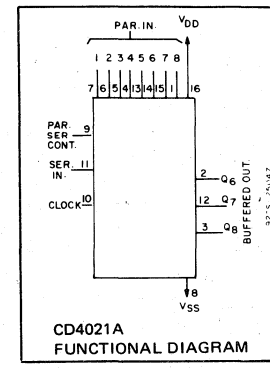
When the PARALLEL/SERIAL CONTROL input is low, data are serially shifted into the 8-stage register synchronously with the positive-going transition of the CLOCK pulse.

Features:

- **Asynchronous parallel or synchronous serial operation under control of parallel/serial control-input**
- **Individual JAM inputs to each register stage**
- **Master-slave flip-flop register stages**
- **Fully static operation. . . . . DC to 5 MHz**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

When the PARALLEL/SERIAL CONTROL input is high, data are jammed into the 8-stage register via the parallel input lines asynchronously with the clock line.

Register expansion is possible using additional CD4021A packages.



CD4021A
FUNCTIONAL DIAGRAM

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

Applications:

- **Parallel to serial data conversion**
- **Asynchronous parallel input/serial output data queueing**
- **General purpose register**

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
				D, K, F, H PACKAGES				E PACKAGE				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	+25 TYP.	+25 LIMIT	+125	-40	+25 TYP.	+25 LIMIT	+85	
Quiescent Device Current I_L Max.	–	–	5	5	0.5	5	300	50	0.5	50	700	μA
	–	–	10	10	1	10	600	100	1	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ., 0.05 Max.								V
	–	10	10	0 Typ., 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity; Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink),	0.5	–	5	0.15	0.3	0.12	0.085	0.072	0.3	0.06	0.05	mA
I_DN Min.	0.5	–	10	0.31	0.5	0.25	0.175	0.12	0.5	0.1	0.08	
P-Channel (Source)	4.5	–	5	-0.1	-0.16	-0.08	-0.055	-0.06	-0.16	-0.05	-0.04	
I_DP Min.	9.5	–	10	-0.25	-0.44	-0.20	-0.14	-0.12	-0.44	-0.1	-0.08	
Input Leakage Current,	Any Input											
I_{IL}, I_{IH}	–	–	15	$\pm 10^{-5}$ Typ., ± 1 Max.								

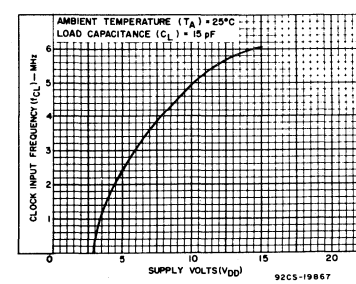


Fig. 1 – Typical clock input frequency vs. supply voltage.

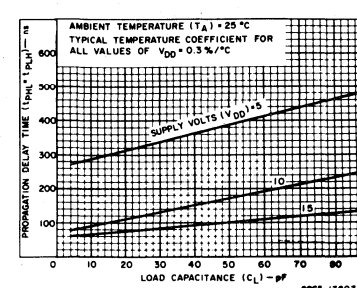


Fig. 2 – Typical propagation delay time vs. load capacitance.

CD4021A Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A)\

PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C

PACKAGE TYPE E . . . . . –40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal) . . . . . –0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D)

FOR T_A = –40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPE E) \ . . . . . Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = –55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

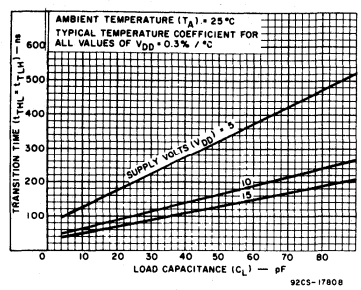


Fig. 3 – Typical transition time vs. load capacitance.

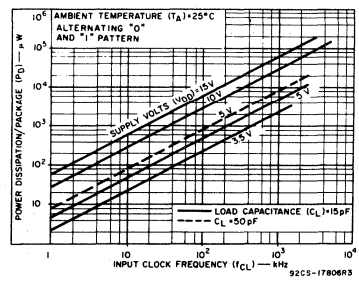


Fig. 4 – Typical dissipation characteristics.

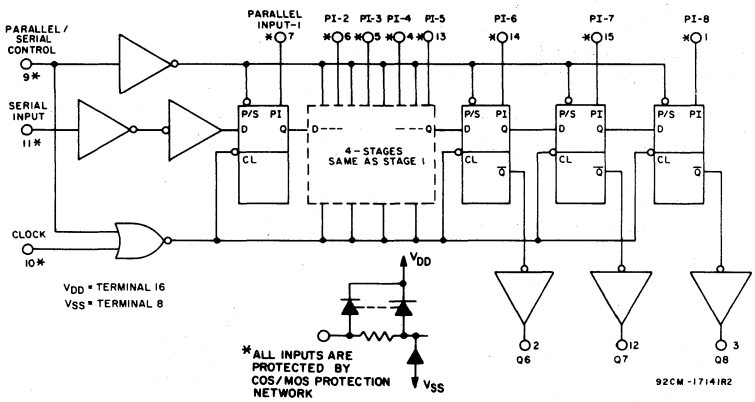


Fig. 5 – Logic diagram.

TRUTH TABLE

CL▲	Serial Input	Parallel/ Serial Control	PI-1	PI-n	Q_1 (Internal)	Q_n
X	X	1	0	0	0	0
X	X	1	0	1	0	1
X	X	1	1	0	1	0
X	X	1	1	1	1	1
⎍	0	0	X	X	0	Q_n-1
⎍	1	0	X	X	1	Q_n-1
⎎	X	0	X	X	Q_1	Q_n

▲ = LEVEL CHANGE X = DON'T CARE CASE

NO CHANGE

92CS-17141R3

Fig. 6 – Truth table.

RECOMMENDED OPERATING CONDITIONS *at T_A = 25°C, Except as Noted.*

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, K, H PACKAGES		E PACKAGE		
		MIN.	MAX.	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)		3	12	3	12	V
Data Setup Time, t_S	5 10	350 80	– –	500 100	– –	ns
Clock Pulse Width, t_W	5 10	500 175	– –	830 200	– –	ns
Clock Input Frequency, f_{CL}	5 10	dc dc	1 3	dc dc	0.6 2.5	MHz
Clock Rise and Fall Time, t_rCL, t_fCL*	5 10	– –	15 15	– –	15 15	μs

*If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

DYNAMIC ELECTRICAL CHARACTERISTICS

at $T_A = 25^oC$, Input t_r, $t_f = 20$ ns, $C_L = 15$ pF, $R_L = 200$ kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		D, F, K, H PACKAGES			E PACKAGE			
	V_{DD} (V)	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Propagation Delay Time,** t_{PLH}, t_{PHL}	5	–	300	750	–	300	1000	ns
	10	–	100	225	–	300	300	
Transition Time; t_{THL}, t_{TLH}	5	–	150	300	–	150	400	ns
	10	–	75	125	–	75	150	
Maximum Clock Input Frequency, f_{CL}	5	1	2.5	–	0.6	2.5	–	MHz
	10	3	5	–	2.5	5	–	
Minimum Clock Pulse Width, t_W	5	–	200	500	–	200	830	ns
	10	–	100	175	–	100	200	
Clock Rise & Fall Time; t_rCL & t_fCL*	5	–	–	15	–	–	15	μs
	10	–	–	15	–	–	15	
Minimum Data Set Up Time, t_S	5	–	100	350	–	100	500	ns
	10	–	50	80	–	50	100	
Minimum High-Level Parallel/Serial Control Pulse Width t_W	5	–	200	500	–	200	830	ns
	10	–	100	175	–	100	200	
Input Capacitance C_I	Any Input	–	5	–	–	5	–	pF

*If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

**From Clock or Parallel/Serial Control Input

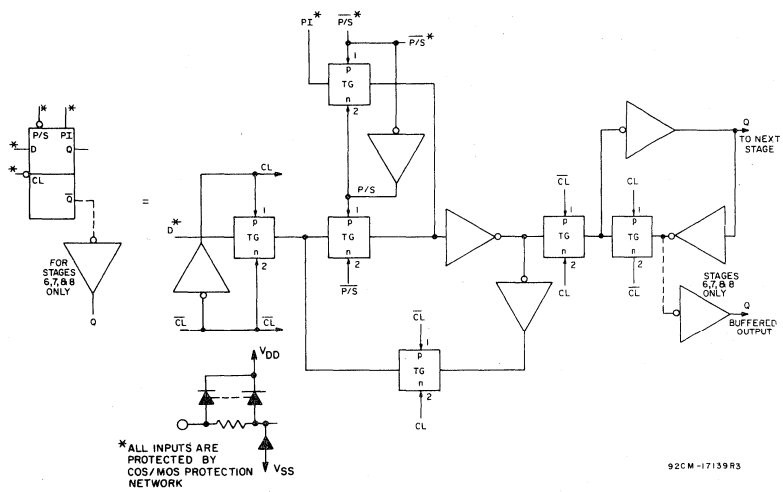


Fig. 10 – One typical stage and its equivalent detailed circuit.

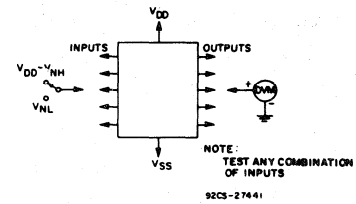


Fig. 7 – Noise-immunity test circuit.

Test performed with the following sequence of "One's" and "Zero's".

S_1	S_2	S_3	S_4	S_5
0	0	1	0	0
1	0	1	1	1
1	0	1	0	1
0	1	1	1	1
0	1	0	0	0

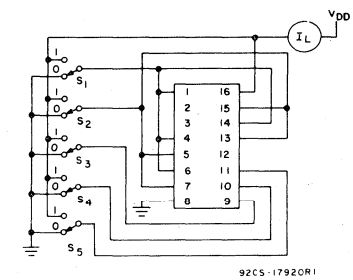


Fig. 8 – Quiescent device current test circuit.

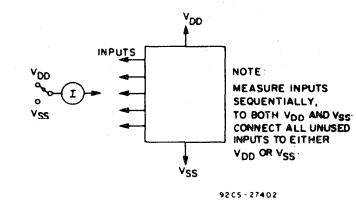


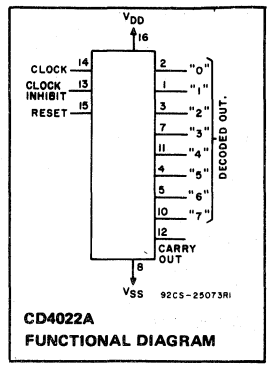
Fig. 9 – Input-leakage-current test circuit.

COS/MOS Divide-By-8 Counter/Divider With 8 Decoded Outputs

The RCA-CD4022A types consist of a 4-stage divide-by-8 Johnson counter, associate decode output gating and a CARRY-OUT BIT. The counter is cleared to its zero count by a high RESET signal. The counter is advanced on the positive CLOCK-signal transition provided the CLOCK INHIBIT signal is low.

Use of the Johnson divide-by-8 counter configuration permits high-speed operation, 2-input decode gating, and spike-free decoder outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The 8 decode gating outputs are normally low and go high only at their respective decoded time slot. Each decode gate output remains high for one full clock cycle. The CARRY-OUT signal completes one cycle every 8 CLOCK-INPUT cycles and is used as a ripple-carry signal to directly clock a succeeding counter package in a multi-package counting system.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).



CD4022A
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): . . . . . −0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max . . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

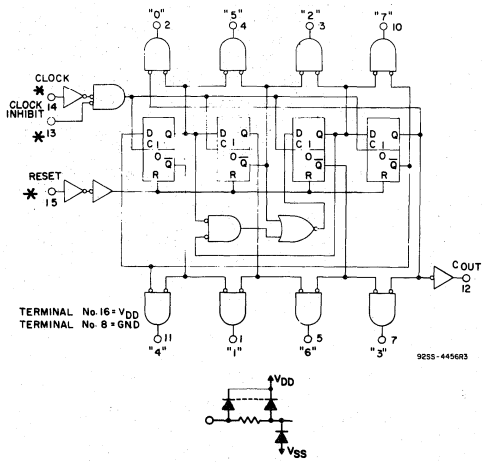
CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D,F,K,H Packages		*E Package*		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Clock Inhibit Setup Time, t_S	5 10	175 75	– –	175 75	– –	ns
Clock Pulse Width, t_W	5 10	500 170	– –	830 250	– –	ns
Clock Input Frequency, f_{CL}	5 10	dc dc	1 3	dc dc	0.6 2	MHz
Clock Rise and Fall Time, t_rCL, t_fCL	5 10	– –	15 15	– –	15 15	μs
Reset Pulse Width	5 10	300 150	– –	600 300	–	ns
Reset Removal Time	5 10	752 225	– –	1000 275	– –	ns

Features:

- **Medium speed operation . . . . 5 MHz (typ.) at $V_{DD} - V_{SS}$ = 10 V**
- **Divide by N counting; N = 2 to 8 with one CD4022A plus one CD4001A package**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Binary counting/decoding**
- **Binary frequency division**
- **Binary counter control/timers**



*ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

Fig. 1 – Logic diagram.

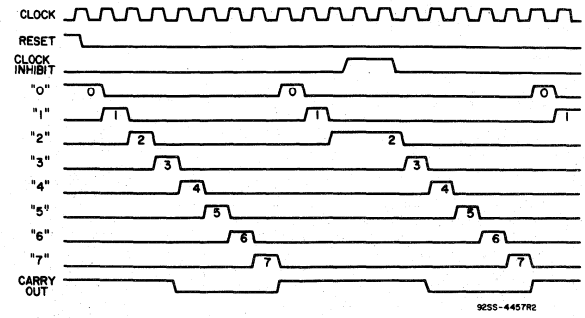


Fig. 2 – Timing diagram.

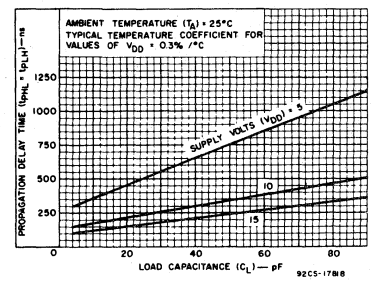


Fig. 3 – Typical propagation delay time vs. load capacitance for decoded outputs.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic		Conditions			Limits at Indicated Temperatures (°C)								Units
					D,K,F,H Packages				E Package				
		V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current I_L Max.		–	–	5	5	0.3	5	300	50	0.5	50	700	μA
		–	–	10	10	0.5	10	600	100	1	100	1400	
		–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low Level V_{OL}		–	5	5	0 Typ.; 0.05 Max.								V
		–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}		–	0	5	4.95 Min.; 5 Typ.								
		–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}		4.2	–	5	1.5 Min.; 2.25 Typ.								V
		9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}		0.8	–	5	1.5 Min.; 2.25 Typ.								
		1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}		4.5	–	5	1 Min.								V
		9	–	10	1 Min.								
Inputs High, V_{NMH}		0.5	–	5	1 Min.								
		1	–	10	1 Min.								
Output Drive Current: n-Channel (Sink) I_{DN} Min.	Decoded Outputs	0.5	–	5	0.062	0.15	0.05	0.036	0.03	0.15	0.025	0.02	mA
		0.5	–	10	0.12	0.3	0.1	0.07	0.06	0.3	0.05	0.04	
	Carry Output	0.5	–	5	0.185	0.5	0.15	0.105	0.095	0.5	0.08	0.065	
		0.5	–	10	0.375	1	0.3	0.21	0.155	1	0.13	0.105	
p-Channel (Source): I_DP Min.	Decoded Outputs	4.5	–	5	-0.038	-0.075	-0.03	-0.021	-0.018	-0.075	-0.015	-0.012	
		9.5	–	10	-0.12	-0.15	-0.1	-0.07	-0.06	-0.15	-0.05	-0.04	
	Carry Output	4.5	–	5	-0.185	-0.4	-0.15	-0.105	-0.095	-0.4	-0.08	-0.065	
		9.5	–	10	-0.375	-0.8	-0.3	-0.21	-0.155	-0.8	-0.13	-0.105	
Input Leakage Current, I_{IL}, I_{IH}		Any Input		15	$\pm 10^{-5}$ Typ., ±1 Max.								μA

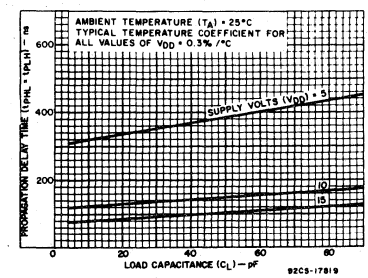


Fig. 4 – Typical propagation delay time vs. load capacitance for carry output.

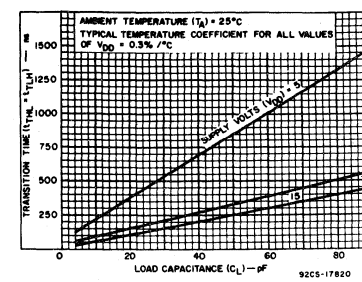


Fig. 5 – Typical transition time vs. load capacitance for decoded outputs.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS D,F,K,H Packages Min.	Typ.	Max.	LIMITS E Package Min.	Typ.	Max.	UNITS
CLOCKED OPERATION								
Propagation Delay Time: t_{PHL}, t_{PLH} Carry-Out Line	5	–	325	1000	–	325	300	ns
	10	–	125	250	–	125	500	
Decode Out Lines	5	–	400	1200	–	400	1600	ns
	10	–	200	400	–	200	800	
Transition Time: t_{THL}, t_{TLH} Carry-Out Line	5	–	85	300	–	85	340	ns
	10	–	50	100	–	50	200	
Decode-Out Lines	5	–	300	900	–	300	1200	ns
	10	–	125	250	–	125	500	
Min. Clock Pulse Width, t_W	5	–	250	500	–	250	830	ns
	10	–	85	170	–	85	250	
Clock Rise and Fall Time, t_{rCL}, t_{fCL}	5	–	–	15	–	–	15	μs
	10	–	–	15	–	–	15	
Min. Clock Inhibit Set-Up Time, t_S	5		175	350		175	700	ns
	10		75	150		75	300	
Max. Clock Input Frequency, f_{CL}*	5	1	2.5	–	0.6	2.5	–	MHz
	10	3	5	–	2	5	–	
Input Capacitance, C_I	Any Input	–	5	–	–	5	–	pF
RESET OPERATION								
Propagation Delay Time: t_{PHL}, t_{PLH} Carry-Out Line	5	–	300	900	–	300	1200	ns
	10	–	125	250	–	125	500	
Decode-Out Line	5	–	500	1250	–	500	2500	ns
	10	–	200	400	–	200	800	
Min. Reset Pulse Width, t_W	5	–	150	300	–	150	600	ns
	10	–	75	150	–	75	300	
Min. Reset Removal Time	5	–	300	752	–	300	1000	ns
	10	–	100	225	–	100	275	

* Measured with respect to carry output line

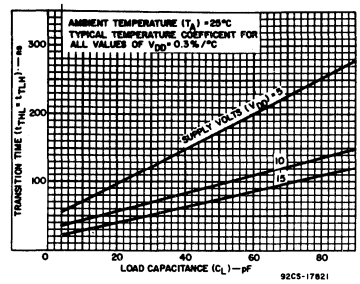


Fig. 6 – Typical transition time vs. load capacitance for carry output.

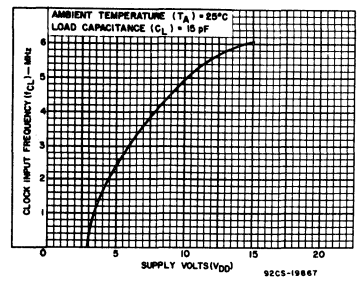


Fig. 7 – Typical clock input frequency vs. supply voltage.

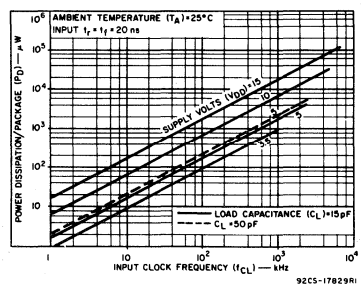


Fig. 8 – Typical dissipation characteristics.

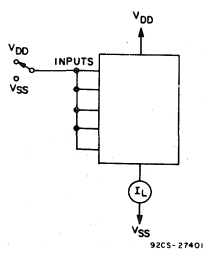


Fig. 9 – Quiescent-device-current test circuit.

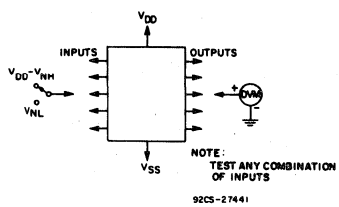


Fig. 10 – Noise-immunity test circuit.

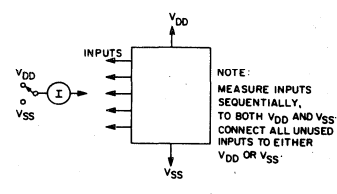


Fig. 11 – Input-leakage-current test circuit.

COS/MOS 7-Stage Binary Counter

With Buffered Reset

The RCA-CD4024A consists of an INPUT PULSE shaping circuit, RESET line driver circuitry, and seven binary counter stages. The counter is reset to "zero" by a high level on the RESET input. Each counter stage is a static master-slave flip-flop. The counter state is advanced one count on the negative-going transition of each INPUT PULSE.

These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

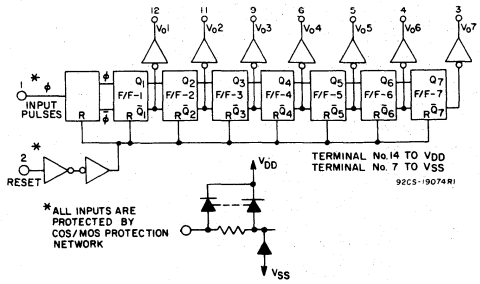
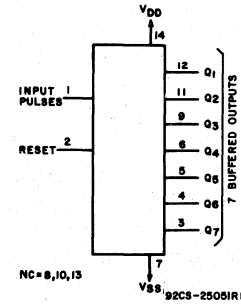


Fig. 1 – Functional diagram for CD4024AD, AE, AF, AK.



Applications:

- **Frequency-dividing circuits**
- **Time-delay circuits**
- **Counter control**
- **D/A counter and switch on one chip**

Features:

- **Medium-speed operation . . . . . 7-MHz (typ.) input pulse rate at $V_{DD} - V_{SS} = 10$ V**
- **Low high-and-low level output impedance . . 700Ω and 500Ω (typ.), respectively at $V_{DD} - V_{SS} = 10$ V**
- **Fully static operation**
- **Common reset**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
PACKAGE TYPE E . . . . . –40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): . . . . . –0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A = –40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = –55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max . . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D,F,K,H Packages		*E Package*		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Clock Pulse Width, t_W	5	330	–	500	–	ns
	10	125	–	165	–	
Clock Input Frequency, f_{CL}	5	dc	1.5	dc	1	MHz
	10	dc	4	dc	3	
Clock Rise or Fall Time, t_rCL, t_fCL	5	15	–	15	–	μs
	10	15	–	15	–	
Reset Pulse Width, t_W	5	500	–	600	–	ns
	10	300	–	350	–	

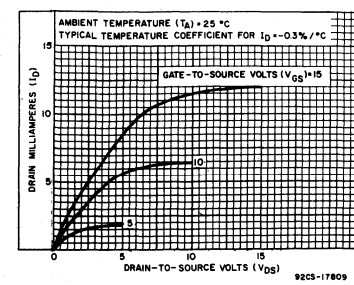
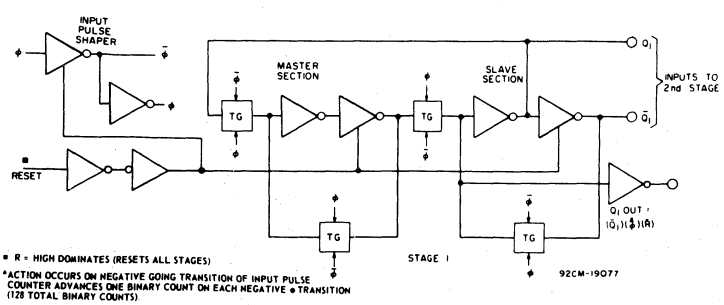


Fig. 2 – Typical output n-channel drain characteristics.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				E Package				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	5	0.3	5	300	50	0.5	50	700	μA
	–	–	10	10	0.5	10	600	100	1	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level, V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: n-Channel (Sink), I_DN Min.	0.5	–	5	0.31	0.5	0.25	0.175	0.15	0.5	0.12	0.095	mA
	0.5	–	10	0.62	1	0.5	0.35	0.31	1	0.25	0.2	
p-Channel (Source) I_DP Min.	4.5	–	5	-0.19	-0.3	-0.15	-0.105	-0.145	-0.3	-0.12	-0.095	
	9.5	–	10	-0.45	-0.7	-0.35	-0.25	-0.31	-0.7	-0.25	-0.2	
Input Leakage Current, I_{IL}, I_{IH}	Any Input –	–	15	$\pm 10^{-5}$ Typ.; ±1 Max.								μA



* R = HIGH DOMINATES (RESETS ALL STAGES)
*ACTION OCCURS ON NEGATIVE GOING TRANSITION OF INPUT PULSE
COUNTER ADVANCES ONE BINARY COUNT ON EACH NEGATIVE ⊕ TRANSITION
(128 TOTAL BINARY COUNTS)

EQUATIONS FOR STAGES 2 TO 7

$Q_{2OUT} = (\bar{Q}_2)(Q_1)(\overset{\blacktriangle}{\oplus})(R)$ $\quad Q_{5OUT} = (\bar{Q}_5)(Q_1)(Q_2)(Q_3)(Q_4)(\overset{\blacktriangle}{\oplus})(\bar{R})$

$Q_{3OUT} = (\bar{Q}_3)(Q_1)(Q_2)(\overset{\blacktriangle}{\oplus})(\bar{R})$ $\quad Q_{6OUT} = (\bar{Q}_6)(Q_1)(Q_2)(Q_3)(Q_4)(Q_5)(\overset{\blacktriangle}{\oplus})(\bar{R})$

$Q_{4OUT} = (\bar{Q}_4)(Q_1)(Q_2)(Q_3)(\overset{\blacktriangle}{\oplus})(\bar{R})$ $\quad Q_{7OUT} = (\bar{Q}_7)(Q_1)(Q_2)(Q_3)(Q_4)(Q_5)(Q_6)(\overset{\blacktriangle}{\oplus})(\bar{R})$

Fig. 6 — Logic block diagram (pulse shaper and 1 binary stage).

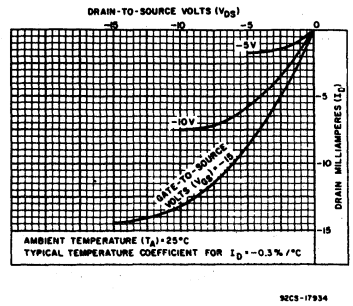


Fig. 3 — Typical output p-channel drain characteristics.

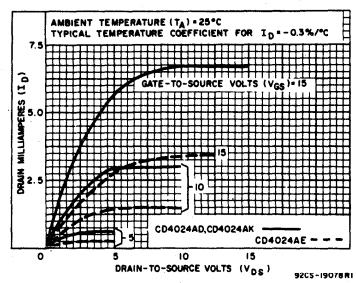


Fig. 4 — Minimum output n-channel drain characteristics.

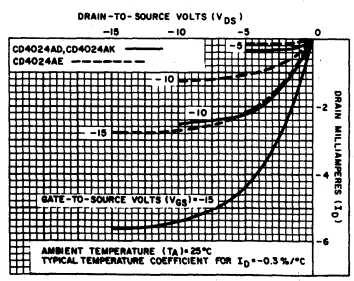


Fig. 5 — Minimum output p-channel drain characteristics.

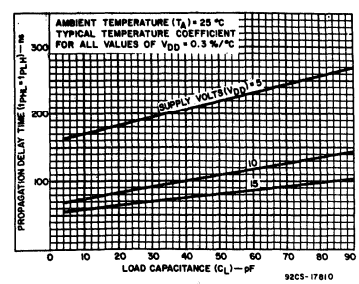


Fig. 7 — Typical propagation delay time vs. C_L.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS D,F,K,H Packages Min.	Typ.	Max.	LIMITS E Package Min.	Typ.	Max.	UNITS
φ INPUT OPERATION								
Propagation Delay Time;* t_{PLH}, t_{PHL}	5	–	175	350	–	175	400	ns
	10	–	80	125	–	80	150	
Transition Time; t_{THL}, t_{TLH}	5	–	175	225	–	175	250	ns
	10	–	80	125	–	80	150	
Maximum Pulse Input Frequency, f_ϕ	5	1.5	2.5	–	1	2.5	–	MHz
	10	4	7	–	3	7	–	
Minimum Input Pulse Width, t_W	5	–	200	330	–	200	500	ns
	10	–	140	125	–	140	165	
Input Pulse Rise & Fall Time, $t_{r\phi}$, $t_{f\phi}$	5	–	–	15	–	–	15	μs
	10	–	–	15	–	–	15	
Average Input Capacitance, C_I	Any Input	–	5	–	–	5	–	pF
RESET OPERATION								
Propagation Delay Time; T_{PLH}, T_{PHL}	5	–	500	700	–	500	800	ns
	10	–	250	350	–	250	400	
Minimum Reset Pulse Width; t_W	5	–	375	500	–	375	600	ns
	10	–	200	300	–	200	350	

* Propagation delay time is from input pulse to Q_1 output.

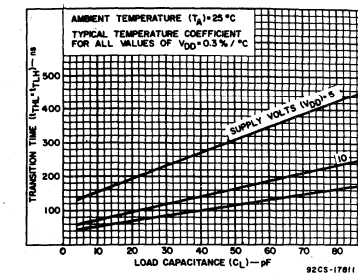


Fig. 8 — Typical transition time vs. C_L.

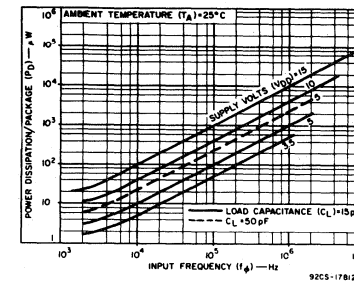


Fig. 9 — Typical dissipation characteristics.

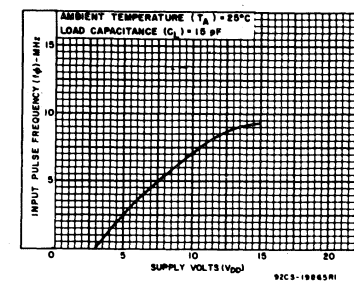


Fig. 10 — Typical input pulse frequency vs. V_{DD}.

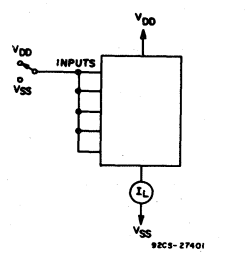


Fig. 11 — Quiescent-device-current test circuit.

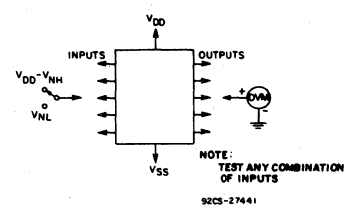


Fig. 12 — Noise-immunity test circuit.

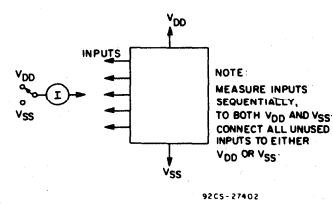


Fig. 13 — Input-leakage-current test circuit.

COS/MOS Decade Counters/Dividers

With Decoded 7-Segment Display Outputs and:
Display Enable – CD4026A
Ripple Blanking – CD4033A

The RCA–CD4026A and CD4033A each consist of a 5-stage Johnson decade counter and an output decoder which converts the Johnson code to a 7-segment decoded output for driving each stage in a numerical display.

These devices are particularly advantageous in display applications where low power dissipation and/or low package count are important.

Inputs common to both types are CLOCK, RESET, & CLOCK INHIBIT; common outputs are CARRY OUT and the seven decoded outputs (a, b, c, d, e, f, g). Additional inputs and outputs for the CD4026A include DISPLAY ENABLE input and DISPLAY ENABLE and UNGATED "C-SEGMENT" outputs. Signals peculiar to the CD4033 are RIPPLE-BLANKING INPUT and LAMP TEST INPUT and a RIPPLE-BLANKING OUTPUT.

A high RESET signal clears the decade counter to its zero count. The counter is advanced one count at the positive clock signal transistion if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. Antilock gating is provided on the Johnson counter, thus assuring proper counting sequence. The CARRY-OUT (C_{out}) signal completes one cycle every ten CLOCK INPUT cycles and is used to clock the succeeding decade directly in a multi-decade counting chain.

The seven decoded outputs (a, b, c, d, e, f, g) illuminate the proper segments in a seven segment display device used for representing the decimal numbers 0 to 9. The 7-segment outputs go high on selection in the CD4033A; in the CD4026A theses outputs go high only when the DISPLAY ENABLE IN is high.

CD4026A

When the DISPLAY ENABLE IN is low the seven decoded outputs are forced low regardless of the state of the counter. Activation of the display only when required results in significant power savings. This system also facilitates implementation of display-character multiplexing.

The CARRY OUT and UNGATED"C-SEGMENT" signals are not gated by the DISPLAY ENABLE and therefore are available continuously. This feature is a requirement in implementation of certain divider functions such as divide-by-60 and divide-by-12.

CD4033A

The CD4033A has provisions for automatic blanking of the non-significant zeros in a multi-digit decimal number which results in an easily readable display consistent with normal writing practice. For example, the number 0050.07000 in an eight digit display would be displayed as 50.07. Zero suppression on the integer side is obtained by connecting the RBI terminal of the CD4033A associated with the most significant digit in the display to a low-level voltage and connecting the RBO terminal of that stage to the RBI terminal of the CD4033A in the next-lower significant position in the display. This procedure is continued for each succeeding CD4033A on the integer side of the display.

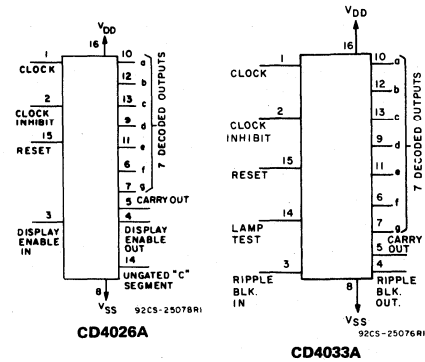
On the fraction side of the display the RBI of the CD4033A associated with the least significant bit is connected to a low level voltage and the RBO of that CD4033A is connected to the RBI terminal of the CD4033A in the next more-significant-bit position. Again, this procedure is continued for all CD4033A's on the fraction side of the display.

In a purely fractional number the zero immediately preceding the decimal point can be displayed by connecting the RBI of that stage to a high level voltage(instead of to the RBO of the next more-significant-stage). For Example: optional zero → 0.7346.

Likewise, the zero in a number such as 763.0 can be displayed by connecting the RBI of the CD4033A associated with it to a high-level voltage.

Ripple blanking of non-significant zeros provides an appreciable savings in display power.

The CD4033A has a LAMP TEST input which, when connected to a high-level voltage, overrides normal decoder operation and enables a check to be made on possible display malfunctions by putting the seven outputs in the high state.



CD4026A CD4033A

FUNCTIONAL DIAGRAMS

Features:

- **Counter and 7-segment decoding in one package**
- **Easily interfaced with 7-segment display types**
- **Fully static counter operation: DC to 2.5 MHz (typ.)**
- **Ideal for low-power displays**
- **Display Enable Output (CD4026A)**
- **"Ripple Blanking" and Lamp Test (CD4033A)**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Decade counting/7-segment decimal display**
- **Frequency division/7-segment decimal displays**
- **Clock/watches/timers (e.g. ÷ 60, ÷ 60, ÷ 12 counter/display)**
- **Counter/display driver for meter applications**

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
PACKAGE TYPE E . . . . . –40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): . . . . . –0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A = –40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = –55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max . . . . . +265°C

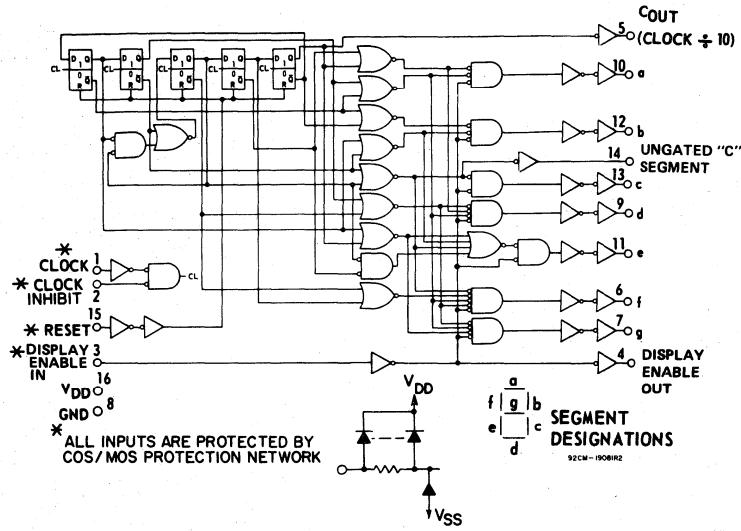


Fig. 1 – CD4026A logic diagram.

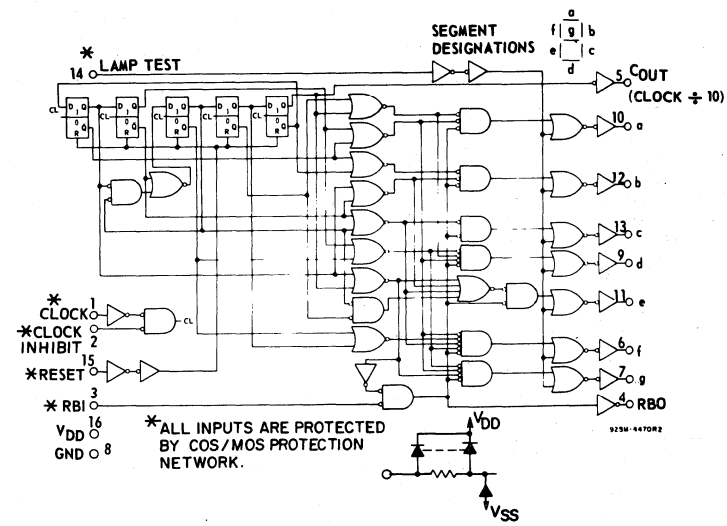


Fig. 3 – CD4033A logic diagram.

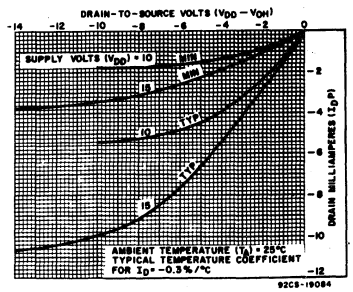


Fig. 6 – Minimum and typical output p-channel decoded drain characteristics @ V_{DD}=10 & 15 V.

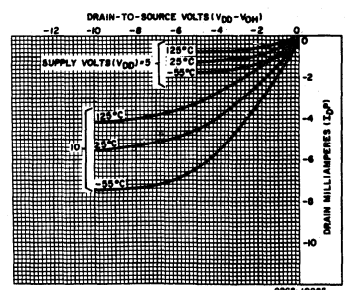


Fig. 7 – Typical output p-channel decoded drain characteristics as a function of temperature.

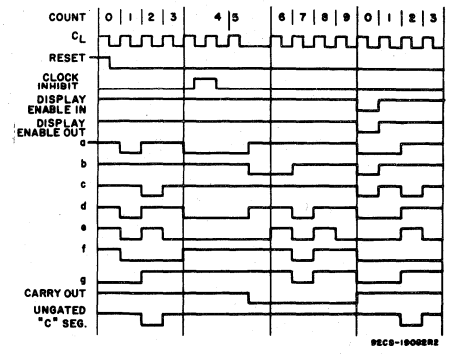


Fig. 2 – CD4026A timing diagram.

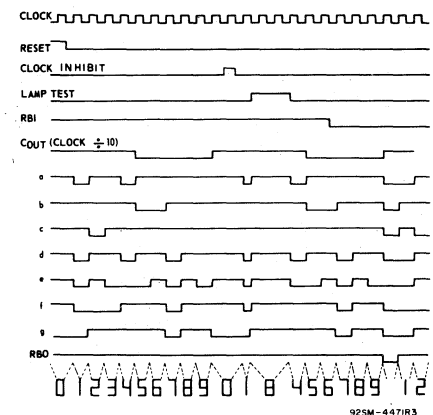


Fig. 4 – CD4033A timing diagram.

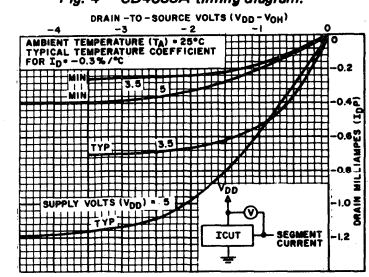


Fig. 5 – Minimum and typical output p-channel decoded drain characteristics @ V_{DD}=3.5 & 5 V.

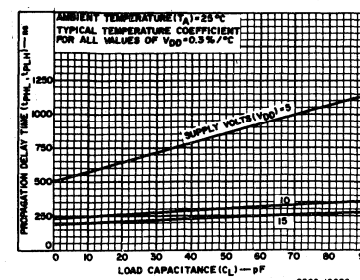


Fig. 8 – Typical propagation delay time vs. C_L for decoded outputs.

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D,F,K,H Packages		*E Package*		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Clock Inhibit Setup Time, t_S	5	500	–	700	–	ns
	10	200	–	300	–	
Clock Pulse Width, t_W	5	330	–	500	–	ns
	10	170	–	250	–	
Clock Input Frequency, f_{CL}	5	dc	1.5	dc	1	MHz
	10	dc	3	dc	2	
Clock Rise or Fall Time, t_rCL, t_fCL	5	–	15	–	15	μs
	10	–	15	–	15	
Reset Pulse Width, t_W	5	330	–	550	–	ns
	10	165	–	250	–	
Reset Removal Time	5	750	–	1000	–	ns
	10	225	–	275	–	

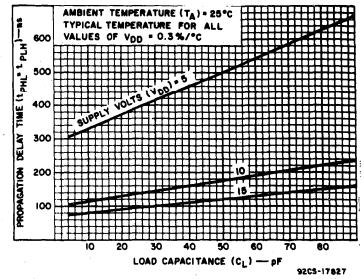


Fig. 9 – Typical propagation delay time vs. C_L for carry outputs.

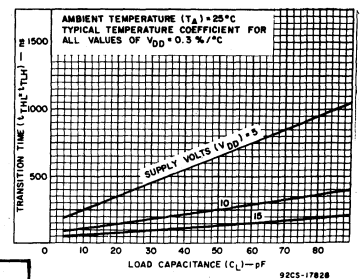


Fig. 10 – Typical transition time vs. C_L for decoded outputs.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic		Conditions			Limits at Indicated Temperatures (°C)								Units
					D,K,F,H Packages				*E Package*				
		V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current I_L Max.		–	–	5	5	0.3	5	300	50	0.5	50	700	μA
		–	–	10	10	0.5	10	600	100	1	100	1400	
		–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}		–	5	5	0 Typ.; 0.05 Max.								V
		–	10	10	0 Typ.; 0.05 Max.								
High Level, V_{OH}		–	0	5	4.95 Min.; 5 Typ.								
		–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}			–	5	1.5 Min.; 2.25 Typ.								V
			–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}			–	5	1.5 Min.; 2.25 Typ.								
				10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}		4.5	–	5	1 Min.								V
		9	–	10	1 Min.								
Inputs High, V_{NMH}		0.5	–	5	1 Min.								
		1	–	10	1 Min.								
Output Drive Current n-Channel (Sink), I_DN Min.	Decoded Outputs	0.5	–	5	0.15	0.24	0.12	0.09	0.08	0.24	0.06	0.05	mA
		0.5	–	10	0.32	0.5	0.25	0.18	0.15	0.5	0.12	0.1	
	Carry Output	0.5	–	5	0.12	0.4	0.15	0.1	0.095	0.4	0.08	0.06	
		0.5	–	10	0.45	1	0.35	0.25	0.3	1	0.25	0.2	
p-Channel (Source), I_DP Min.	Decoded Outputs	4.5	–	5	-0.21	-0.28	-0.14	-0.1	-0.09	-0.28	-0.07	-0.06	
		9.5	–	10	-0.45	-0.6	-0.3	-0.22	-0.2	-0.6	-0.15	-0.13	
	Carry Output	4.5	–	5	-0.12	-0.4	-0.15	-0.1	-0.095	-0.4	-0.08	-0.06	
		9.5	–	10	-0.45	-1	-0.35	-0.25	-0.3	-1	-0.24	-0.2	
Input Leakage Current, I_{IL}, I_{IH}		Any Input –	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								μA

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
			D,F,K,H Packages			*E Package*			
		V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
CLOCKED OPERATION									
Propagation Delay Time; t_{PLH}, t_{PHL} Carry Out Line		5	–	350	1000	–	350	1300	ns
		10	–	125	250	–	125	300	
Decode Out Lines		5	–	600	1700	–	600	2200	ns
		10	–	250	500	–	250	700	
Transition Time; t_{THL}, t_{TLH} Carry Out Line		5	–	100	300	–	100	350	ns
		10	–	50	150	–	50	200	
Decode Out Lines		5	–	300	900	–	300	1200	ns
		10	–	125	350	–	125	450	
Maximum Clock Input Frequency, f_{CL}▲		5	1.5	2.5	–	1	2.5	–	MHz
		10	3	5	–	2	5	–	
Min. Clock Pulse Width, t_W		5	–	200	330	–	200	500	ns
		10	–	100	170	–	100	250	
Clock Rise & Fall Time; t_{rCL}, t_{fCL}		5	–	–	15	–	–	15	μs
		10	–	–	15	–	–	15	
Min. Clock Inhibit Set Up Time, t_S		5	–	175	500	–	175	700	ns
		10	–	75	200	–	75	300	
Average Input Capacitance, C_I	Any Input		–	5	–	–	5	–	pF
RESET OPERATION									
Propagation Delay Time: t_{PLH}, t_{PHL} To Carry Out Line		5	–	350	1000	–	350	1300	ns
		10	–	125	250	–	125	300	
To Decode Out Lines		5	–	550	1400	–	550	1900	ns
		10	–	240	500	–	240	600	
Min. Reset Pulse Width t_W		5	–	200	330	–	200	500	ns
		10	–	100	165	–	100	250	
Min. Reset Removal Time		5	–	300	750	–	300	1000	ns
		10	–	100	225	–	100	275	

▲ Measured with respect to carry out line.

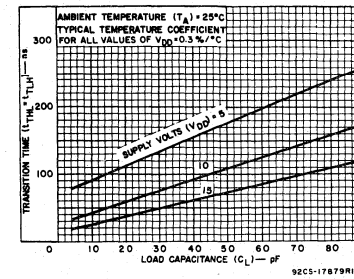


Fig. 11 – Typical transition time vs. C_L for carry output.

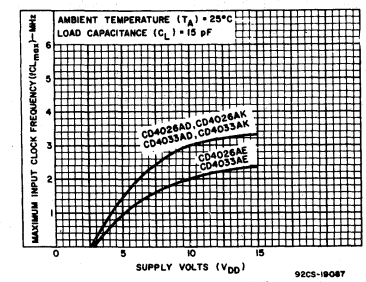


Fig. 12 – Maximum input clock frequency vs. V_{DD}.

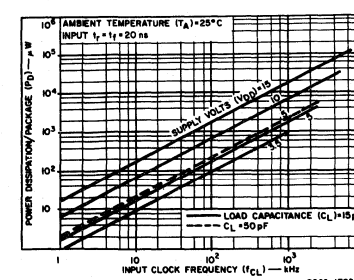


Fig. 13 – Typical dissipation characteristics.

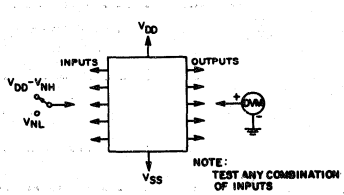


Fig. 14 – Noise immunity test circuit.

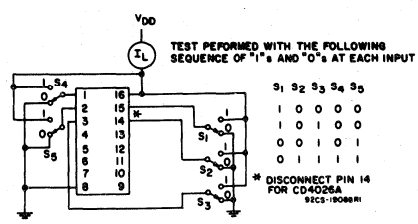


Fig. 15 – Quiescent-device-current test circuit.

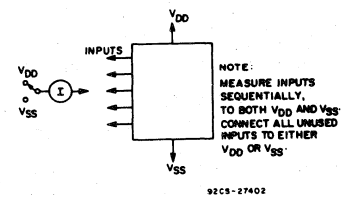
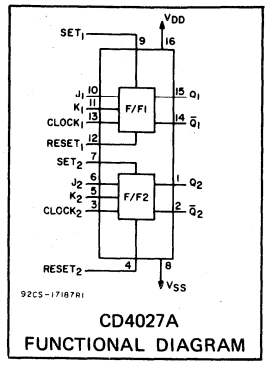


Fig. 16 – Input-leakage-current test circuit.

COS/MOS Dual J-K Master-Slave Flip-Flop

The RCA-CD4027A is a single monolithic chip integrated circuit containing two identical complementary-symmetry J-K master-slave flip-flops. Each flip-flop has provisions for individual J, K, Set, Reset, and Clock input signals. Buffered Q and $\overline{Q}$ signals are provided as outputs. This input-output arrangement provides for compatible operation with the RCA-CD4013A dual D-type flip-flop.

The CD4027A is useful in performing control, register, and toggle functions. Logic levels present at the J and K inputs along with internal self-steering control the state of each flip-flop; changes in the flip-flop state are synchronous with the positive-going transition of the clock pulse. Set and reset functions are independent of the clock and are initiated when a high level signal is present at either the Set or Reset input.



CD4027A
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . -65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H. . . . . -55 to +125°C

PACKAGE TYPE E . . . . . -40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal): . . . . . -0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = -40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = -55 to +100°C (PACKAGE TYPES D, F, K). . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K). . . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . -0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS *at T_A = 25°C, Except as Noted.*
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, K, H PACKAGES		E PACKAGE		
		MIN.	MAX.	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Data Setup Time, t_S	5	150	—	200	—	ns
	10	50	—	75	—	
Clock Pulse Width, t_W	5	330	—	500	—	ns
	10	110	—	165	—	
Clock Input Frequency (Toggle Mode) f_{CL}	5	dc	1.5	dc	1	MHz
	10		4.5		3	
Clock Rise or Fall Time, t_rCL,* t_fCL	5	—	15	—	15	μs
	10	—	5	—	5	
Set or Reset Pulse Width, t_W	5	200	—	300	—	ns
	10	80	—	120	—	

*If more than one unit is cascaded in a parallel clocked operation, t_rCL should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- Set-Reset capability
- Static flip-flop operation—retains state indefinitely with clock level either "high" or "low"
- Medium-speed operation—10 MHz (typ.) clock toggle rate at 10V
- Quiescent current specified to 15 V
- Maximum input leakage of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications

- Registers, counters, control circuits

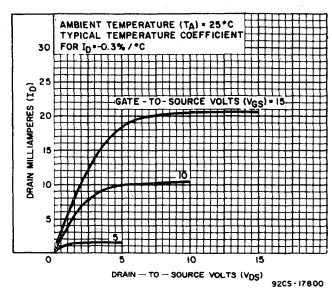
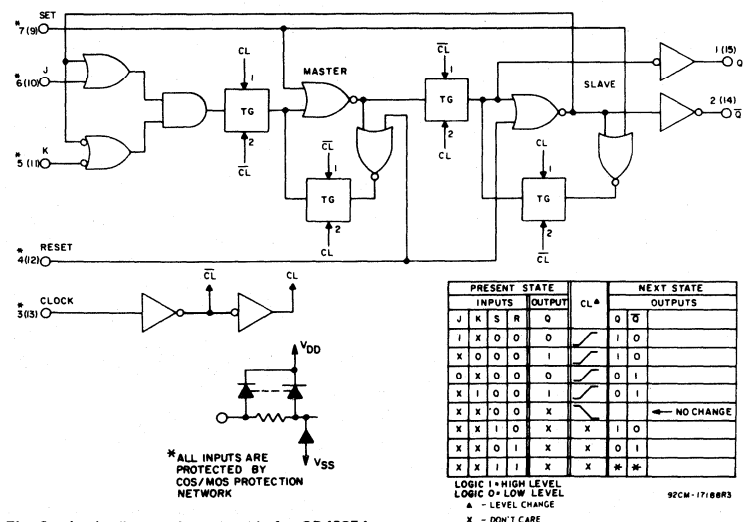


Fig. 1 — Typical n-channel drain characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
				D, K, F, H PACKAGES				E PACKAGE				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	+25 TYP.	+25 LIMIT	+125	-40	+25 TYP.	+25 LIMIT	+85	
Quiescent Device Current, I_L Max.			5	1	0.005	1	60	10	0.01	10	140	μA
			10	2	0.005	2	120	20	0.05	20	280	
			15	25	0.5	25	1000	250	2.5	250	2500	
Output Voltage: Low Level, V_{OL}	–	0.5	5	0 Typ.; 0.05 Max								V
	–	0.10	10	0 Typ.; 0.05 Max								
High Level V_{OH}	–	0.5	5	5 Typ.; 4.95 Min.								
	–	0.10	10	10 Typ.; 9.95 Min.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	2.25 Typ.; 1.5 Min.								V
	9	–	10	4.5 Typ.; 3 Min.								
Inputs High V_{NH}	0.8	–	5	2.25 Typ.; 1.5 Min.								
	1	–	10	4.5 Typ.; 3 Min.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N Channel (Sink), I_DN Min.	0.5	–	5	0.65	1	0.5	0.35	0.35	1	0.3	0.24	mA
	0.5	–	10	1.25	2.5	1	0.75	0.72	2.5	0.6	0.5	
P-Channel (Source): I_DP Min.	4.5	–	5	–0.31	–0.5	–0.25	–0.175	–0.17	–0.5	–0.14	–0.12	
	9.5	–	10	–0.8	–1.3	–0.65	–0.45	–0.4	–1.3	–0.33	–0.27	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		15	$\pm 10^{-5}$ Typ., ±1 Max.								μA



PRESENT STATE						NEXT STATE	
INPUTS				OUTPUT	CL▲	OUTPUTS	
J	K	S	R	Q		Q	Q̄
1	X	0	0	0		1	0
X	0	0	0	1		1	0
0	X	0	0	0		0	1
X	1	0	0	1		0	1
X	X	0	0	X			← NO CHANGE
X	X	1	0	X	X	1	0
X	X	0	1	X	X	0	1
X	X	1	1	X	X	*	*

LOGIC 1 = HIGH LEVEL
LOGIC 0 = LOW LEVEL
▲ – LEVEL CHANGE
X – DON'T CARE

92CM-17168R3

Fig. 2 – Logic diagram & truth table for CD4027A (one of two identical J-K flip flops).

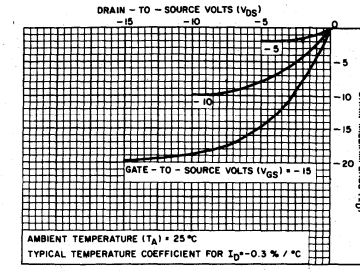


Fig. 3 – Typical p-channel drain characteristics.

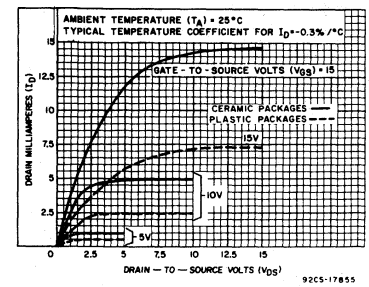


Fig. 4 – Minimum n-channel drain characteristics.

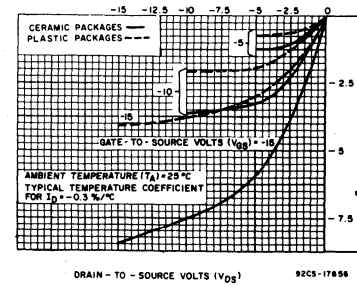


Fig. 5 – Minimum p-channel drain characteristics.

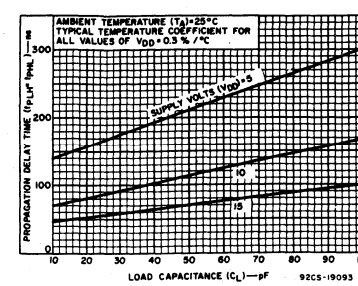


Fig. 6 – Typical propagation delay time vs. C_L.

DYNAMIC ELECTRICAL CHARACTERISTICS
at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS						UNITS
		D, F, K, H PACKAGES			E PACKAGE			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Propagation Delay Time: Clock to Q or $\overline{Q}$ Outputs t_{PHL}, t_{PLH}	5	–	150	300	–	150	400	ns
	10	–	75	110	–	75	150	
Set to Q or Reset to $\overline{Q}$, t_{PLH}	5	–	175	225	–	175	350	ns
	10	–	75	110	–	75	150	
Set to $\overline{Q}$ or Reset to Q, t_{PHL}	5	–	175	225	–	175	350	ns
	10	–	75	110	–	75	150	
Transition Time t_{THL}, t_{TLH}	5	–	75	125	–	75	250	ns
	10	–	50	70	–	50	140	
Maximum Clock Input Frequency (Toggle Mode) f_{CL}	5	1.5	3	–	1	3	–	MHz
	10	4.5	8	–	3	8	–	
Minimum Clock Pulse Width, t_W	5	–	165	330	–	165	500	ns
	10	–	65	110	–	65	165	
Minimum Set or Reset Pulse Width, t_W	5	–	125	200	–	125	300	ns
	10	–	50	80	–	50	120	
Minimum Data Setup Time, t_S	5	–	70	150	–	70	200	ns
	10	–	25	50	–	25	75	
Clock Rise or Fall Time, t_{rCL}, t_{fCL}	5	–	–	15	–	–	15	us
	10	–	–	5	–	–	5	
Average Input Capacitance, C_I	Any Input	–	5	–	–	5	–	pF

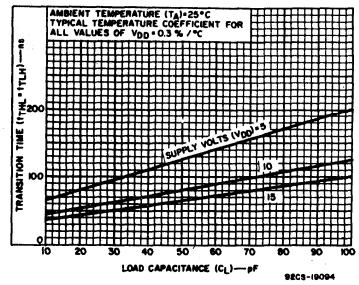


Fig.7 – Typical transition time vs. C_L.

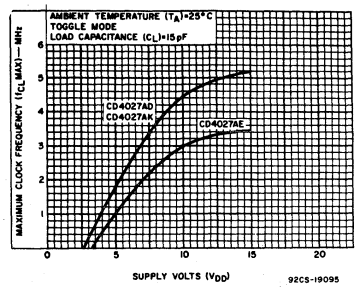


Fig.8 – Typical maximum clock input frequency vs. supply voltage.

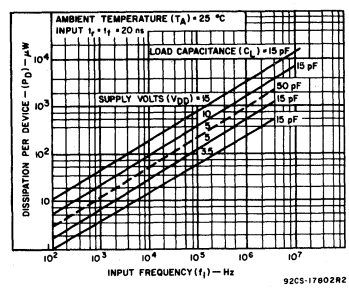


Fig.9 – Typical dissipation characteristics.

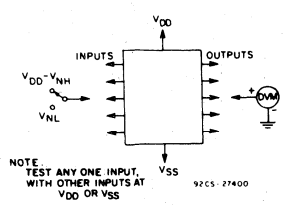


Fig. 10 – Noise immunity test circuit.

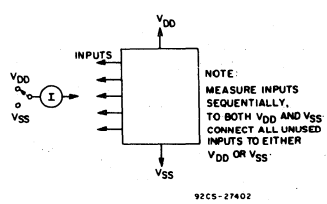


Fig. 11 – Input leakage current test circuit.

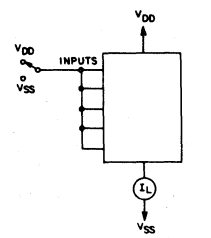
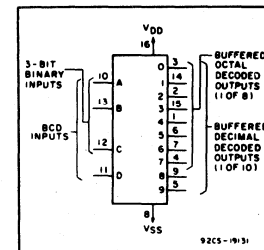


Fig. 12 – Quiescent device current test circuit.

COS/MOS
BCD-to-Decimal Decoder

The RCA-CD4028A types are BCD-to-decimal or binary-to-octal decoders consisting of pulse-shaping circuits on all 4 inputs, decoding-logic gates, and 10 output buffers. A BCD code applied to the four inputs, A to D, results in a high level at the selected one of 10 decimal decoded outputs. Similarly, a 3-bit binary code applied to inputs A through C is decoded in octal code at output 0 to 7. A high-level signal at the D input inhibits octal decoding and causes outputs 0 through 7 to go low. If unused, the D input must be connected to V_{SS}. High drive capability is provided at all outputs to enhance dc and dynamic performance in high fan-out applications.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).



CD4028A
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C

PACKAGE TYPE E . . . . . –40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages references to V_{SS} Terminal) . . . . . –0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = –40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = –55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, K, H PACKAGES		E PACKAGE		
		MIN.	MAX.	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)		3	12	3	12	V

Features:

- **BCD-to-decimal decoding or binary-to-octal decoding**
- **High decoded output drive capability. . . . . 8 mA (typ.) sink or source**
- **"Positive logic" inputs and outputs. . . . . decoded outputs go high on selection**
- **Medium-speed operation . . . . . t_{THL}, t_{TLH} = 30 ns (typ.) @ V_{DD} = 10 V**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Code conversion**
- **Address decoding—memory selection control**
- **Indicator-tube decoder**

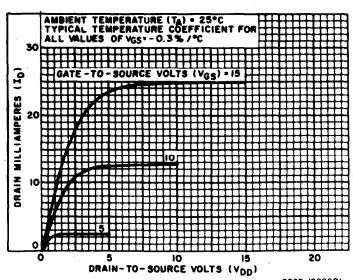


Fig. 1 — Typical output n-channel drain characteristics.

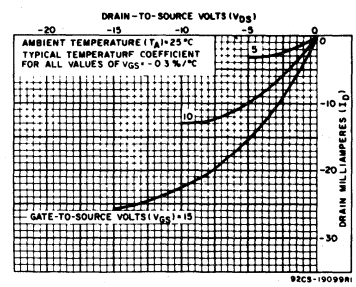


Fig. 2 — Typical output p-channel drain characteristics.

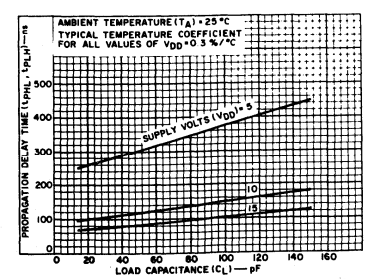


Fig. 3 — Typical propagation delay time vs. C_L.

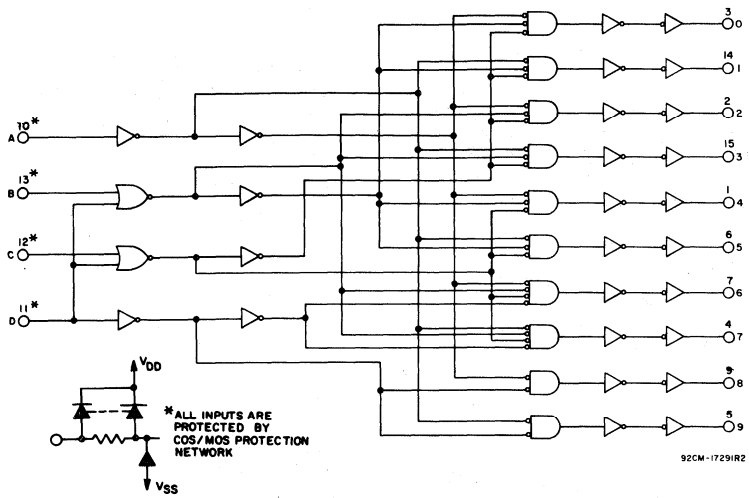


Fig. 4 – Logic diagram.

TABLE I – TRUTH TABLE

D	C	B	A	0	1	2	3	4	5	6	7	8	9	
0	0	0	0	1	0	0	0	0	0	0	0	0	0	*
0	0	0	1	0	1	0	0	0	0	0	0	0	0	
0	0	1	0	0	0	1	0	0	0	0	0	0	0	
0	0	1	1	0	0	0	1	0	0	0	0	0	0	
0	1	0	0	0	0	0	0	1	0	0	0	0	0	
0	1	0	1	0	0	0	0	0	1	0	0	0	0	
0	1	1	0	0	0	0	0	0	0	1	0	0	0	
0	1	1	1	0	0	0	0	0	0	0	1	0	0	
1	0	0	0	0	0	0	0	0	0	0	0	1	0	
1	0	0	1	0	0	0	0	0	0	0	0	0	1	
1	0	1	0	0	0	0	0	0	0	0	0	1	0	**
1	0	1	1	0	0	0	0	0	0	0	0	0	1	
1	1	0	0	0	0	0	0	0	0	0	0	1	0	
1	1	0	1	0	0	0	0	0	0	0	0	0	1	
1	1	1	0	0	0	0	0	0	0	0	0	1	0	
1	1	1	1	0	0	0	0	0	0	0	0	0	1	

* WHERE 1 = HIGH LEVEL
0 = LOW LEVEL

** EXTRAORDINARY STATES

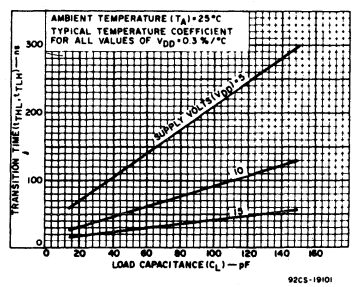


Fig. 5 – Typical transition time vs. C_L.

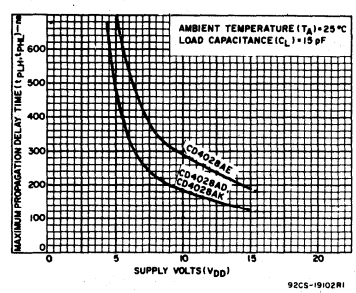


Fig. 6 – Maximum propagation delay time vs. V_{DD}.

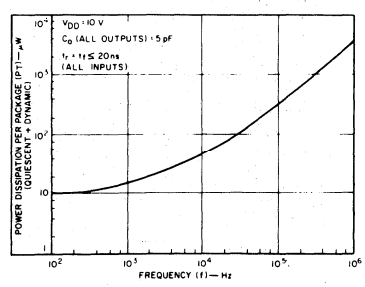


Fig. 7 – Dissipation vs. input frequency.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
				D, K, F, H PACKAGES				E PACKAGE				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	+25 TYP.	+25 LIMIT	+125	-40	+25 TYP.	+25 LIMIT	+85	
Quiescent Device Current, I_L Max.	–	–	5	5	0.5	5	300	50	5	50	700	µA
	–	–	10	10	1	10	600	100	10	100	1400	
	–	–	15	50	1	50	2000	500	10	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4 2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current N-Channel (Sink), I_{DN} Min.	0.5	–	5	0.75	1.2	0.6	0.45	0.35	1.2	0.3	0.25	mA
	0.5	–	10	1.5	2.4	1.2	0.9	0.7	2.4	0.6	0.5	
P-Channel (Source), I_DP Min.	4.5	–	5	-0.7	-0.9	-0.45	-0.32	-0.32	-0.9	-0.22	-0.18	
	9	–	10	-1.4	-1.9	-0.95	-0.65	-0.65	-1.9	-0.48	-0.4	
Input Leakage Current, I_{IL}, I_{IH}	Any Input –	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								µA

DYNAMIC ELECTRICAL CHARACTERISTICS

at $T_A = 25^oC$, Input t_r, $t_f = 20$ ns, $C_L = 15$ pF, $R_L = 200$ kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS D, F, K, H PACKAGES MIN.	TYP.	MAX.	LIMITS E PACKAGE MIN.	TYP.	MAX.	UNITS
Propagation Delay Time; t_{PLH}, t_{PHL}	5	–	250	480	–	250	700	ns
	10	–	100	180	–	100	290	
Transition Time; t_{THL}, t_{TLH}	5	–	60	150	–	60	300	ns
	10	–	30	75	–	30	150	
Average Input Capacitance, C_I	Any Input	–	5	–	–	5	–	pF

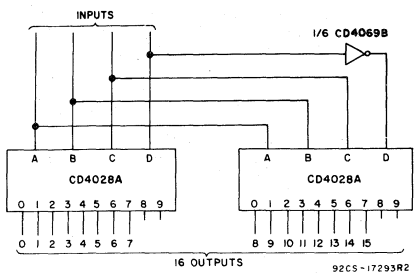
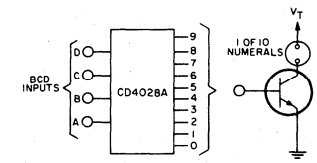


Fig. 8 – Code conversion circuit.

The circuit shown in Fig. 9 converts any 4-bit code to a decimal or hexadecimal code. Table 2 shows a number of codes and the decimal or hexadecimal number in these codes which must be applied to the input terminals of the CD4028A to select a particular output. For example: in order to get a high on output No. 8 the input must be either an 8 expressed in 4-Bit Binary code, a 15 expressed in 4-Bit Gray code, or a 5 expressed in Excess-3 code.



▲ (Trademark) Burroughs Corp.

TUBE REQUIREMENTS:

Type	V_T (Vdc)	mA/numeral
Burroughs B4081	170	1.4
B4336/718	170	2
B4032	170	1.4
B4021	120	1.4

TRANSISTOR CHARACTERISTICS

Leakage with transistor cutoff ≤ 0.05mA

$V_{(BR)CEO}$ ≥ 70V

Fig. 9 – Neon readout (Nixie Tube▲) display application.

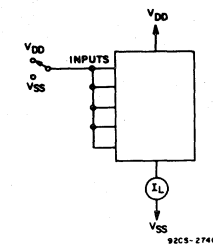


Fig. 10 – Quiescent-device-current test circuit.

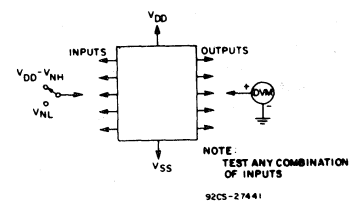


Fig. 11 – Noise-immunity test circuit.

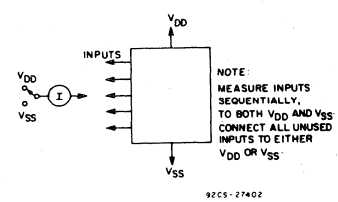


Fig. 12 – Input-leakage-current test circuit.

TABLE II – CODE CONVERSION CHART

INPUTS D	C	B	A	INPUT CODES Hexa-Decimal 4-BIT BINARY	4-BIT GRAY	Decimal EXCESS-3	EXCESS-3 GRAY	AIKEN	4-2-2-1	OUTPUT NUMBER 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0			0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	1			1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	2	3		0	2	2	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	3	2	0	3	3		0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	4	7	1	4	4		0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	5	6	2			3	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	1	1	0	6	4	3	1		4	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	1	1	1	7	5	4	2			0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	0	8	15	5				0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	9	14	6			5	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
1	0	1	0	10	12	7	9		6	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
1	0	1	1	11	13	8		5		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1	1	0	0	12	8	9	5	6		0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
1	1	0	1	13	9		6	7	7	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
1	1	1	0	14	11		8	8	8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	1	1	1	15	10		7	9	9	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

COS/MOS Presettable Up/Down Counter

Binary or BCD-Decade

The RCA-CD4029A consists of a four-stage binary or BCD-decade up/down counter with provisions for look-ahead carry in both counting modes. The inputs consist of a single CLOCK, CARRY-IN (CLOCK INHIBIT), BINARY/DECADE, UP/DOWN, PRESET ENABLE, and four individual JAM signals and a CARRY OUT signal are provided as outputs.

A high PRESET ENABLE signal allows information on the JAM INPUTS to preset the counter to any state asynchronously with the clock. A low on each JAM line, when the PRESET-ENABLE signal is high, resets the counter to its zero count. The counter is advanced one count at the positive transition of the clock when the CARRY-IN and PRESET ENABLE signals are low. Advancement is inhibited when the CARRY-IN or PRESET ENABLE signals are high. The CARRY-OUT signal is normally high and goes low when the counter reaches its maximum count in the UP mode or the minimum count in the DOWN mode provided the CARRY-IN signal is low. The CARRY-IN signal in the high state can thus be considered a CLOCK INHIBIT. The CARRY-IN terminal must be connected to V_{SS} when not in use.

Binary counting is accomplished when the BINARY/DECADE input is high; the counter counts in the decade mode when the BINARY/DECADE input is low. The counter counts Up when the UP/DOWN INPUT is high, and Down when the UP/DOWN INPUT is low. Multiple packages can be connected in either a parallel-clocking or a ripple-clocking arrangement as shown in Fig. 13.

Parallel clocking provides synchronous control and hence faster response from all counting outputs. Ripple-clocking allows for longer clock input rise and fall times.

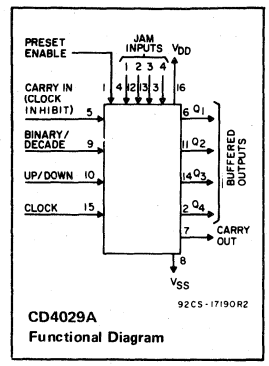
These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- **Medium speed operation . . . 5 MHz (typ.) @ C_L=15 pF and $V_{DD}-V_{SS}$=10 V**
- **Multi-package parallel clocking for synchronous high speed output response or ripple clocking for slow clock input rise and fall times**
- **"Preset Enable" and individual "Jam" inputs provided**
- **Binary or decade up/down counting**
- **BCD outputs in decade mode**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Programmable binary and decade counting/frequency synthesizers-BCD output**
- **Analog to digital and digital to analog conversion**
- **Up/Down binary counting**
- **Magnitude and sign generation**
- **Up/Down decade counting**
- **Difference counting**



CD4029A
Functional Diagram

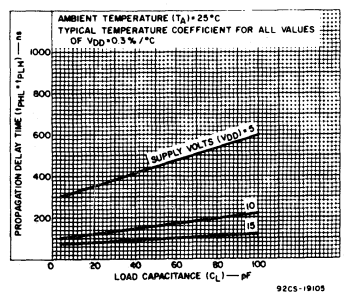


Fig. 1— Typical propagation delay time vs. C_L for Q outputs.

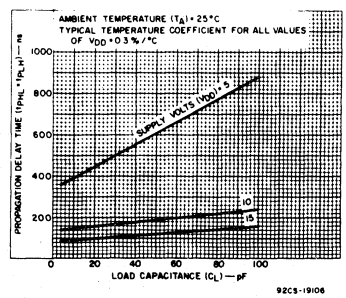


Fig. 2— Typical propagation delay time vs. C_L for carry output.

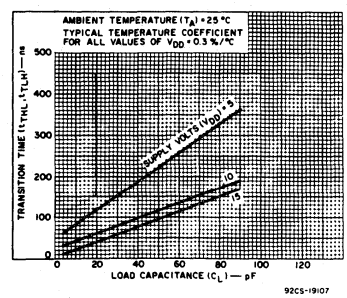


Fig. 3— Typical transition time vs. C_L for Q outputs.

RECOMMENDED OPERATING CONDITIONS at T_A=25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS D,F,K,H Packages Min.	LIMITS D,F,K,H Packages Max.	LIMITS E Package Min.	LIMITS E Package Max.	UNITS
Supply-Voltage Range (For T_A=Full Package-Temperature Range)		3	12	3	12	V
Setup Time, t_S*	5	650	–	1300	–	ns
	10	230	–	460	–	
Clock Pulse Width, t_W	5	340	–	500	–	ns
	10	170	–	250	–	
Clock Input Frequency, f_{CL}	5	dc	1.5	dc	1	MHz
	10	dc	3	dc	2	
Clock Rise or Fall Time, t_rCL,t_fCL**	5	–	15	–	15	μs
	10	–	15	–	15	
Preset Enable Pulse Width, t_W	5	330	–	660	–	ns
	10	160	–	320	–	

*From Up/Down, Binary/Decode, Carry In, or Preset Enable Control Inputs to Clock Edge.

**If more than one unit is cascaded in the parallel clocked application, t_rCL should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transition time of the carry output driving stage for the estimated capacitive load.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) ..... −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):
- PACKAGE TYPES D,F,K,H ..... −55 to +125°C
- PACKAGE TYPE E ..... −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... −0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D):
- FOR T_A=−40 to +60°C (PACKAGE TYPE E) ..... 500 mW
- FOR T_A=+60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
- FOR T_A=−55 to +100°C (PACKAGE TYPES D,F,K) ..... 500 mW
- FOR T_A=+100 to +125°C (PACKAGE TYPES D,F,K) ..... Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
- FOR T_A=FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) ..... 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):
- At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C, Input t_r,t_f=20 ns, C_L=15 pF, R_L=200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS D,F,K,H Packages Min.	D,F,K,H Typ.	D,F,K,H Max.	E Package Min.	E Typ.	E Max.	UNITS
Clocked Operation								
Propagation Delay Time: t_{PHL}, t_{PLH} Q Outputs	5	–	325	650	–	325	1300	ns
	10	–	115	230	–	115	460	
Carry Output	5	–	425	850	–	425	1700	
	10	–	150	300	–	150	600	
Transition Time: t_{THL}, t_{TLH} Q Outputs	5	–	100	200	–	100	400	ns
	10	–	50	100	–	50	200	
Carry Output	5	–	200	400	–	200	800	
	10	–	100	200	–	100	400	
Minimum Clock Pulse Width, t_W	5	–	200	340	–	200	500	ns
	10	–	100	170	–	100	250	
Clock Rise & Fall Time, t_rCL, t_fCL**	5	–	–	15	–	–	15	μs
	10	–	–	15	–	–	15	
Minimum Setup Times, t_S*	5	–	325	650	–	325	1300	ns
	10	–	115	230	–	115	460	
Maximum Clock Input Frequency, f_{CL}	5	1.5	2.5	–	1	2.5	–	MHz
	10	3	5	–	2	5	–	
Input Capacitance, C_I	Any Input	–	5	–	–	5	–	pF
Preset Enable								
Propagation Delay Time: t_{PHL}, t_{PLH} Q Outputs	5	–	325	650	–	325	1300	ns
	10	–	115	230	–	115	460	
Carry Output	5	–	425	850	–	425	1700	
	10	–	150	300	–	150	600	
Minimum Preset Enable Pulse Width, t_W	5	–	115	330	–	115	660	ns
	10	–	80	160	–	80	320	
Minimum Preset Enable Removal Time	5	–	325	650	–	325	1300	ns
	10	–	115	230	–	115	460	
Carry Input								
Propagation Delay Time: t_{PHL}, t_{PLH} Carry Output	5	–	175	350	–	175	700	ns
	10	–	50	100	–	50	200	

For footnotes, see Recommended Operating Conditions.

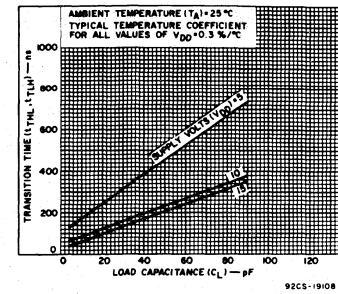


Fig. 4—Typical transition time vs. C_L for carry output.

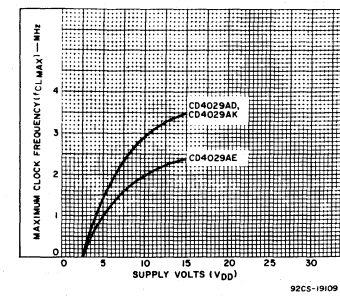


Fig. 5—Maximum clock input frequency vs. V_{DD}.

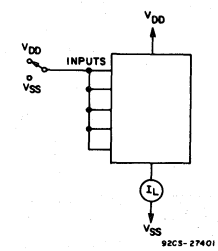


Fig. 6—Quiescent-device-current test circuit.

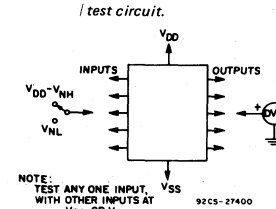


Fig. 7—Noise-immunity test circuit.

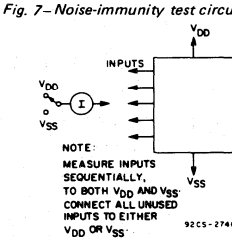


Fig. 8—Input-leakage-current test circuit.

CD4029A Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				E Package				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	5	0.3	5	300	50	0.5	50	700	μA
	–	–	10	10	0.5	10	600	100	1	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High-Level, V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink), I_DN Min. Q Outputs	0.5	–	5	0.5	0.8	0.4	0.28	0.24	0.8	0.2	0.16	mA
	0.5	–	10	0.74	1.2	0.6	0.42	0.36	1.2	0.3	0.24	
Carry Output	0.5	–	5	0.1	0.16	0.08	0.06	0.05	0.16	0.04	0.03	
	0.5	–	10	0.4	0.64	0.32	0.22	0.19	0.64	0.16	0.13	
P-Channel (Source), I_DP Min. Q Outputs	4.5	–	5	−0.18	−0.24	−0.12	−0.08	−0.07	−0.24	−0.06	−0.05	
	9.5	–	10	−0.3	−0.4	−0.2	−0.14	−0.14	−0.4	−0.1	−0.08	
Carry Output	4.5	–	5	−0.09	−0.12	−0.06	−0.04	−0.04	−0.12	−0.03	−0.02	
	9.5	–	10	−0.15	−0.2	−0.1	−0.07	−0.07	−0.2	−0.05	−0.04	
Input Leakage Current, I_{IL}, I_{IH}	Any Input	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								μA

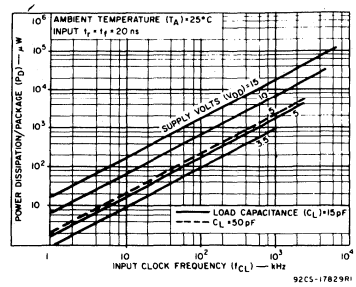


Fig. 9—Typical dissipation characteristics.

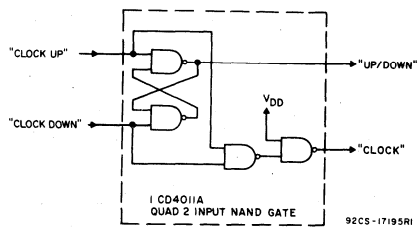


Fig. 10—Conversion of clock up, clock down input signals to clock and up/down input signals.

The CD4029A CLOCK and UP/DOWN inputs are used directly in most applications. In applications where CLOCK UP and CLOCK DOWN inputs are provided, conversion to the CD4029A CLOCK and UP/DOWN inputs can easily be realized by use of the circuit shown below.

CD4029A changes count on positive transitions of CLOCK UP or CLOCK DOWN inputs. For the gate configuration shown below, when counting up the CLOCK DOWN input must be maintained high and conversely when counting down the CLOCK UP input must be maintained high.

* TRUTH TABLE FOR F-F No 1

CLOCK	TE	PE	J	Q	$\bar{Q}$
X	X	0	0	0	1
↓	1	1	X	$\bar{Q}$	Q
X	X	0	1	1	Q
↓	0	1	X	Q	$\bar{Q}$ NC
↑	X	1	X	Q	$\bar{Q}$ NC

NC-NO CHANGE TE-TOGGLE ENABLE

** TRUTH TABLE FOR F-F'S 2,3,4

CLOCK	TE	PE	J	Q	$\bar{Q}$
X	X	0	0	0	1
↓	0	1	X	$\bar{Q}$	Q
X	X	0	1	1	0
↓	1	1	X	Q	$\bar{Q}$ NC
↑	X	1	X	Q	$\bar{Q}$ NC

Y-DON'T CARE

CONTROL INPUT	LOGIC LEVEL	ACTION
BIN/DEC (B/D)	1	BINARY COUNT
	0	DECADE COUNT
UP/DOWN (U/D)	1	UP COUNT
	0	DOWN COUNT
PRESET ENABLE (PE)	1	JAM IN
	0	NO JAM
CARRY IN (CI) (CLOCK INHIBIT)	1	NO COUNTER ADVANCE AT POS CLOCK TRANSITION
	0	ADVANCE COUNTER AT POS CLOCK TRANSITION

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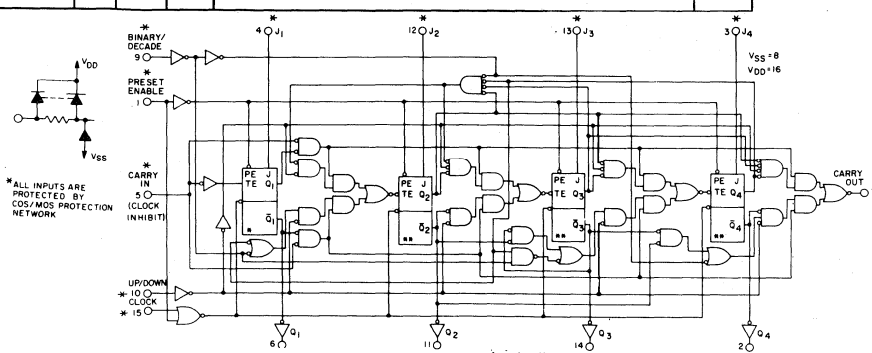
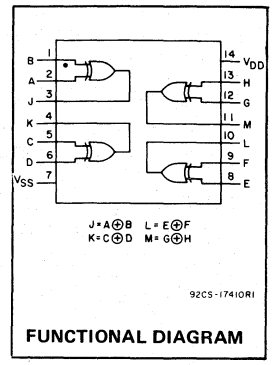


Fig. 11 – Logic diagram.

COS/MOS
Quad Exclusive-OR Gate

The RCA-CD4030A types consist of four independent Exclusive-OR gates integrated on a single monolithic silicon chip. Each Exclusive-OR gate consists of four n-channel and four p-channel enhancement-type transistors. All inputs and outputs are protected against electrostatic effects.

These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).



FUNCTIONAL DIAGRAM

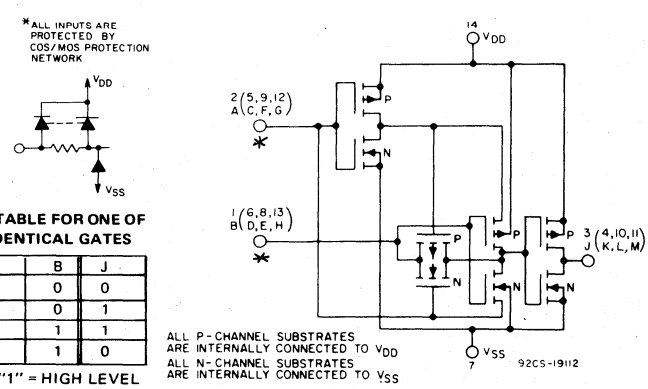
MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg})	−65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A)	
PACKAGE TYPES D, F, K, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)	
FOR T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K)	500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING) At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max	+265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C,

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	D,F,K,H Packages		E Package		
	Min.	Max.	Min.	Max.	
Supply Voltage Range (For T_A = Full Package Temperature Range)	3	12	3	12	V



TRUTH TABLE FOR ONE OF FOUR IDENTICAL GATES

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

WHERE "1" = HIGH LEVEL
"0" = LOW LEVEL

Fig.1 — Schematic diagram for 1 of 4 identical exclusive-OR gates.

For quiescent device current, noise immunity, and input leakage current test circuits see "Ratings and Characteristics" at the beginning of the COS/MOS section.

Features:

- **Medium speed operation. . .**
  . . . $t_{PHL} = t_{PLH}$ = 40 ns (typ.) @ C_L = 15 pF and $V_{DD}-V_{SS}$ = 10 V
- **Low output impedance. . .**
  . . . 500 Ω (typ.) @ $V_{DD}-V_{SS}$ = 10 V
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (Full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Even and odd-parity generators and checkers**
- **Logical comparators**
- **Adders/subtractors**
- **General logic functions**

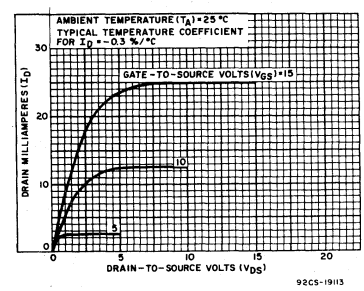


Fig.2 — Typical output n-channel drain characteristics.

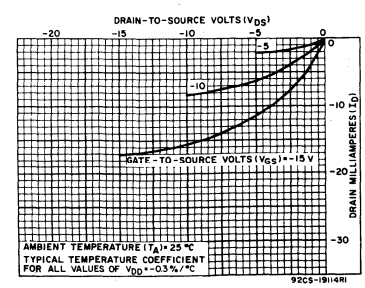


Fig.3 — Typical output p-channel drain characteristics.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				E Package				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current I_L Max.	–	–	5	0.5	0.005	0.5	30	5	0.05	5	70	μA
	–	–	10	1	0.01	1	60	10	0.1	10	140	
	–	–	15	25	0.5	25	1000	250	2.5	250	2500	
Output Voltage: Low Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	3.6	–	5	1.5 Min.; 2.25 Typ.								V
	7.2	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	1.4	–	5	1.5 Min.; 2.25 Typ.								
	2.8	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N Channel (Sink) I_DN Min.	0.5	–	5	0.75	1.2	0.6	0.45	0.35	1.2	0.3	0.25	mA
	0.5	–	10	1.5	2.4	1.2	0.9	0.7	2.4	0.6	0.5	
P Channel (Source): I_DP Min.	4.5	–	5	−0.45	−0.6	−0.3	−0.21	−0.21	−0.6	−0.15	−0.12	
	9.5	–	10	−0.95	−1.3	−0.65	−0.45	−0.45	−1.3	−0.32	−0.25	
Input Leakage Current I_{IL}, I_{IH}	Any Input		15	± 10^{-5} Typ., ± 1 Max.								μA

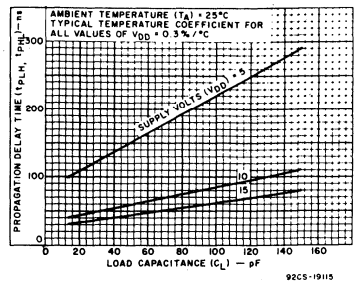


Fig.4 – Typical propagation-delay time vs. load capacitance.

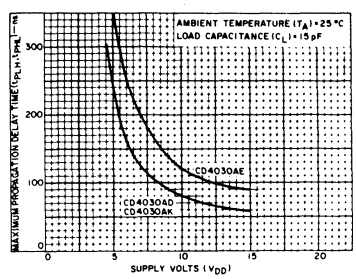


Fig.5 – Maximum propagation-delay time vs. supply voltage.

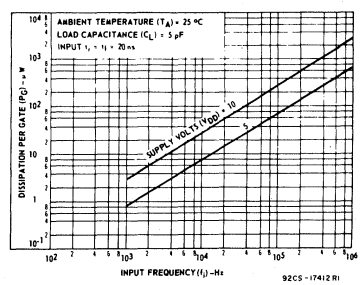


Fig.6 – Typical dynamic power dissipation characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

Characteristic	Test Conditions		LIMITS						Units
			D,F,K,H Packages			E Package			
		V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
Propagation Delay Time: t_{PLH}, t_{PHL}		5	–	100	200	–	100	300	ns
		10	–	40	100	–	40	150	
Transition Time: High-to-Low Level, t_{THL}		5	–	70	150	–	70	300	ns
		10	–	25	75	–	25	150	
Low-to-High Level, t_{TLH}		5	–	80	150	–	80	300	
		10	–	30	75	–	30	150	
Average Input Capacitance, C_I	Any Input		–	5	–	–	5	–	pF

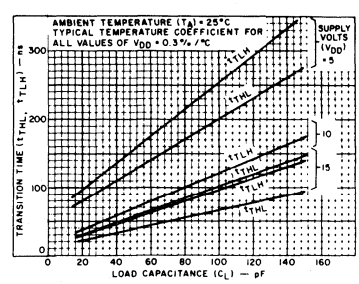


Fig.7 – Typical transition time vs. load capacitance.

COS/MOS 64-Stage Static Shift Register

The RCA-CD4031A is a 64-stage static shift register in which each stage is a D-type, master-slave flip-flop.

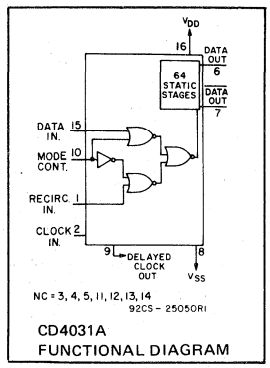
The logic level present at the DATA input is transferred into the first stage and shifted one stage at each positive-going clock transition. Maximum clock frequencies up to 4 Megahertz (typical) can be obtained. Because fully static operation is allowed, information can be permanently stored with the clock line in either the low or high state. The CD4031A has a MODE CONTROL input that, when in the high state, allows operation in the recirculating mode. Register packages can be cascaded and the clock lines driven directly for high speed operation. Alternatively, a delayed clock output (CL_D) is provided that enables cascading register packages while allowing reduced clock drive fan-out and rise- and fall-time requirements.

Data (Q) and $\overline{\text{Data}}$ ($\overline{Q}$) outputs are provided from the 64th register stage. The Data (Q) output is capable of drving one TTL or DTL load.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- **Fully static operation: DC to 4 MHz typ. @ $V_{DD} - V_{SS} = 10$ V**
- **Operation from a single 3 to 15 V positive or negative power supply**
- **High noise immunity**
- **Microwatt quiescent power dissipation: 10 μW (typ.) for ceramic packages; 100 μW (typ.) for plastic packages**



CD4031A
FUNCTIONAL DIAGRAM

- **Single phase clocking requirements**
- **Recirculation capability**
- **Data compatible with TTL-DTL**
- **Two cascading modes:**
  Direct clocking for high-speed operation
  Delayed clocking for reduced clock drive requirements
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Serial shift registers**
- **Time delay circuits**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg})	-65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})	
Voltages referenced to V_{SS} Terminal):	-0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)	
FOR T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = -55 to +100°C (PACKAGE TYPES D, F, K)	500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25° C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, K, H PACKAGES		E PACKAGE		
		MIN.	MAX.	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Data Hold Time, t_H	5	100	–	100	–	ns
	10	200	–	200	–	
Clock Pulse Width, t_W	5	0.62	–	1.3	–	μs
	10	1.25	–	0.5	–	
Clock Input Frequency, f_{CL}	5	dc	0.8	dc	0.4	MHz
	10	dc	2	dc	1	
Clock Rise and Fall Time, t_rCL, t_fCL*	5	–	2	–	2	μs
	10	–	1	–	1	

* If more than one unit is cascaded in the parallel clocked application, t_rCL should be made less than or equal to the sum of the propagation delay at 15 pF and the transition time of the output driving stage.

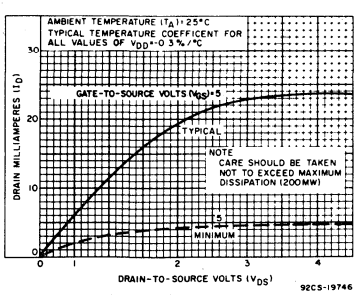


Fig. 1 – Typical and minimum output n-channel drain characteristics for Q output.

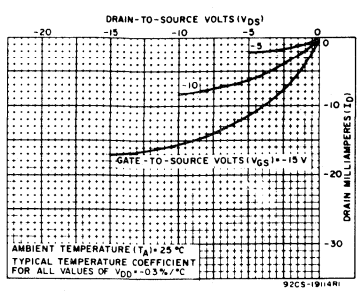


Fig. 2 – Typical output p-channel drain characteristics for Q output.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
				D, K, F, H PACKAGES				E PACKAGE				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	+25 TYP.	+25 LIMIT	+125	-40	+25 TYP.	+25 LIMIT	+85	
Quiescent Device Current, I_L Max.	–	–	5	10	0.5	10	600	50	1	50	700	μA
	–	–	10	25	1	25	1500	100	2	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max								V
	–	10	10	0 Typ.; 0.05 Max								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink), I_DN Min.	Q	0.4	–	4.5	1.6	2.6	1.3	0.91	1.6	2.6	1.3	1.05	mA
		0.5	–	10	5	8	4	3.2	5	8	4	3.2	
	$\overline{Q}$	0.5	–	5	0.11	0.18	0.09	0.06	0.05	0.18	0.045	0.037	
		0.5	–	10	0.24	0.4	0.2	0.14	0.12	0.4	0.1	0.08	
	CL_D	0.5	–	5	0.48	0.8	0.4	0.28	0.24	0.8	0.2	0.16	
		0.5	–	10	1.5	2.4	1.2	0.84	0.75	2.4	0.6	0.5	
P- Channel (Source): I_DP Min.	Q	4.5	–	5	-0.4	-0.64	-0.32	-0.22	-0.20	-0.64	-0.16	-0.13	
		9.5	–	10	-0.85	-1.4	-0.70	-0.49	-0.42	-1.4	-0.35	-0.29	
	$\overline{Q}$	4.5	–	5	-0.11	-0.18	-0.09	-0.06	-0.05	-0.18	-0.045	-0.037	
		9.5	–	10	-0.24	-0.4	-0.20	-0.14	-0.12	-0.4	-0.10	-0.08	
	CL_D	4.5	–	5	-0.48	-0.8	-0.40	-0.28	-0.24	-0.8	-0.20	-0.16	
		9.5	–	10	-1	-1.6	-0.80	-0.56	-0.5	-1.6	-0.40	-0.32	
Input Leakage Current, I_{IL}, I_{IH}	Any Input	–	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								μA

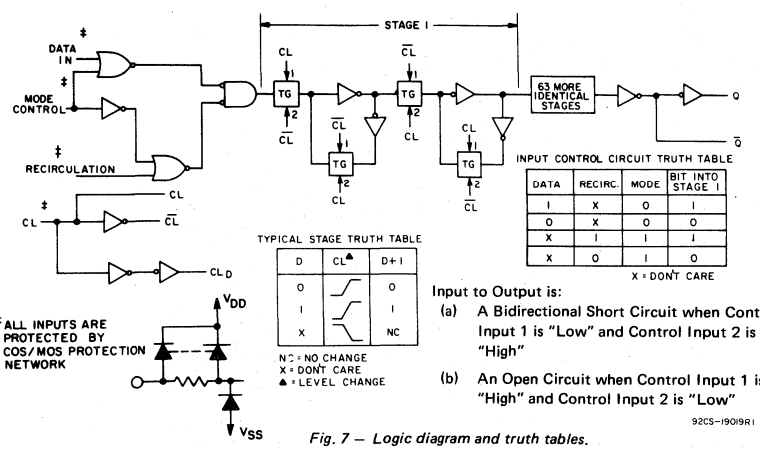


Fig. 7 – Logic diagram and truth tables.

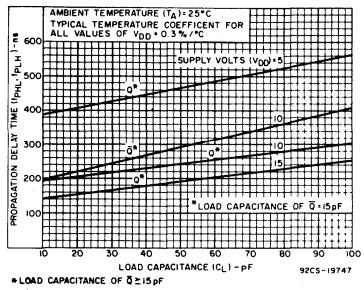


Fig. 3 – Typical propagation delay time vs. load capacitance for data outputs.

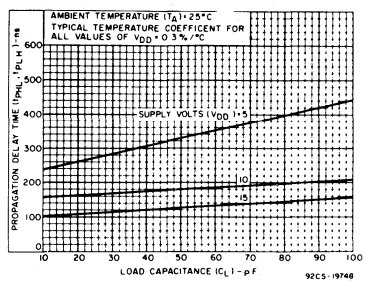


Fig. 4 – Typical propagation delay vs. load capacitance for delayed clock output.

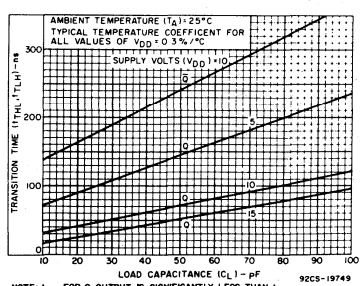


Fig. 5 – Typical transition time vs. load capacitance for data outputs.

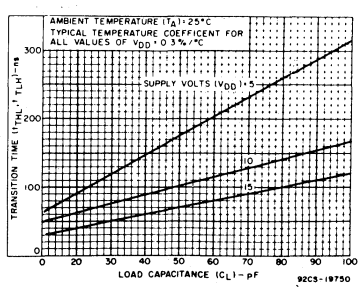


Fig. 6 – Typical transition time vs. load capacitance for delayed clock output.

DYNAMIC ELECTRICAL CHARACTERISTICS

at T_A=25°C, Input t_r,t_f=20 ns, C_L=15 pF (unless otherwise specified), R_L=200 kΩ

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	LIMITS D, F, K, H MIN.	D, F, K, H TYP.	D, F, K, H MAX.	E MIN.	E TYP.	E MAX.	UNITS
Propagation Delay Time; t_{PLH}, t_{PHL}		5	–	400	800	–	400	1600	ns
Clock to Data Output Q & $\overline{Q}$*		10	–	200	400	–	200	800	
Clock to CL_D	C_L = 60 pF	5	–	400	800	–	400	1600	
		10	–	200	400	–	200	800	
Transition Time; t_{THL}, t_{TLH} Q Output		5	–	75	150	–	75	300	ns
		10	–	30	60	–	30	120	
$\overline{Q}$ Output		5	–	300	600	–	300	1200	
		10	–	150	300	–	150	600	
CL_D Output	C_L = 60 pF	5	–	200	400	–	200	800	
		10	–	100	200	–	100	400	
Clock Rise and Fall Time; t_rCL, t_fCL**		5	–	–	2	–	–	2	μs
		10	–	–	1	–	–	1	
Minimum Data Set-Up Time, t_S		5	–	200	400	–	200	800	ns
		10	–	50	100	–	50	200	
Maximum Clock Input Frequency, f_{CL}***		5	0.8	2	–	0.4	2	–	MHz
		10	2	4	–	1	4	–	
Minimum Data Hold Time, t_H		5	–	50	100	–	50	100	ns
		10	–	100	200	–	100	250	
Minimum Clock Pulse Width, t_W		5	–	1.3	0.62	–	2.6	1.3	μs
		10	–	2.5	1.25	–	1	0.5	
Average Input Capacitance, C_I Clock			–	60	–	–	60	–	pF
All Others			–	5	–	–	5	–	

* Capacitive loading on $\overline{Q}$ output affects propagation delay of Q output. These limits apply for $\overline{Q}$ load $C_L \leq 15$ pF.

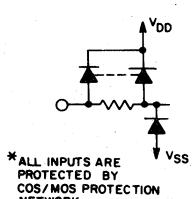
** If more than one unit is cascaded in the parallel clocked application, t_rCL should be made less than or equal to the sum of the propagation delay at 15 pF and the transition time of the output driving stage.

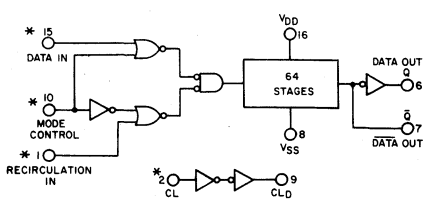
*** Maximum Clock Frequency for Cascaded Units;

a) Using Delayed Clock Feature –

$$f_{max} = \frac{1}{(n-1)\,CL_D \text{ prop. delay} + Q \text{ prop. delay} + \text{set-up time}}$$ where n = number of packages

b) Not Using Delayed Clock – $f_{max} = \frac{1}{\text{propagation delay} + \text{set-up time}}$





92CS-19745R2

Fig. 12 – Functional diagram.

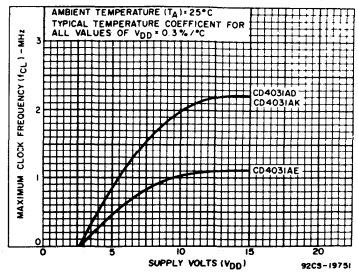


Fig. 8 – Maximum clock input frequency vs. supply voltage.

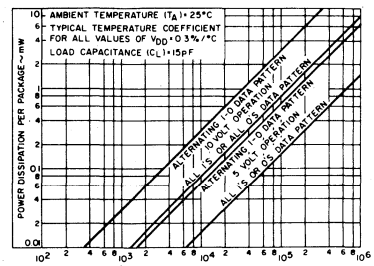


Fig. 9 – Typical power dissipation vs. frequency.

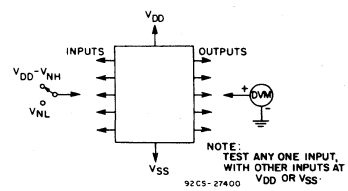


Fig. 10 – Noise-immunity test circuit.

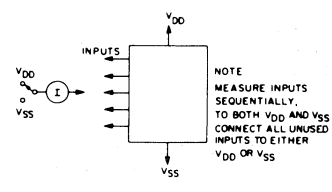
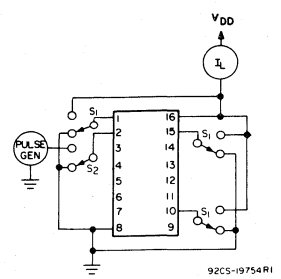


Fig. 11 – Input-leakage-current test circuit.



WITH S_1 AT GROUND, CLOCK UNIT 64 TIMES BY CONNECTING S_2 TO PULSE GENERATOR. RETURN S_2 TO GND AND MEASURE LEAKAGE CURRENT. REPEAT WITH S_1 AT V_{DD}.

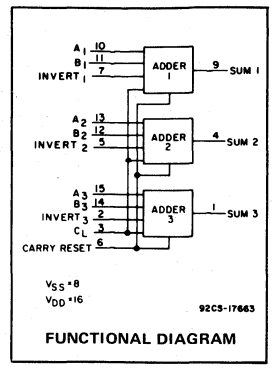
Fig. 13 – Quiescent-device-current test circuit.

CD4032A, CD4038A Types

COS/MOS Triple Serial Adders

Positive Logic Adder – CD4032A

Negative Logic Adder – CD4038A



FUNCTIONAL DIAGRAM

Features:

- **Invert inputs on all adders for sum complementing applications**
- **Fully static operation. . . . . dc to 5 MHz (typ.)**
- **Buffered outputs**
- **Single-phase clocking**
- **Microwatt quiescent power dissipation. . . . 5 μW (typ.)**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

The RCA-CD4032A and CD4038A types consist of three serial adder circuits with common CLOCK and CARRY-RESET inputs. Each adder has two provisions for two serial DATA INPUT signals and an INVERT command signal. When the command signal is a logical "1", the sum is complemented. Data words enter the adder with the least significant bit first; the sign bit trails. The output is the MOD 2 sum of the input bits plus the carry from the previous bit position. The carry is only added at the positive-going clock transition for the CD4032A or at the negative-going clock for the CD4038A, thus, for spike free operation the input data transitions should occur as soon as possible after the triggering edge.

The CARRY is reset to a logical "0" at the end of each word by applying a logical "1" signal to a CARRY-RESET input one bit-position before the application of the first bit of the next word. Figs. 2 and 4 show definitive waveforms for all input and output signals.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

Applications:

- **Serial arithmetic units**
- **Digital correlators**
- **Digital datalink computers**
- **Flight control computers**
- **Digital servo control systems**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C

OPERATINT GEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C

PACKAGE TYPE E . . . . . −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D)

FOR T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, K, H Packages		E Package		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Input Setup Time, t_S	5 10	t_fCL	–	t_fCL	–	ns
Clock Input Frequency, f_{CL}	5 10	dc dc	1.5 3	dc dc	2.5 5	MHz
Clock Rise or Fall Time, t_rCL, t_fCL	5 10	– –	15 15	– –	15 15	μs

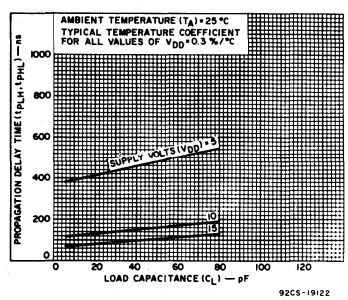


Fig. 1 – Typical propagation delay time vs. load capacitance for A, B, or INVERT inputs to sum outputs.

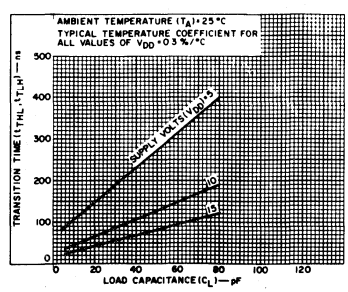


Fig. 2 – Typical transition time vs.load capacitance for sum outputs.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS D, F, K, H Packages Min.	Typ.	Max.	LIMITS E Package Min.	Typ.	Max.	UNITS
Propagation Delay Time; t_{PLH}, t_{PHL} A, B, or Invert Inputs to Sum	5	–	400	1100	–	400	1400	ns
Outputs	10	–	125	250	–	125	300	
Clock Input to Sum Outputs	5	–	800	2200	–	800	2400	
	10	–	250	500	–	250	600	
Transition Time; t_{THL}, t_{TLH} (Sum Outputs)	5	–	125	375	–	125	425	ns
	10	–	50	150	–	50	200	
Maximum Clock Input Frequency, f_{CL}	5	1.5	2.5	–	1	2.5	–	MHz
	10	3	5	–	2	5	–	
Clock Rise & Fall Time; t_rCL, t_fCL**	5	–	–	15	–	–	15	μs
	10	–	–	15	–	–	15	
Minimum Input Set Up Time, t_S*	5	–	–	t_rCL	–	–	t_rCL	ns
	10							
Average Input Capacitance, C_I		–	5	–	–	5	–	pF

*This characteristic refers to the minimum time required for the A, B, or Reset Inputs to change state following a positive clock transition (CD4032A) or negative transition (CD4038A).

**If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

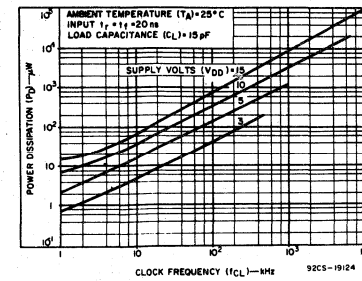


Fig. 3 – Typical dissipation characteristics.

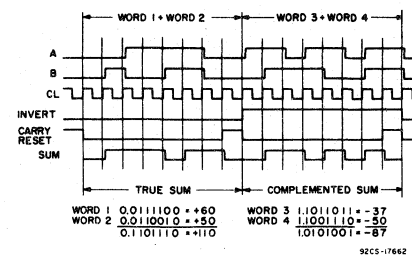


Fig. 4 – CD4032A timing diagram.

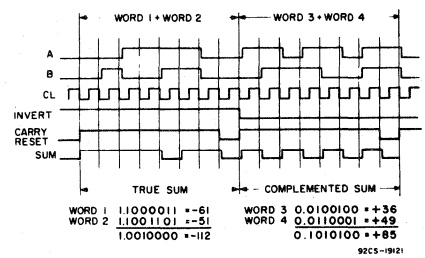


Fig. 5 – CD4038A timing diagram.

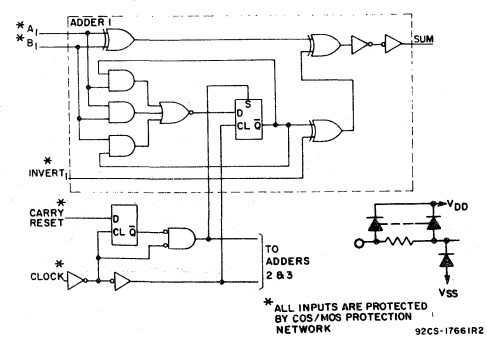


Fig. 6 – CD4032A logic diagram of one of three serial adders.

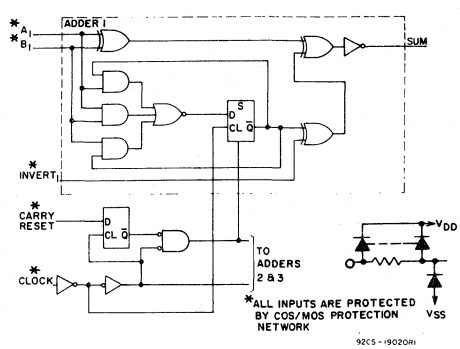


Fig. 7 – CD4038A logic diagram of one of three serial adders.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D, K, F, H Packages				E Package				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current I_L Max.	–	–	5	5	0.3	5	300	50	0.5	50	700	μA
	–	–	10	10	0.5	10	600	100	1	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current N-Channel (Sink), I_DN Min.	0.5	–	5	0.6	0.9	0.5	0.3	0.25	0.9	0.2	0.14	mA
	0.5	–	10	0.75	2.4	0.7	0.6	0.6	2.4	0.5	0.4	
P-Channel (Source), I_DP Min.	4.5	–	5	−0.21	−0.4	−0.15	−0.075	−0.14	−0.4	−0.1	−0.095	
	9.5	–	10	−0.7	−7.2	−0.55	−0.35	−0.3	−1.2	−0.27	−0.22	
Input Leakage Current, I_{IL}, I_{IH}	Any Input			±10^{-5} Typ., ±1 Max.								μA
	–	–	15									

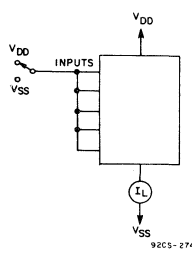


Fig. 8 – Quiescent-device-current test circuit.

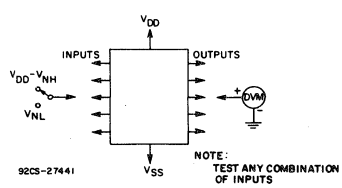


Fig. 9 – Noise-immunity test circuit.

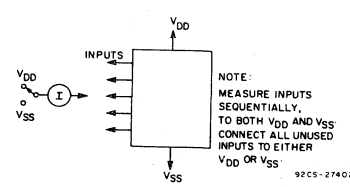


Fig. 10 – Input-leakage-current test circuit.

COS/MOS 8-Stage Static Bidirectional Parallel/Serial Input/Output Bus Register

The RCA-CD4034A is a static eight-stage parallel-or serial-input parallel-output register. It can be used to:

1) bidirectionally transfer parallel information between two buses, 2) convert serial data to parallel form and direct the parallel data to either of two buses, 3) store (recirculate) parallel data, or 4) accept parallel data from either of two buses and convert that data to serial form. Inputs that control the operations include a single-phase CLOCK (CL), A DATA ENABLE (AE), ASYNCHRONOUS/SYNCHRONOUS (A/S), A-BUS-TO-B-BUS/2B-BUS-TO-A-BUS (A/B), and PARALLEL/SERIAL (P/S).

Data inputs include 16 bidirectional parallel data lines of which the eight A data lines are inputs (outputs) and the B data lines are outputs (inputs) depending on the signal level on the A/B input. In addition, an input for SERIAL DATA is also provided.

All register stages are D-type master-slave flip-flops with separate master and slave clock inputs generated internally to allow synchronous or asynchronous data transfer from master to slave. Isolation from external noise and the effects of loading is provided by output buffering.

PARALLEL OPERATION

A high P/S input signal allows data transfer into the register via the parallel data lines synchronously with the positive transition of the clock provided the A/S input is low. If the A/S input is high the transfer is independent of the clock. The direction of data flow is controlled by the A/B input. When this signal is high the A data lines are inputs (and B data lines are outputs); a low A/B signal reverses the direction of data flow.

The AE input is an additional feature which allows many registers to feed data to a common bus. The A DATA lines are enabled only when this signal is high.

Data storage through recirculation of data in each register stage is accomplished by making the A/B signal high and the AE signal low.

SERIAL OPERATION

A low P/S signal allows serial data to transfer into the register synchronously with the positive transition of the clock. The A/S input is internally disabled when the register is in the serial mode (asynchronous serial operation is not allowed).

The serial data appears as output data on either the B lines (when A/B is high) or the A lines (when A/B is low and the AE signal is high).

Register expansion can be accomplished by simply cascading CD4034A packages.

The CD4034A-Series types are supplied in 24-lead hermetic dual-in-line ceramic packages (D suffix), 24-lead dual-in-line plastic packages (E suffix), 24-lead ceramic flat packages (K suffix), and in chip form (H suffix).

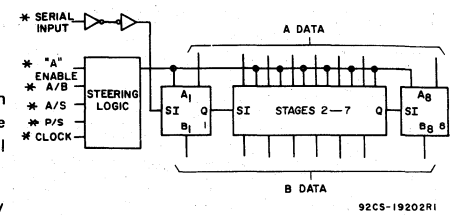
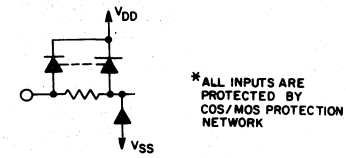


Fig. 1 – Functional diagram.



MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . -65 to + 150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, K, H . . . . . -55 to +125°C

PACKAGE TYPE E. . . . . -40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal) . . . . . -0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D)

FOR T_A = -40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = -55 to +100°C (PACKAGE TYPES D, K) . . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, K) . . . . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . -0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS *at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:*

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, K, H PACKAGES		E PACKAGE		
		MIN.	MAX.	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Data Setup Time, t_S	5 10	500 200	– –	500 200	– –	ns
Clock Pulse Width, t_W	5 10	400 175	– –	400 175	– –	ns
Clock Input Frequency, f_{CL}	5 10	dc dc	1.5 3	dc dc	1.5 3	MHz
Clock Rise and Fall Time, t_rCL, t_fCL*	5,10	–	15	–	15	μs

*If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

CD4034A Types

Table I — Truth Table for Register Input-Levels and the Resulting Register Operation (L = Low Level, H = High Level, X = Don't Care)

"A" Enable	P/S	A/B	A/S	Operation*
L	L	L	X	Serial Mode; Synch. Serial Data Input, "A" Parallel Data Outputs Disabled
L	L	H	X	Serial Mode; Synch. Serial Data Input, "B" Parallel Data Output
L	H	L	L	Parallel Mode; "B" Synch. Parallel Data Inputs, "A" Parallel Data Outputs Disabled
L	H	L	H	Parallel Mode; "B" Asynch. Parallel Data Inputs, "A" Parallel Data Outputs Disabled
L	H	H	L	Parallel Mode; "A" Parallel Data Inputs Disabled, "B" Parallel Data Outputs, Synch. Data Recirculation
L	H	H	H	Parallel Mode; "A" Parallel Data Inputs Disabled, "B" Parallel Data Outputs, Asynch. Data Recirculation
H	L	L	X	Serial Mode; Synch. Serial Data Input, "A" Parallel Data Output
H	L	H	X	Serial Mode; Synch. Serial Data Input, "B" Parallel Data Output
H	H	L	L	Parallel Mode; "B" Synch. Parallel Data Input, "A" Parallel Data Output
H	H	L	H	Parallel Mode; "B" Asynch. Parallel Data Input, "A" Parallel Data Output
H	H	H	L	Parallel Mode; "A" Synch. Parallel Data Input, "B" Parallel Data Output
H	H	H	H	Parallel Mode; "A" Asynch. Parallel Data Input, "B" Parallel Data Output

*Outputs change at positive transition of clock in the serial mode and when the A/S control input is "low" in the parallel mode.

Features:

- Bidirectional parallel data input
- Parallel or serial inputs/parallel outputs
- Asynchronous or synchronous parallel data loading
- Parallel data-input enable on "A" data lines
- Data recirculation for register expansion
- Multipackage register expansion
- Fully static operation DC-to-5 MHz (typ.) At $V_{DD}-V_{SS}$ = 10 V
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications:

- Parallel Input/Parallel Output, Parallel Input/Serial Output, Serial Input/Parallel Output, Serial Input/Serial Output Register
- Shift right/shift left register
- Shift right/shift left with parallel loading
- Address register
- Buffer register
- Bus system register with enable parallel lines at bus side
- Double bus register system
- Up-Down Johnson or ring counter
- Pseudo-random code generators
- Sample and hold register (storage, counting, display)
- Frequency and phase comparator

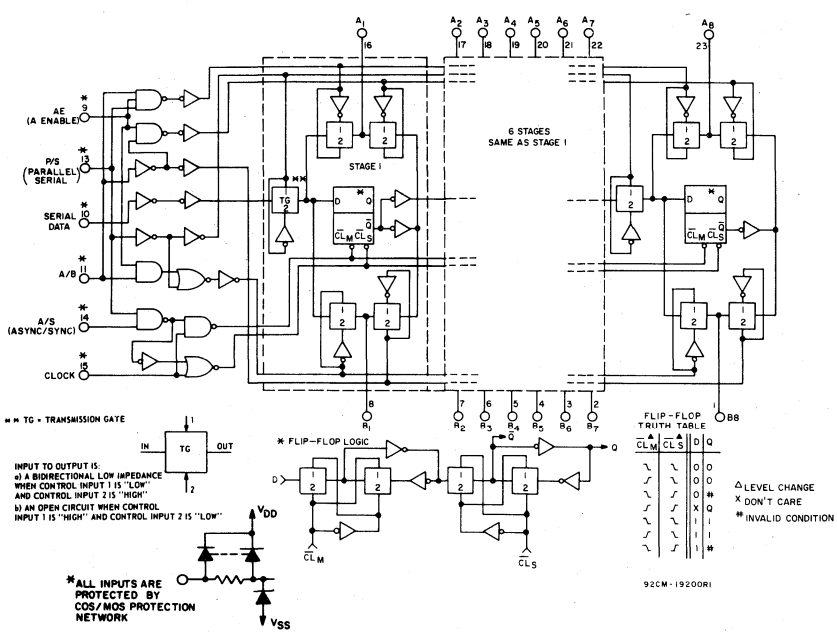


Fig. 2 — Logic diagram.

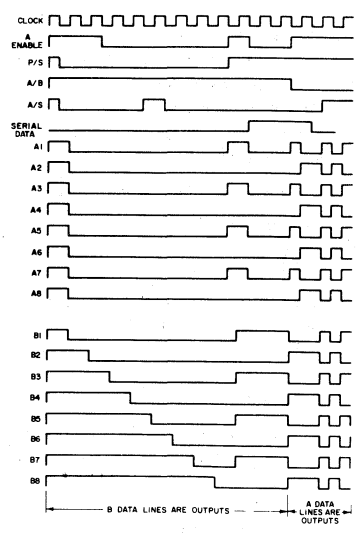


Fig. 3 — Timing diagram.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
				D, K, H PACKAGES				E PACKAGE				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	+25 TYP.	+25 LIMIT	+125	-40	+25 TYP.	+25 LIMIT	+85	
Quiescent Device Current, I_L Max.	–	–	5	5	0.3	5	300	50	5	50	700	μA
	–	–	10	10	0.5	10	600	100	1	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max								V
	–	10	10	0 Typ.; 0.05 Max								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink),	0.5	–	5	0.124	0.2	0.1	0.07	0.124	0.2	0.1	0.07	mA
I_DN Min.	0.5	–	10	0.31	0.5	0.25	0.175	0.31	0.5	0.25	0.175	
P-Channel (Source):	4.5	–	5	-0.075	-0.1	-0.05	-0.035	-0.075	-0.1	-0.05	-0.035	
I_DP Min.	9.5	–	10	-0.188	-0.25	-0.125	-0.088	-0.188	-0.25	-0.125	-0.088	
Input Leakage Current, I_{IL}, I_{IH}	Any Input –	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								μA

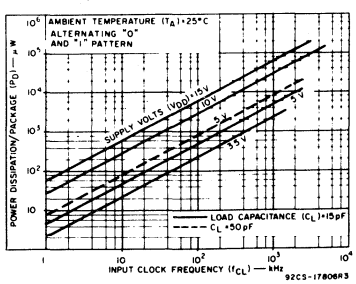


Fig. 7 – Typical dissipation characteristics.

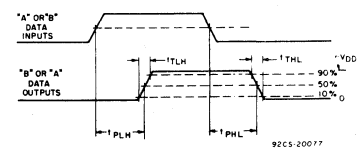


Fig. 8 – Asynchronous operation propagation delay time and transition time.

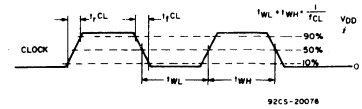


Fig. 9 – Clock pulse rise and fall times.

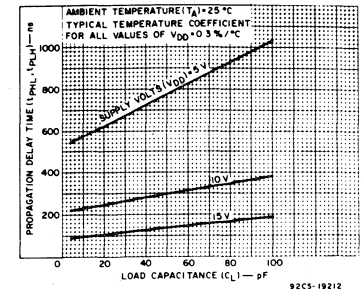


Fig. 4 – Typical propagation delay time vs. load capacitance.

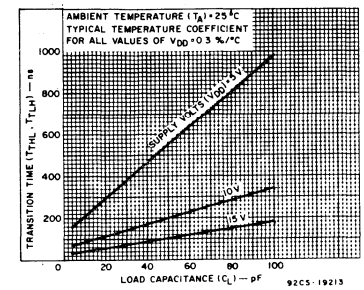


Fig. 5 – Typical transition time vs. load capacitance.

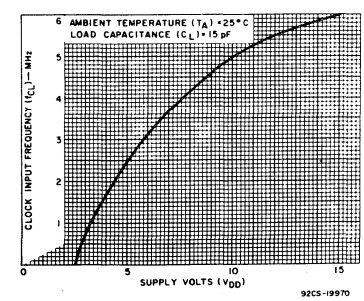


Fig. 6 – Typical clock input frequency vs. supply voltage.

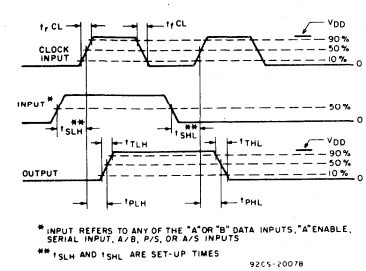


Fig. 10 – Synchronous operation propagation delay times, transition times, and set-up times.

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, RL = 200kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNIT
		D, K, H PACKAGES			E PACKAGE			
	V_{DD} (V)	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Propagation Delay Time; t_{PLH}, t_{PHL}	5	–	600	1200	–	600	1200	ns
	10	–	240	480	–	240	480	
Transition Time; t_{THL}, t_{TLH}	5	–	250	750	–	250	750	ns
	10	–	100	300	–	100	300	
Maximum Clock Input Frequency, f_{CL}	5	1.5	2.5	–	1.5	2.5	–	MHz
	10	3	5	–	3	5	–	
Clock Pulse Width, t_W	5	–	200	400	–	200	400	ns
	10	–	100	175	–	100	175	
Min. High-Level AE, P/S, A/S Pulse Width	5	–	240	480	–	240	480	ns
	10	–	85	195	–	85	195	
Clock Rise & Fall Time t_rCL, t_fCL*	5	–	–	15	–	–	15	μs
	10	–	–	15	–	–	15	
Data Set-Up Time, t_S	5	–	250	500	–	250	500	ns
	10	–	100	200	–	100	200	
Average Input Capacitance, C_I	Any Input	–	5	–	–	5	–	pF

*If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

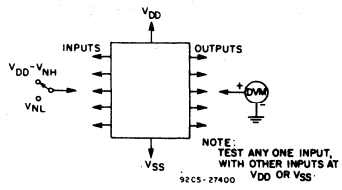


Fig. 11 – Noise-immunity test circuit.

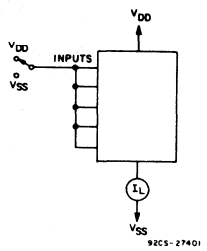


Fig. 12 – Quiescent-device-current test circuit.

APPLICATIONS

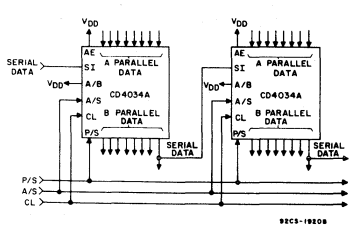


Fig. 14 – 16-Bit parallel in/parallel out, parallel in/serial out, serial in/parallel out, serial in/serial out register.

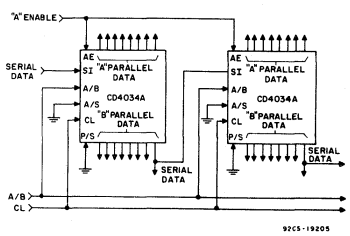


Fig. 15 – 16-Bit serial in/gated parallel out register.

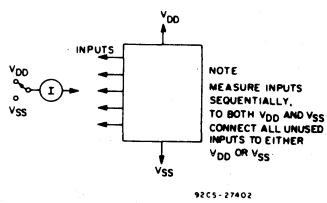


Fig. 13 – Input-leakage-current test circuit.

COS/MOS 4-Stage Parallel In/Parallel Out Shift Register

with J-$\overline{K}$ Serial Inputs and True/Complement Outputs

Features:

- 4-Stage clocked shift operation
- Synchronous parallel entry on all 4 stages
- J$\overline{K}$ inputs on first stage
- Asynchronous True/Complement control on all outputs
- Static flip-flop operation; Master-slave configuration
- Reset control
- Buffered outputs
- Low power dissipation — 5μW typ. (ceramic)
- High speed — to 5 MHz
- Quiescent current specified to 15 V
- Maximum input leakage current of 1μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

The RCA-CD4035A is a four-stage clocked signal serial register with provision for SYNCHRONOUS PARALLEL inputs to each stage and SERIAL inputs to the first stage via J$\overline{K}$ logic. Register stages 2, 3, and 4 are coupled in a serial D flip-flop configuration when the register is in the serial mode (PARALLEL/SERIAL control low).

Parallel entry via the D line of each register stage is permitted only when the PARALLEL/SERIAL control is high.

In the parallel or serial mode information is transferred on positive clock transitions.

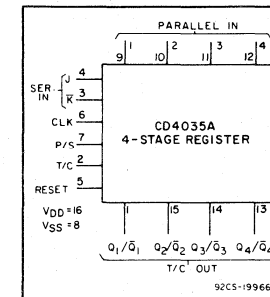
When the TRUE/COMPLEMENT control is high, the TRUE contents of the register are available at the output terminals. When the TRUE/COMPLEMENT control is low, the outputs are the complements of the data in the register. The TRUE/COMPLEMENT control functions asynchronously with repect to the CLOCK signal.

J$\overline{K}$ input logic is provided on the first stage SERIAL input to minimize logic requirements particularly in counting and sequence-generation applications. With J$\overline{K}$ inputs connected together, the first stage becomes a D flip-flop. An asynchronous common RESET is also provided.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

Applications

- **Counters, Registers**
  Arithmetic-unit registers
  Shift left — shift right registers
  Serial-to-parallel/parallel-to-serial conversions
- **Sequence generation**
- **Control circuits**
- **Code conversion**



CD4035A
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . −66 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H. . . . . −55 to +125°C

PACKAGE TYPE E . . . . . −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal): . . . . . −0.5 to +15V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12mW/°C to 200 mW

FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . Derate Linearly at 12mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES). 100mW

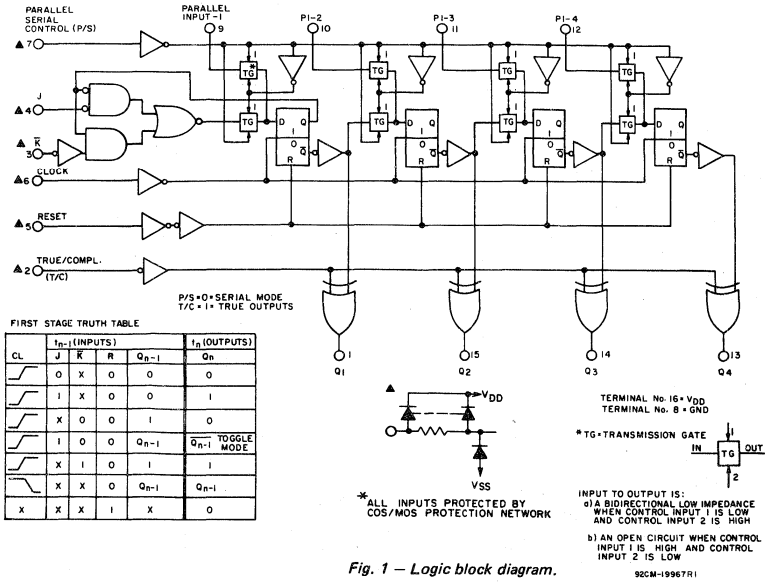
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max . . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A=25°C, except as noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, K, H PACKAGES		E PACKAGE		
		MIN.	MAX.	MIN.	MAX.	
Supply Voltage Range (For T_A = Full Package-Temperature Range		3	12	3	12	V
Data Setup Time, t_S:						
J/$\overline{K}$ Lines	5	500	—	750	—	ns
	10	200	—	250	—	
Parallel-In Lines	5	350	—	500	—	
	10	80	—	100	—	
Clock Pulse Width, t_W	5	335	—	500	—	ns
	10	165	—	250	—	
Clock Rise and Fall Time, t_rCL,t_fCL	5	—	15	—	15	µs
	10	—	5	—	5	
Reset Pulse Duration, t_W	5	400	—	500	—	ns
	10	175	—	200	—	



FIRST STAGE TRUTH TABLE

CL	t_{n-1} (INPUTS) J	K	R	Q_{n-1}	t_n (OUTPUTS) Q_n
⎍⎍	0	X	0	0	0
⎍⎍	1	X	0	0	1
⎍⎍	X	0	0	1	0
⎍⎍	1	0	0	Q_{n-1}	$\overline{Q_{n-1}}$ TOGGLE MODE
⎍⎍	X	1	0	1	1
⎍⎍	X	X	0	Q_{n-1}	Q_{n-1}
X	X	X	1	X	0

Fig. 1 — Logic block diagram.

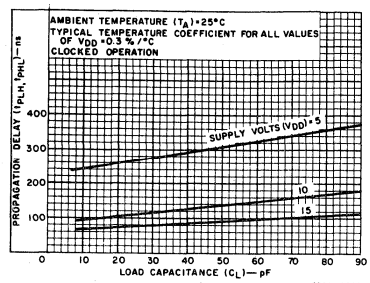


Fig. 2 — Typical propagation delay time vs. load capacitance.

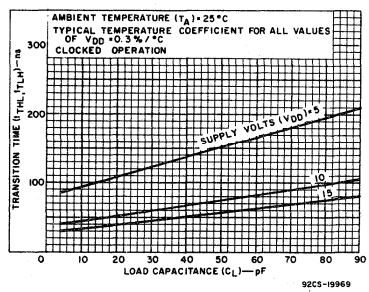


Fig. 3 — Typical transition time vs. load capacitance.

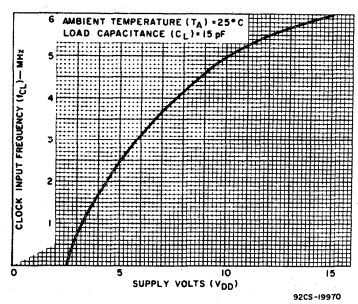


Fig. 4 — Typical clock input frequency vs. supply voltage.

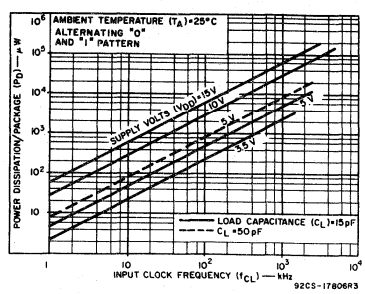


Fig. 5 — Typical dynamic power dissipation characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) D, K, F, H PACKAGES -55	+25 TYP.	+25 LIMIT	+125	E PACKAGE -40	+25 TYP.	+25 LIMIT	+85	UNITS
Quiescent Device Current, I_L Max.	—	—	5	5	0.3	5	300	50	0.5	50	700	μA
	—	—	10	10	0.5	10	600	100	1	100	1400	
	—	—	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low Level, V_{OL}	—	5	5	0 Typ.; 0.05 Max								V
	—	10	10	0 Typ.; 0.05 Max								
High Level V_{OH}	—	0	5	4.95 Min.; 5 Typ.								
	—	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	—	5	1.5 Min.; 2.25 Typ.								V
	9	—	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	—	5	1.5 Min.; 2.25 Typ.								
	1	—	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	—	5	1 Min.								V
	9	—	10	1 Min.								
Inputs High, V_{NMH}	0.5	—	5	1 Min.								
	1	—	10	1 Min.								
Output Drive Current: N-Channel (Sink),	0.5	—	5	0.62	1	0.5	0.35	0.43	1	0.35	0.24	mA
I_DN Min.	0.5	—	10	1.55	2.5	1.25	0.87	1.05	2.5	0.85	0.59	
P-Channel (Source):	4.5	—	5	-0.31	-0.5	-0.25	-0.17	-0.2	-0.5	-0.18	-0.12	
I_DP Min.	9.5	—	10	-0.81	-1.3	-0.65	-0.45	-0.56	-0.31	-0.45	-0.31	
Input Leakage Current,	Any Input											μA
I_{IL}, I_{IH}	—	—	15	$\pm 10^{-5}$ Typ., ±1 Max.								

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25^oC$, Input $t_r, t_f = 20$ ns, $C_L = 15$ pF, $R_L = 200$ kΩ

CHARACTERISTICS	TEST CONDITIONS		LIMITS						UNITS
			D, F, K, H PACKAGES			E PACKAGE			
		V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
CLOCKED OPERATION									
Propagation Delay Time: t_{PLH}, t_{PHL}		5	–	250	500	–	250	700	ns
		10	–	100	200	–	100	300	
Transition Time: t_{THL}, t_{TLH}		5	–	100	200	–	100	300	ns
		10	–	50	100	–	50	150	
Minimum Clock Pulse Width, t_W		5	–	200	335	–	200	500	ns
		10	–	100	165	–	100	250	
Maximum Clock Rise & Fall Time t_{rCL}, t_{fCL}*		5	–	–	15	–	–	15	μs
		10	–	–	5	–	–	5	
Minimum Setup Time: J/$\overline{K}$ Lines		5	–	250	500	–	250	750	ns
		10	–	100	200	–	100	250	
Parallel-In Lines		5	–	100	350	–	100	500	
		10	–	50	80	–	50	100	
Maximum Clock Frequency, f_{CL}		5	1.5	2.5	–	1	2.5	–	MH_z
		10	3	5	–	2	5	–	
Input Capacitance, C_I	Any Input		–	5	–	–	5	–	pF
RESET OPERATION									
Propagation Delay Time: t_{PHL}, t_{PLH}		5	–	250	500	–	250	700	ns
		10	–	100	200	–	100	300	
Minimum Reset Pulse Width, t_W		5	–	200	400	–	200	500	ns
		10	–	100	175	–	100	200	

*If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

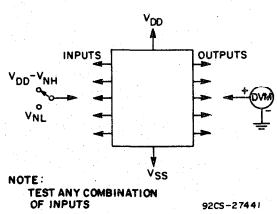


Fig. 6 – Noise-immunity test circuit.

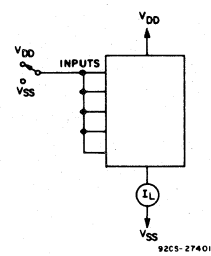


Fig. 7 – Quiescent-device-current test circuit.

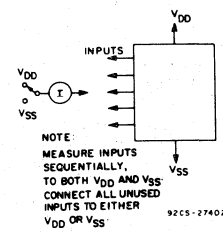


Fig. 8 – Input-leakage-current test circuit.

CD4036A, CD4039A Types

COS/MOS 4-Word by 8-Bit Random-Access NDRO Memory

Binary Addressing — CD4036AD, CD4036AK
Direct Word-Line Addressing — CD4039AD, CD4039AK

RCA type CD4036A is a single monolithic integrated circuit containing a 4-word x 8-bit Random Access NDRO Memory. Inputs include 8 INPUT-BIT lines, CHIP INHIBIT, WRITE, READ INHIBIT, MEMORY BYPASS, and 2 ADDRESS inputs. 8 OUTPUT-BIT lines are provided.

All input and output lines utilize standard COS/MOS inverter configurations and hence can be directly interfaced with COS/MOS logic devices.

CHIP INHIBIT allows memory word expansion by WIRE-ORing of multiple CD4036A packages at either the 8-bit input and/or output lines (See Fig.15). With CHIP INHIBIT "high", both READ and WRITE operations are inhibited on the CD4036A. With CHIP INHIBIT "low", information can be written into and/or read continuously from one of the four words selected by the binary code on the two address lines. With CHIP INHIBIT "low", a "high" WRITE signal and a "low" READ INHIBIT signal activate WRITE and READ operations, respectively, at the addressed word location (See Fig.4).

The MEMORY BYPASS signal, when "high", allows shunting of information from the 8 INPUT-BIT lines directly to the 8 OUTPUT-BIT lines without disturbing the state of the 4 words. During the bypass operation input information may also be written into a selected word location, provided the CHIP INHIBIT is "low" and the WRITE is "high". The READ operation is deactivated during the BYPASS operation because information is fed directly from the 8 INPUT-BIT lines to the 8 OUTPUT-BIT lines.

RCA type CD4039A is identical to the CD4036A with the exception that individual address-line inputs have been provided for each memory word in place of the binary ADDRESS, CHIP INHIBIT, and READ INHIBIT inputs. When Wire-Oring multiple CD4039A packages for memory word expansion, an individual CD4039A is selected by addressing one of its word locations. The READ operation is activated whenever a word location is addressed (via a "high" signal—see Fig.5).

These devices will be supplied in two different 24-lead ceramic packages; the CD4036AK and CD4039AK in the flat-pack, and the CD4036AD and CD4039AD in the dual-in-line package.

Special Features:

- **COS/MOS logic compatibility at all input and output terminals**
- **Memory bit expansion**
- **Memory word expansion via Wire-OR capability at the 8 INPUT-BIT and 8 OUTPUT-BIT lines**
- **Memory bypass capability for all bits**
- **Buffering on all outputs**
- **CD4036A- on-chip binary address decoding, separate READ INHIBIT and WRITE controls**
- **Access Time—200 ns(Typ) at V_{DD}=10 V**
- **CD4039A-Direct word-line addressing**

Applications:

Digital equipment where low power dissipation and/or high noise immunity are primary design requirements.

- **Channel Preset Memory in digital frequency-synthesizer circuits**
- **General-purpose and scratch-pad memory in COS/MOS and other low-power systems.**

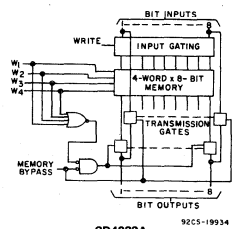
MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage Temperature Range	−65 to +150	°C	
Operating Temperature Range	−55 to +125	°C	
DC Supply Voltage Range (V_{DD} − V_{SS})	−0.5 to +15	V	
Device Dissipation (Per Pkg.)	200	mW	
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$		
Recommended DC Supply Voltage (V_{DD} − V_{SS})	3 to 15	V	
Lead Temperature (During soldering) At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 seconds max.	265	°C	

STATIC ELECTRICAL CHARACTERISTICS (All inputs $V_{SS} \leq V_I \leq V_{DD}$)
(Recommended DC Supply Voltage (V_{DD} − V_{SS}) = 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS CD4036AD, CD4036AK CD4039AD, CD4039AK									UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.
			V_O Volts	V_{DD} Volts	−55°C Min.	−55°C Typ.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Typ.	125°C Max.		
Quiescent Device Current	I_L			5	–	–	5	–	0.5	5	–	–	300	μA	11, 12
				10	–	–	10	–	1	10	–	–	600		
Quiescent Device Dissipation/Package	P_D			5	–	–	25	–	2.5	25	–	–	1500	μW	–
				10	–	–	100	–	10	100	–	–	6000		
Output Voltage: Low-Level	V_{OL}			5	–	–	0.01	–	0	0.01	–	–	0.05	V	–
				10	–	–	0.01	–	0	0.01	–	–	0.05		
High-Level	V_{OH}			5	4.99	–	–	4.99	5	–	4.95	–	–	V	–
				10	9.99	–	–	9.99	10	–	9.95	–	–		
Noise Immunity (All inputs except bit inputs when in memory bypass mode.)	V_{NL}		0.8	5	1.5	–	–	1.5	2.25	–	1.4	–	–	V	13
			1.0	10	3	–	–	3	4.5	–	2.9	–	–		
	V_{NH}		4.2	5	1.4	–	–	1.5	2.25	–	1.5	–	–		
			9.0	10	2.9	–	–	3	4.5	–	3	–	–		
Output Drive Current: N-Channel	I_{DN}	Normal Read Modes	0.5	5	0.12	–	–	0.10	0.20	–	0.07	–	–	mA	6
			0.5	10	0.30	–	–	0.25	0.50	–	0.17	–	–		
P-Channel	I_{DP}		4.5	5	−0.12	–	–	−0.10	−0.20	–	−0.07	–	–	mA	7
			9.5	10	−0.30	–	–	−0.25	−0.50	–	−0.17	–	–		
Output Drive Current: N-Channel	I_{DN}	Memory Bypass Mode +	0.5	5	0.04	–	–	0.03	0.06	–	0.02	–	–	mA	–
			0.5	10	0.09	–	–	0.075	0.15	–	0.05	–	–		
P-Channel	I_{DP}		4.5	5	−0.04	–	–	−0.03	−0.06	–	−0.02	–	–	mA	–
			9.5	10	−0.09	–	–	−0.075	−0.15	–	−0.05	–	–		
Input Current	I_I		–	–	–	–	–	–	10	–	–	–	–	pA	–

+Bit inputs driven from low-impedance driver.



CD4039A

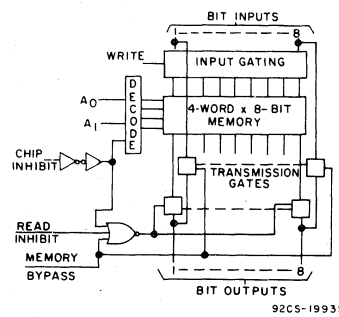


Fig.1 – CD4036A – Logic block diagram.

Write (Pin 2)	Read Inhibit (Pin 21)	Memory Bypass (Pin 11)	Chip Inhibit (Pin 22)	Operating Mode
X	X	L	H	Chip Inhibited (Outputs float)
X	X	H	H	Input/Output Shunted to output; No Reading from Memory;
L	X	H	L	Information in Memory Undisturbed
H	X	H	L	Input/Output Shunted to output; No Reading from Memory; Write Data into Addressed Word
L	L	L	L	Read Data from Addressed Word Write Deactivated
L	H	L	L	Read/Write Deactivated (Outputs float)
H	L	L	L	Read from Memory while Writing Data into Addressed Word
H	H	L	L	Write Data into Addressed Word Read Deactivated (outputs float)

Fig.2 – Operating-mode truth table.

A1 Pin 1	A0 Pin 23	Addressed Word
L	L	Word 1
L	H	Word 2
H	L	Word 3
H	H	Word 4

L = Low-Level Voltage,
H = High-Level Voltage

Fig.3 – Address truth table.

CD4036A, CD4039A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C and C_L = 15 pF
Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	CD4036AD, CD4036AK CD4039AD, CD4039AK				UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS
			V_{DD} Volts	Min.	Typ.	Max.		
Read Delay Time: (Access time) Read Inhibit (RI)	t_{rd}	OUTPUT TIED THROUGH 100 kΩ TO V_{SS} FOR DATA OUTPUT "HIGH" AND TO V_{DD} FOR DATA OUTPUT "LOW"	5	–	375	750	ns	4,5
			10	–	150	300	Note 4	
Chip Inhibit (CI)			5	–	500	1000	ns	4,5
			10	–	200	400	Note 4	
Memory Bypass (MB)			5	–	375	750	ns	4,5
			10	–	150	300		
Address[1] (ADD)			5	–	500	1000	ns	4,5,8
			10	–	200	400		
Write Set-up Time[2]	t_{WS}		5	250	125	–	ns	4,5
			10	100	50	–		
Write Removal Time[3]	t_{WR}		5	0	0	–	ns	4,5
			10	0	0	–		
Write Pulse Duration	t_W		5	150	75	–	ns	4,5
			10	60	30	–		
Data Set-up Time[5]	t_{DS}		5	–	0	0*	ns	4,5
			10	–	0	0*		
Data Overlap Time[6]	t_{DO}		5	100●	50	–	ns	4,5
			10	40●	20	–		
Output Transition Time	t_{THL}, t_{TLH}		5	–	200	400	ns	9
			10	–	100	200		
Input Capacitance	C_I	Any Input		–	5	–	pF	–

1. For CD4036A only, remove 100-kΩ test condition and write all 1's in word one, and all 0's in word two, or vice-versa.
2. Delay from change of ADDRESS or CHIP-INHIBIT signals to application of WRITE pulse.
3. Delay from removal of WRITE pulse to change of ADDRESS or CHIP-INHIBIT signals.
4. Values for CD4036AD & 4036AK only.
5. The time that DATA signal must be present before the WRITE pulse removal.
   * Max. indicates satisfactory operation if t_{DS} equals or exceeds this value.
6. The time that DATA signal must remain present after the WHITE pulse removal.
   ● Min. indicates satisfactory operation if t_{DO} equals or exceeds this value.

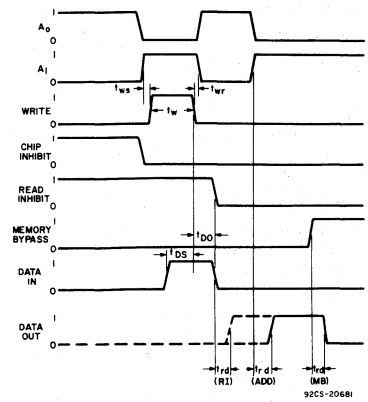


Fig.4—CD4036A Timing Diagram.

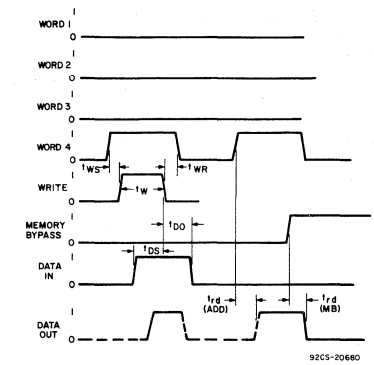


Fig.5—CD4039A Timing Diagram.

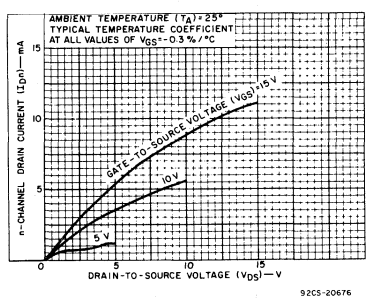


Fig.6—Typical n-channel drain characteristics.

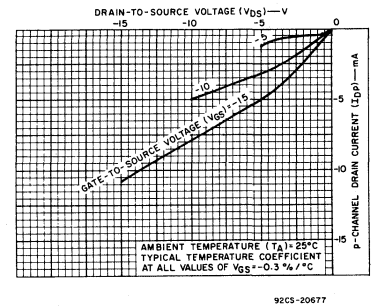


Fig.7—Typical p-channel drain characteristics.

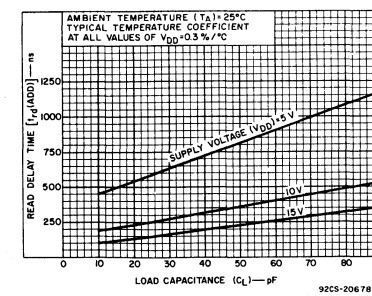


Fig.8—Typical read delay time vs. C_L.

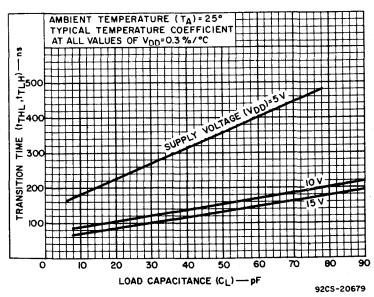


Fig.9—Typical transition time vs. C_L.

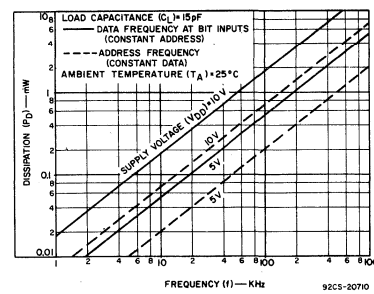


Fig.10—Typical power dissipation vs. frequency.

TEST CIRCUITS

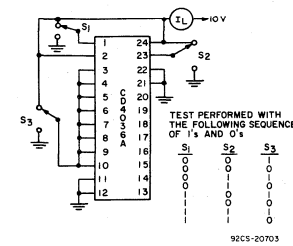


Fig.11—Quiescent current (CD4036A).

TEST CIRCUITS (Cont'd)

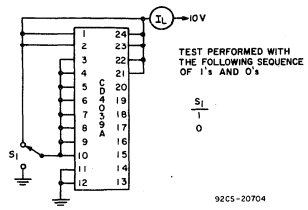


Fig.12–Quiescent current (CD4039A).

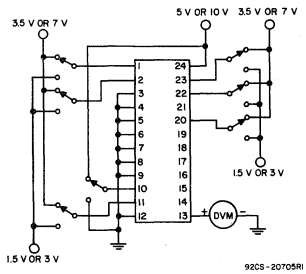
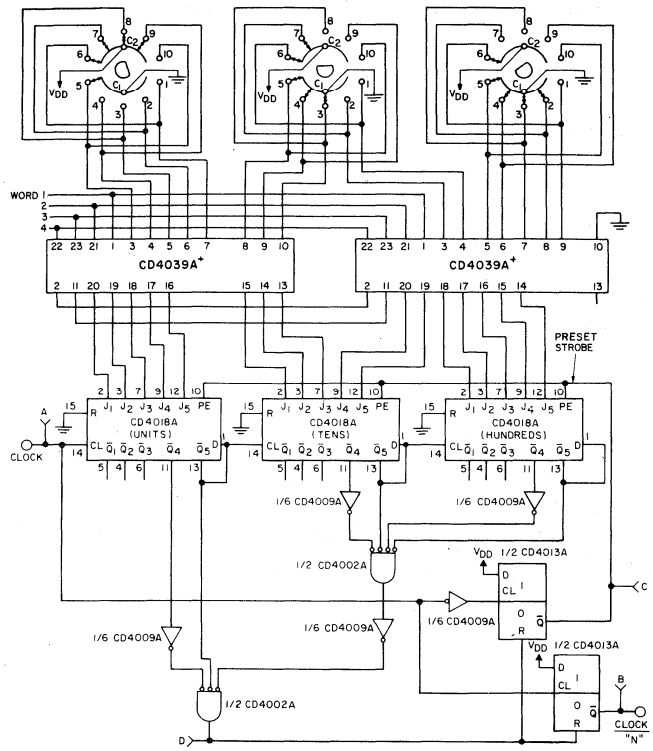


Fig.13–Noise immunity.



Switches shown are GRAYHILL 2-pole switches 50CY23133, CENTRALAB PA160, or equivalent can also be used.

Switches (left to right) read 5-3-2. The equivalent value of "N" for these switch positions (from the Table below) is 3-1-0 or N = 13.

N Value (Front panel notation)	Switch Positions
0	2
1	3
2	4
3	5
4	6
5	7
6	8
7	9
8	10
9	1

+ The CD4036A CAN BE UTILIZED IN A SIMILAR FASHION.

SEE APP. NOTE ICAN-6498 – "DESIGN OF FIXED AND PROGRAMMABLE COUNTERS USING THE RCA CD4018A COS/MOS PRESETTABLE DIVIDE-BY-'N' COUNTER" AND ICAN-6716, "LOW POWER DIGITAL FREQUENCY SYNTHESIZERS UTILIZING COS/MOS IC'S".

Fig.14–Three-decade programmable ÷N counter with 4-channel preset memory settings for frequency synthesizers.

The divide-by-N counter system shown in Fig.14 is programmable from 2 to 999. Four counter-preset words, selected by means of the rotary switches, can be stored in the CD4039A devices and can be read into each CD4018A by simply addressing the proper word. Note that the CD4029A (see Bulletin File No. 503) Presettable Up/Down Counter with BCD decade counting can also be used to perform the basic counting function.

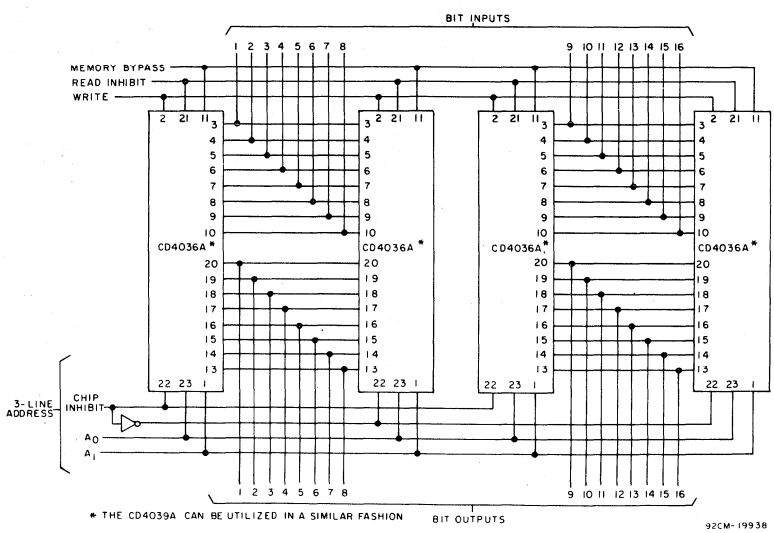


Fig.15–General-purpose memory storage – 8 words x 16 bits (RAM or ROM).

COS/MOS Triple AND/OR Bi-Phase Pairs

The RCA-CD4037A consists of three AND/OR pairs driven by common control signals A and B.

Each circuit has a data input (C), and two output terminals (D and E) that provide outputs in accordance with the truth table shown in Fig. 1. The circuit is useful for coding or decoding signals for split-phase (Bi-phase) communication systems, magnetic recording, and plated wire and core memory systems. A separate V_{CC} terminal is provided to allow level conversion to any voltage from 3 volts to V_{DD}.

These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

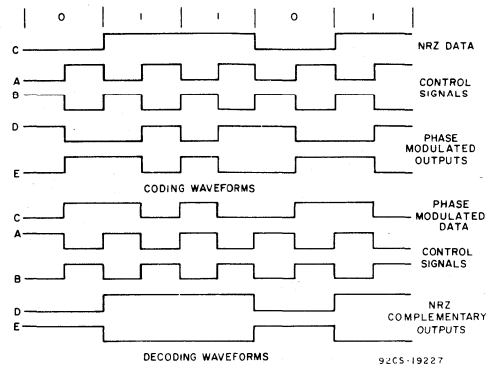
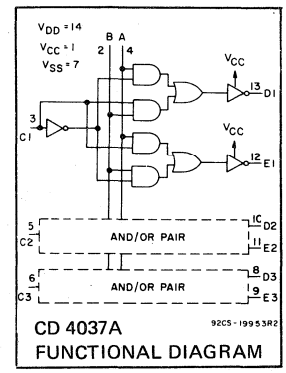
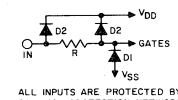


Fig. 1 — Coding and decoding waveforms.



TRUTH TABLE

INPUT		OUTPUT	
A	B	D	E
0	0	1	1
1	0	C	$\overline{C}$
0	1	$\overline{C}$	C
1	1	0	0



RECOMMENDED OPERATING CONDITIONS. For maximum reliability, nominal operating conditions should be selected to that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, K, H PACKAGES		E PACKAGE		
		MIN.	MAX.	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V

CAUTION: V_{CC} VOLTAGE LEVEL MUST BE EQUAL TO OR LESS POSITIVE THAN V_{DD}

DYNAMIC ELECTRICAL CHARACTERISTICS
at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		D, F, K, H PACKAGES			E PACKAGE			
	V_{DD} (V)	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Propagation Delay Time: A and B Inputs t_{PHL}, t_{PLH}	5	—	225	450	—	325	650	ns
	10	—	75	150	—	100	200	
C Inputs t_{PHL}	5	—	250	500	—	350	700	ns
	10	—	75	150	—	100	200	
t_{PLH}	5	—	225	450	—	325	650	
	10	—	90	180	—	125	250	
Transition Time: High-to-Low Level, t_{THL}	5	—	40	80	—	60	120	ns
	10	—	15	30	—	20	40	
Low-to-High Level, t_{TLH}	5	—	75	150	—	100	200	ns
	10	—	60	120	—	90	180	
Input Capacitance, C_I	Any Input	—	5	—	—	5	—	pF

Features:

- **Outputs compatible with low-power TTL systems.**
- **High sink and source current (1.6 mA typ.) capability at $V_{DD} = V_{CC} = 10V$ and $V_{DS} = 0.5$ V.**
- **Microwatt quiescent power dissipation: P_D = 0.5 μW/ceramic pkg. (typ.), P_D = 2 μW/plastic pkg. (typ.) at V_{DD} = 10 V**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Split-phase (Bi-Phase) communication systems.**
- **Disc, drum, and tape digital recording systems.**
- **Plated wire and core memory systems.**
- **High-to-low logic level converter.**

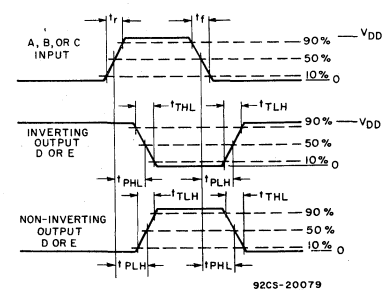


Fig. 2 — Waveforms for measurement of dynamic characteristics.

CD4037A Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . -65 to +150° C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H . . . . . -55 to +125° C

PACKAGE TYPE E . . . . . -40 to +85° C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal) . . . . . -0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = -40 to +60° C (PACKAGE TYPE E) . . . . . 500 mW

FOR T_A = +60 to +85° C (PACKAGE TYPE E) . . Derate Linearly at 12 mW/° C to 200 mW

FOR T_A = -55 to +100° C (PACKAGE TYPES D, F, K) . . . . . 500 mW

FOR T_A = +100 to +125° C (PACKAGE TYPES D, F, K)Derate Linearly at 12 mW/° C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . -0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max . . . . . +265° C

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
				D, K, F, H PACKAGES				E PACKAGE				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	+25 TYP.	+25 LIMIT	+125	-40	+25 TYP.	+25 LIMIT	+85	
Quiescent Device Current, I_L Max.	–	–	5	5	0.03	5	300	50	0.1	50	700	μA
	–	–	10	10	0.05	10	600	100	0.2	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max								V
	–	10	10	0 Typ.; 0.05 Max								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink), I_DN Min.	0.5	–	5	0.85	0.7	1.2	0.45	0.4	0.35	0.7	0.3	mA
	0.5	–	10	1.3	1.1	2	0.7	0.65	0.55	1.1	0.45	
P-Channel (Source): I_DP Min.	4.5	–	5	-0.65	-0.55	-1	-0.35	-0.35	-0.3	-0.55	-0.2	
	9.5	–	10	-0.9	-0.75	-1.6	-0.45	-0.5	-0.4	-0.75	-0.3	
Input Leakage Current, I_{IL}, I_{IH}	Any Input											μA
	–	–	15	±10^{-5} Typ., ±1 Max.								

For quiescent device current, noise immunity, and input leakage current test circuits see "Ratings and Characteristics" at the beginning of the COS/MOS section.

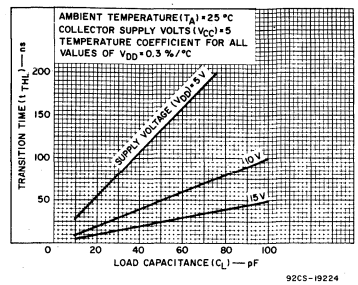


Fig. 3 — Typical transition time vs. load capacitance.

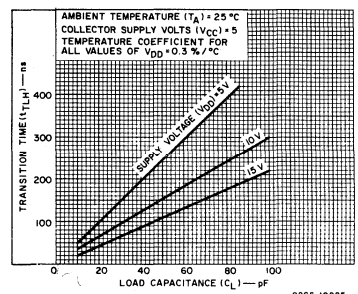


Fig. 4 — Typical transition time vs. load capacitance.

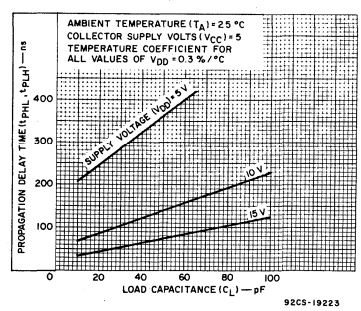


Fig. 5 — Typical propagation delay time vs. load capacitance.

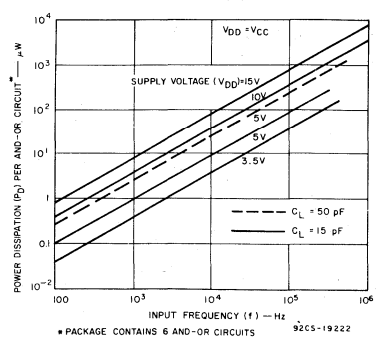


Fig. 6 — Typical dissipation characteristics.

COS/MOS 12-Stage Ripple-Carry Binary Counter/Divider

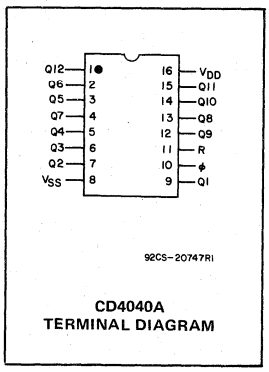
The RCA-CD4040A consists of an input-pulse-shaping circuit and 12 ripple-carry binary counter stages. Resetting the counter to the all-0's state is accomplished by a high-level on the reset line. A master-slave flip-flop configuration is utilized for each counter stage. The state of the counter is advanced one step in binary order on the negative-going transition of the input pulse. All inputs and outputs are fully buffered. These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- Medium-speed operation . . . 5 MHz (typ.) input pulse rate at $V_{DD} - V_{SS} = 10$ V
- Low output impedance . . . 750 Ω (typ.) at $V_{DD} - V_{SS} = 10$ V and $V_{DS} = 0.5$ V
- Common reset
- Fully static operation
- All 12 buffered outputs available
- Low-power TTL compatible
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications:

- Frequency-dividing circuits
- Time-delay circuits
- Control counters



CD4040A TERMINAL DIAGRAM

RECOMMENDED OPERATING CONDITONS at T_A = 25°C, Except as Noted:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges :

CHARACTERISTIC	V_{DD} (V)	LIMITS D,F,K,H Packages Min.	D,F,K,H Packages Max.	LIMITS E Package Min.	E Package Max.	UNITS
Supply Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Input Pulse Width, t_W	5	400	–	500	–	ns
	10	110	–	125	–	
Input-Pulse Frequency, f_ϕ	5	dc	1.5	dc	1.5	MHz
	10	dc	4	dc	4	
Input-Pulse Rise or Fall Time, $t_{r\phi}, t_{f\phi}$	5	15	–	15	–	μs
	10	15	–	15	–	
Reset Pulse Width, t_W	5	1000	–	1250	–	ns
	10	500	–	600	–	

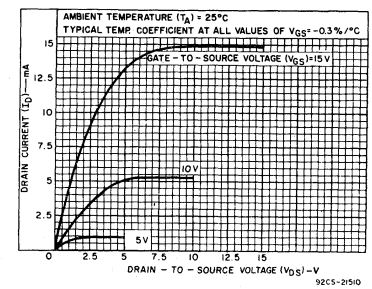


Fig.2 – Typical output n-channel drain characteristics.

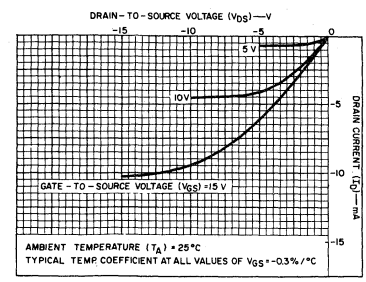


Fig.3 – Typical output p-channel drain characteristics.

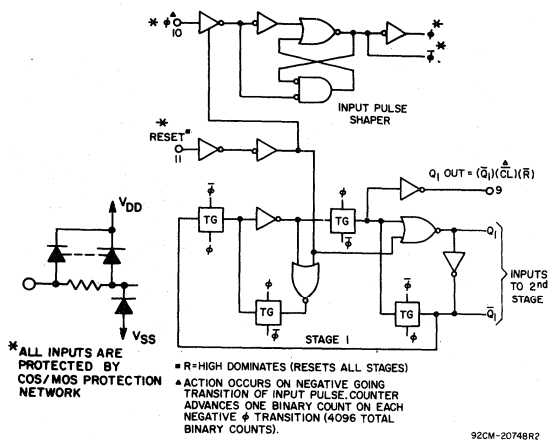


Fig.1 – Logic diagram of CD4040A input pulse shaper and 1 of 12 stages.

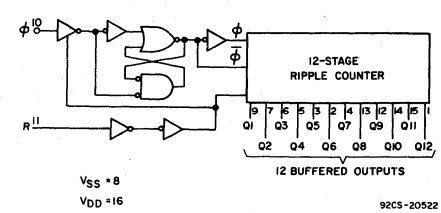


Fig.4 – Functional diagram.

CD4040A Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) ..... −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H ..... −55 to +125°C

PACKAGE TYPE E ..... −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal) ..... −0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = −40 to +60°C (PACKAGE TYPE E) ..... 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) ..... Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) ..... 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

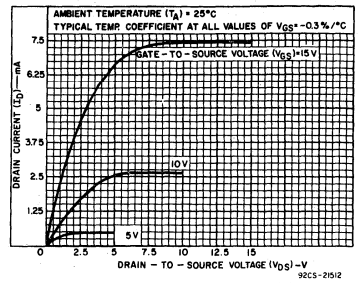


Fig.5 – Minimum output n-channel drain characteristics.

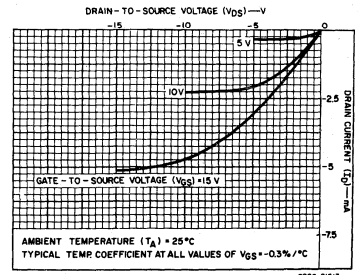


Fig.6 – Minimum output p-channel drain characteristics.

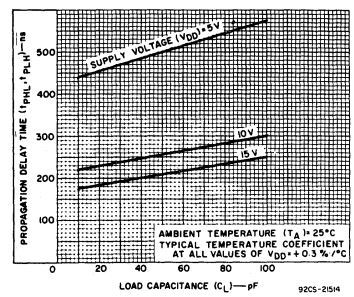


Fig.7 – Typical propagation delay time vs. load capacitance (per stage).

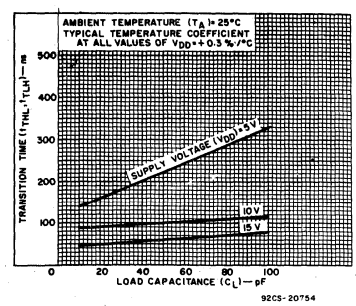


Fig.8 – Typical transition time vs. load capacitance.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				E Package				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	15	0.5	15	900	50	1	50	700	μA
	–	–	10	25	1	25	1500	100	2	100	1400	
	–	–	15	50	2.5	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High-Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink). I_DN Min.	0.5	–	5	0.22	0.36	0.145	0.102	0.21	0.36	0.08	0.056	mA
	0.5	–	10	0.44	0.75	0.4	0.250	0.42	0.75	0.2	0.14	
P-Channel (Source): I_DP Min.	4.5	–	5	−0.15	−0.25	−0.1	−0.07	−0.45	−0.25	−0.06	−0.04	
	9.5	–	10	−0.03	−0.5	−0.25	−0.175	−0.29	−0.5	−0.15	−0.1	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		15	±10^{-5} Typ., ±1 Max.								μA

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

Characteristic	Test Conditions	V_{DD} (V)	LIMITS D,F,K,H Packages Min.	Typ.	Max.	E Package Min.	Typ.	Max.	Units
Input-Pulse Operation									
Propagation Delay Time, t_{PLH}, t_{PHL}●		5	–	450	900	–	450	950	ns
		10	–	225	450	–	225	475	
Transition Time, t_{THL}, t_{TLH}		5	–	150	300	–	150	350	ns
		10	–	75	150	–	75	175	
Maximum Input-Pulse Frequency, f_ϕ		5	1.5	2.5	–	1.5	2.5	–	MHz
		10	4	6	–	4	6	–	
Minimum Input-Pulse Width, t_W	f=100 kHZ	5	–	200	400	–	200	500	ns
		10	–	75	110	–	75	125	
Input-Pulse Rise & Fall Time, $t_{r\phi}$, $t_{f\phi}$▲		5	–	–	15	–	–	15	μs
		10	–	–	7.5	–	–	7.5	
Average Input Capacitance, C_I	Any Input		–	5	–	–	5	–	pF
Reset Operation									
Propagation Delay Time, t_{PHL}*		5	–	500	1000	–	500	1250	ns
		10	–	250	500	–	250	600	
Minimum Reset Pulse Width, t_W		5	–	500	1000	–	500	1250	ns
		10	–	250	500	–	250	600	

● Measured from the 50% level of the negative input pulse edge to the 50% level of either the positive or negative edge of the Q1 output (pin 9); or measured from the negative edge of Q1 through Q11 outputs to the positive or negative edge of the next higher output.

▲ Maximum input rise or fall time for functional operation.

* Measured from the positive edge of the reset pulse to the negative edge of any output (Q1 to Q12).

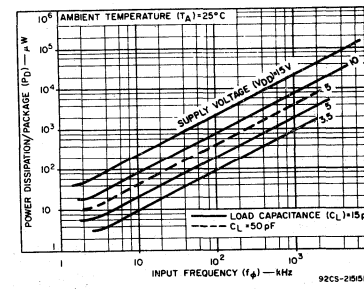


Fig.9 – Typical dissipation characteristics.

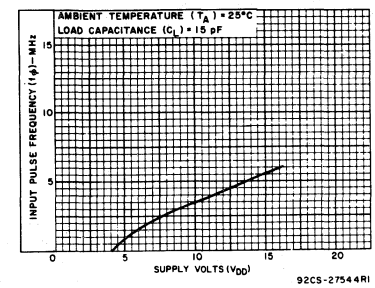


Fig.10 – Typical input-pulse frequency vs. supply voltage.

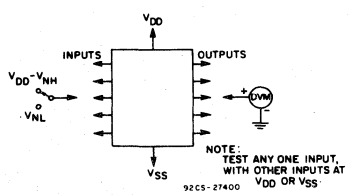


Fig. 11– Noise-immunity test circuit.

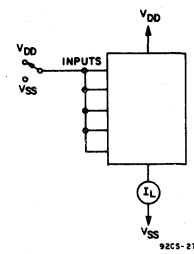


Fig.12 – Quiescent-device-current test circuit.

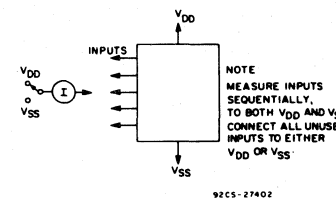
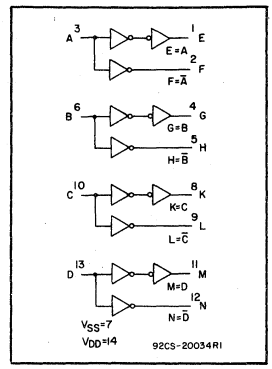


Fig.13 – Input-leakage-current test circuit.

COS/MOS Quad True/Complement Buffer

The RCA-CD4041A types are quad true/complement buffers consisting of n- and p-channel units having low channel resistance and high current (sourcing and sinking) capability. The CD4041A is intended for use as a buffer, line driver, or COS/MOS-to-TTL driver. It can be used as an ultra-low power resistor-network driver for A/D and D/A conversion, as a transmission-line driver, and in other applications where high noise immunity and low-power dissipation are primary design requirements.

These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).



MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) ..... −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H ..... −55 to +125°C

PACKAGE TYPE E ..... −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal) ..... −0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = −40 to +60°C (PACKAGE TYPE E) ..... 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) ..... Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) ..... 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply Voltage Range (For T_A = Full Package Temperature Range)	3	12	V

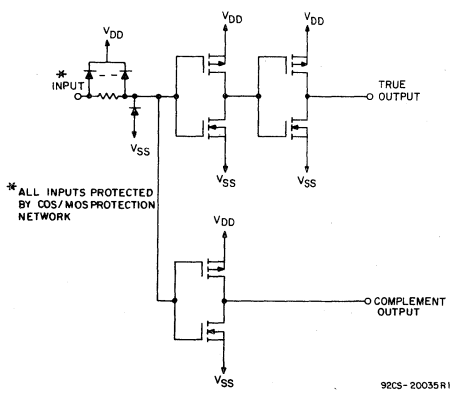


Fig. 1 – CD4041A schematic diagram.

Features:

True Output

- **High current source and sink capability**
  8 mA (typ.) @ V_{DS} = 0.5 V, V_{DD} = 10 V
  3.2 mA (typ.) @ V_{DS} = 0.4 V, V_{DD} = 5 V
  (two TTL loads)

Complement Output

- **Medium current source and sink capability**
  3.6 mA (typ.) @ V_{DS} = 0.5 V, V_{DD} = 10 V
  1.6 mA (typ.) @ V_{DS} = 0.5 V, V_{DD} = 5 V
- **Quiescent current specified to 15 V**
- **Maximum input peakage of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package temperature range)**

Applications:

- **High current source/sink driver**
- **COS/MOS-to-DTL/TTL converter**
- **Display driver**
- **MOS clock driver**
- **Resistor network driver (Ladder or weighted R)**
- **Buffer**
- **Transmission line driver**

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C and C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (Volts)	LIMITS D,F,K,H Packages TYP.	D,F,K,H Packages MAX.	E Package TYP.	E Package MAX.	UNITS
Propagation Delay Time: High-to-Low Level t_{PHL}	True Output	5	65	115	65	140	ns
		10	40	75	40	100	
	Comp. Output	5	55	100	55	125	ns
		10	30	45	30	65	
Low-to-High Level t_{PLH}	True Output	5	75	125	75	150	ns
		10	45	75	45	100	
	Comp. Output	5	45	100	45	125	ns
		10	25	40	25	60	
Transition Time: High-to-Low Level t_{THL}	True Output	5	20	40	20	60	ns
		10	13	25	13	40	
	Comp. Output	5	40	60	40	80	ns
		10	25	40	25	50	
Low-to-High Level t_{TLH}	True Output	5	20	40	20	60	ns
		10	13	25	13	40	
	Comp. Output	5	35	55	35	75	ns
		10	25	40	25	50	
Input Capacitance C_I	Any Input		5	–	5	–	pF

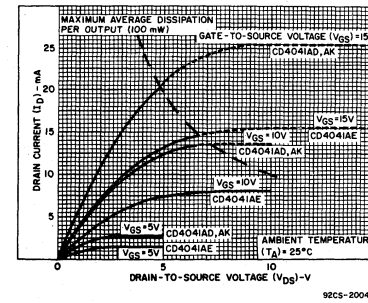


Fig.8 – Minimum output n-channel drain characteristics –complement output.

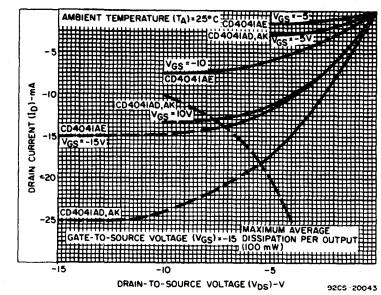


Fig.9 – Minimum output p-channel drain characteristics – complement output.

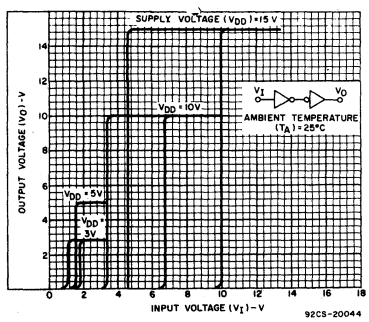


Fig.10 – Minimum and maximum transfer characteristics – true output.

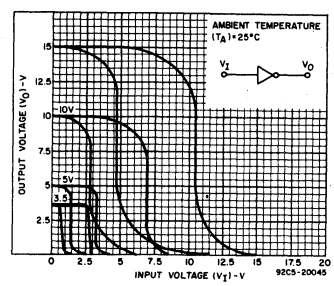


Fig.11 – Minimum and maximum transfer characteristics – complement output.

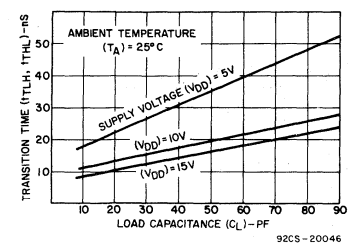


Fig.12 – Typical transition time vs. C_L – true output.

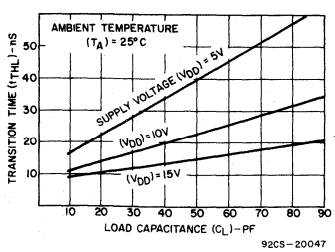


Fig.13 – Typical high-to-low level transition time vs. C_L – complement output.

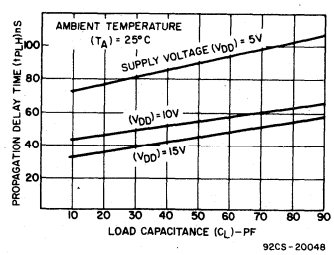


Fig.14 – Typical low-to-high level propagation delay time vs. C_L – true output.

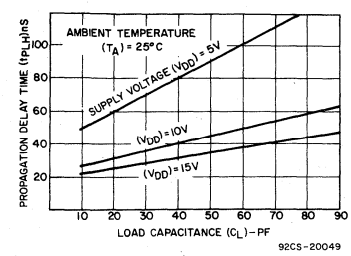


Fig.15 – Typical low-to-high level propagation delay time vs. C_L – complement output.

CD4041A Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				E Package				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	1	0.005	1	60	10	0.01	10	140	μA
	–	–	10	2	0.005	2	120	20	0.02	20	280	
	–	–	15	25	0.25	25	1000	250	2.5	250	2500	
Output Voltage: Low-Level, V_{OL}	–	0.5	5	0 Typ.; 0.05 Max.								V
	–	0.10	10	0 Typ.; 0.05 Max.								
High-Level, V_{OH}	–	0.5	5	4.95 Min.; 5 Typ.								
	–	0.10	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	3.6	–	5	1.5 Min.; 2.25 Typ.								V
	7.2	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}	1.4	–	5	1.5 Min.; 2.25 Typ.								
	2.8	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink), I_{DN} Min.	0.4	True	5	2.1	3.2	1.6	1.2	1	3.2	0.8	0.7	mA
	0.5		10	6.25	10	5	3.5	3	10	2.5	2.2	
	0.5	Comp.	5	1	1.6	0.8	0.55	0.5	1.6	0.4	0.35	
	0.5		10	2.5	4	2	1.4	1.2	4	1	0.9	
P-Channel (Source) I_{DP} Min.	4.5	True	5	−1.75	−2.8	−1.4	−1	−0.85	−2.8	−0.7	−0.6	
	9.5		10	−5	−8	−4	−2.8	−2.4	−8	−2	−1.8	
	4.5	Comp.	5	−0.75	−1.2	−0.6	−0.4	−0.35	−1.2	−0.3	−0.27	
	9.5		10	−2.25	−3.6	−1.8	−1.25	−1.1	−3.6	−0.9	−0.8	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		15	$\pm 10^{-5}$ Typ.; 1 Max.								μA

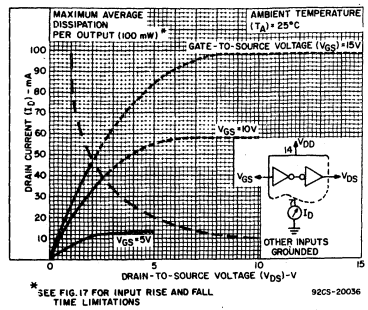


Fig.2 – Typical output n-channel drain characteristics – true output.

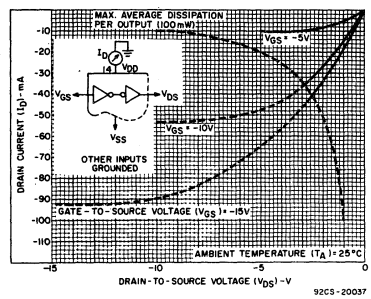


Fig.3 – Typical output p-channel drain cheracteristics – true output.

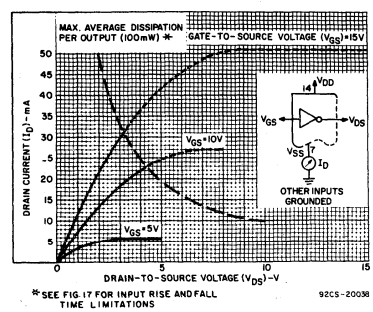


Fig.4 – Typical output n-channel drain characteristics – complement output.

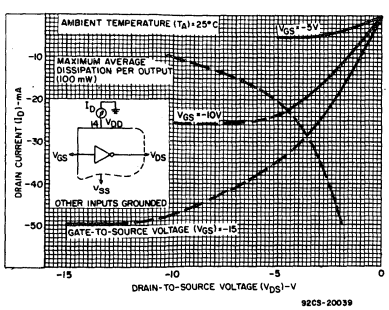


Fig.5 – Typical output p-channel drain characteristics – complement output.

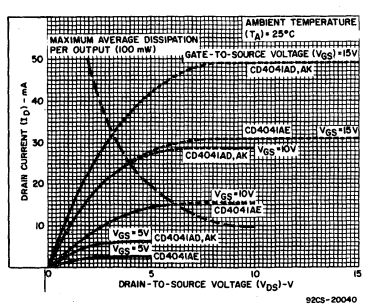


Fig.6 – Minimum output n-channel drain characteristics – true output.

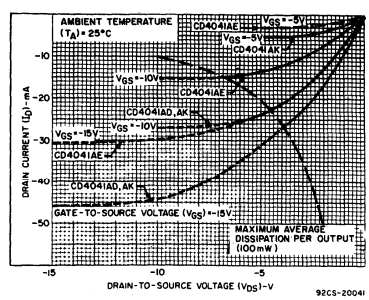


Fig.7 – Minimum output p-channel drain characteristics – true output.

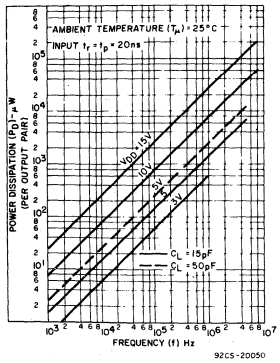


Fig.16 – Typical power dissipation vs. frequency per output pair.

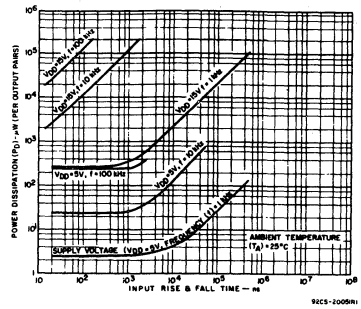


Fig.17 – Typical power dissipation vs. input rise & fall time per output pair.

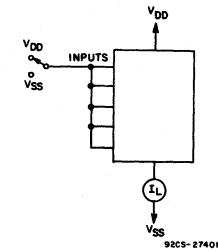


Fig.18 – Quiescent device current test circuit.

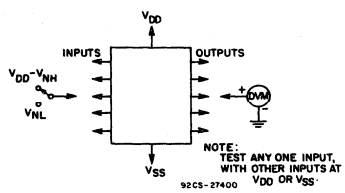


Fig.19 – Noise immunity test circuit.

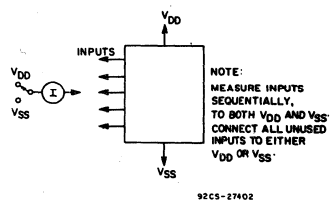


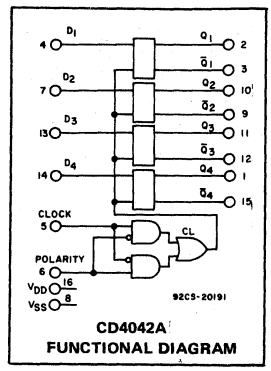
Fig.20 – Input leakage current test circuit.

COS/MOS Quad Clocked "D" Latch

The RCA-CD4042A types contain four latch circuits, each strobed by a common clock. Complementary buffered outputs are available from each circuit. The impedance of the n- and p-channel output devices is balanced and all outputs are electrically identical.

Information present at the data input is transferred to outputs Q and $\overline{Q}$ during the CLOCK level which is programmed by the POLARITY input. For POLARITY = 0 the transfer occurs during the 0 CLOCK level and for POLARITY = 1 the transfer occurs during the 1 CLOCK level. The outputs follow the data input providing the CLOCK and POLARITY levels defined above are present. When a CLOCK transition occurs (positive for POLARITY = 0 and negative for POLARITY = 1) the information present at the input during the CLOCK transition is retained at the outputs until an opposite CLOCK transition occurs.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).



CD4042A
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): . . . . . −0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):
FOR T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max . . . . . +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 KΩ

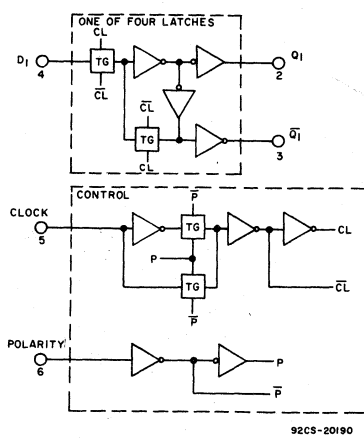
CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D,F,K,H Packages		*E Package*		
		Typ.	Max.	Typ.	Max.	
Propagation Delay Time: t_{PHL}, t_{PLH} Data In to Q	5	150	300	150	400	ns
	10	75	150	75	200	
Data In to $\overline{Q}$	5	250	500	250	600	ns
	10	100	200	100	250	
Clock to Q	5	300	600	300	750	ns
	10	125	250	125	300	
Clock to $\overline{Q}$	5	400	800	400	1000	ns
	10	175	350	175	400	
Transition Time: t_{THL}, t_{TLH}	5	100	200	100	300	ns
	10	50	100	50	150	
Minimum Clock Pulse Width, t_W	5	175	250	175	350	ns
	10	60	120	60	175	
Minimum Hold Time, t_H	5	150	300	150	350	ns
	10	60	120	60	150	
Minimum Setup Time, t_S	5	0	50	0	50	ns
	10	0	30	0	30	
Minimum Clock Rise or Fall Time: t_r, t_f	5	[c] Not rise or fall time sensitive.				μs
	10					
Input Capacitance, C_I (Any Input)	—	5	—	5	—	pF

Features:

- **Clock polarity control**
- **Q and $\overline{Q}$ outputs**
- **Common clock**
- **Low power TTL compatible**
- **Quiescent current specified to 15 V**
- **Maximum input leakage of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Buffer storage**
- **Holding register**
- **General digital logic**



CLOCK	POLARITY	Q
0	0	D
↗	0	LATCH
1	1	D
↘	1	LATCH

Fig. 1 — Logic block diagram & truth table.

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D,F,K,H Packages		*E Package*		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	–	3	12	3	12	V
Clock Pulse Width, t_W	5 10	350 175	– –	250 120	– –	ns
Setup Time, t_S	5 10	50 30	– –	50 30	– –	ns
Hold Time, t_H	5 10	350 150	– –	300 120	– –	ns
Clock Rise or Fall Time: t_r, t_f	5 10	Not rise or fall time sensitive.				μs

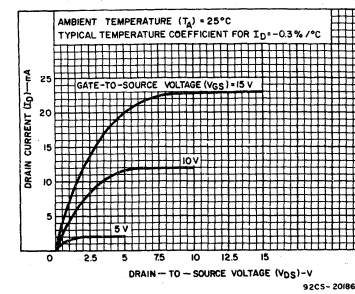


Fig. 2 – Typical output n-channel drain characteristics.

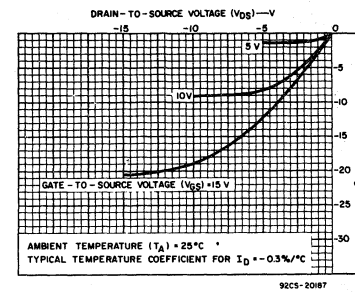


Fig. 3 – Typical output p-channel drain characteristics.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				*E Package*				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	+25 Typ.	+25 Limit	+125	–40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	1	0.005	1	60	10	0.01	10	140	μA
	–	–	10	2	0.005	2	120	20	0.02	20	280	
	–	–	15	25	0.25	25	1000	250	2.5	250	2500	
Output Voltage: Low-Level, V_{OL}	–	0,5	5	0 Typ.; 0.05 Max.								V
	–	0,10	10	0 Typ.; 0.05 Max.								
High Level, V_{OH}	–	0,5	5	4.95 Min.; 5 Typ.								
	–	0,10	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: n-Channel (Sink), I_DN Min.	0.5	–	5	0.5	1	0.4	0.27	0.24	1	0.2	0.18	mA
	0.5	–	10	1.25	2	1	0.7	0.6	2	0.5	0.45	
p-Channel (Source), I_DP Min.	4.5	–	5	-0.45	-1	-0.35	-0.25	-0.2	-1	-0.175	-0.15	
	9.5	–	10	-1.15	-2	-0.9	-0.6	-0.34	-2	-0.45	-0.4	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		15	$\pm 10^{-5}$ Typ.; 1 Max.								μA

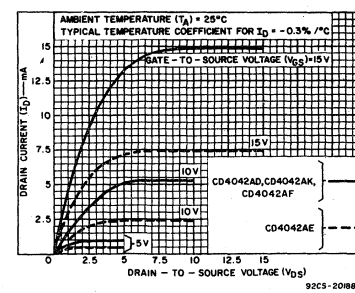


Fig. 4 – Minimum n-channel drain characteristics.

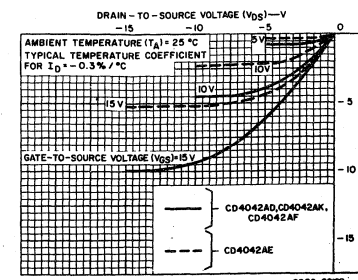
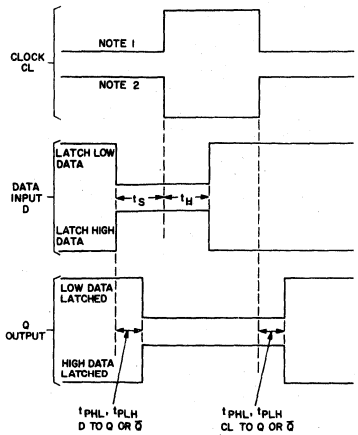
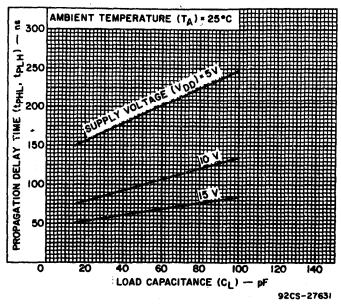


Fig. 5 – Minimum p-channel drain characteristics.



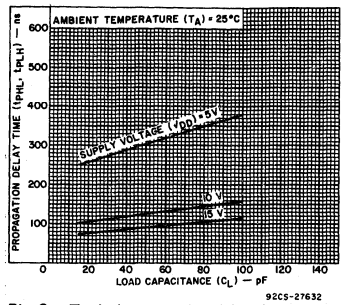
NOTES:
1. FOR POSITIVE CLOCK EDGE, INPUT DATA IS LATCHED WHEN POLARITY IS LOW.
2. FOR NEGATIVE CLOCK EDGE, INPUT DATA IS LATCHED WHEN POLARITY IS HIGH.

92CS-27630



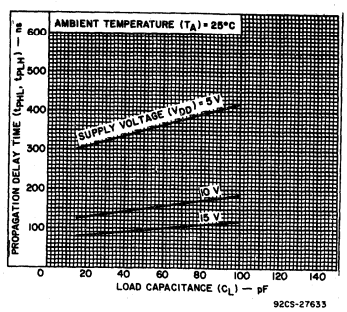
92CS-27631

Fig. 7 – Typical propagation delay time vs. load capacitance– data to Q.



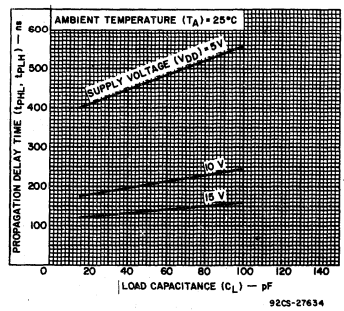
92CS-27632

Fig. 8 – Typical propagation delay time vs. load capacitance – data to $\overline{Q}$.



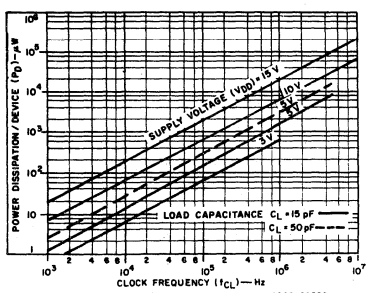
92CS-27633

Fig. 9 – Typical propagation delay time vs. load capacitance – clock to Q.



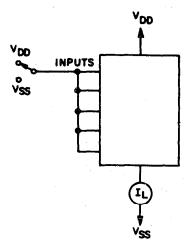
92CS-27634

Fig. 10 – Typical propagation delay time vs. load capacitance – clock to $\overline{Q}$.



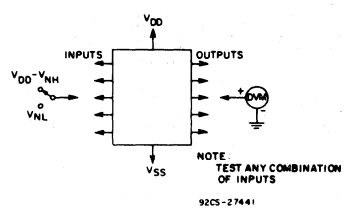
92CS-20200

Fig. 11 – Typical dissipation characteristics.



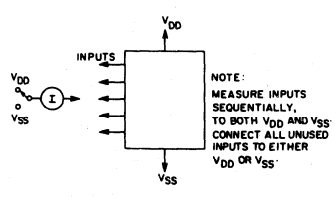
92CS-27401

Fig. 12 – Quiescent device current test circuit.



92CS-27441

Fig. 13 – Noise immunity test circuit.



92CS-27402

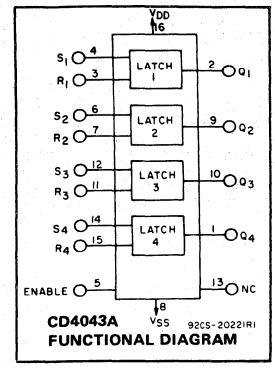
Fig. 14 – Input leakage current test circuit.

COS/MOS Quad 3-State R/S Latches

Quad NOR R/S Latch – CD4043A
Quad NAND R/S Latch – CD4044A

The RCA-CD4043A types are quad cross-coupled 3-state COS/MOS NOR latches and the CD4044A types are quad cross-coupled 3-state COS/MOS NAND latches. Each latch has a separate Q output and individual SET and RESET inputs. The Q outputs are controlled by a common ENABLE input. A logic "1" or high on the ENABLE input connects the latch states to the Q outputs. A logic "0" or low on the ENABLE input disconnects the latch states from the Q outputs, resulting in an open circuit condition on the Q outputs. The open circuit feature allows common busing of the outputs. The logic operation of the latches is summarized in the truth table shown in Fig. 1

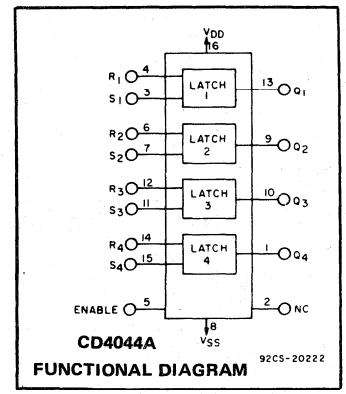
These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).



FUNCTIONAL DIAGRAM

Applications:

- **Holding register in multi-register system**
- **Four bits of independent storage with output ENABLE**
- **Strobed register**
- **General digital logic**



FUNCTIONAL DIAGRAM

Features:

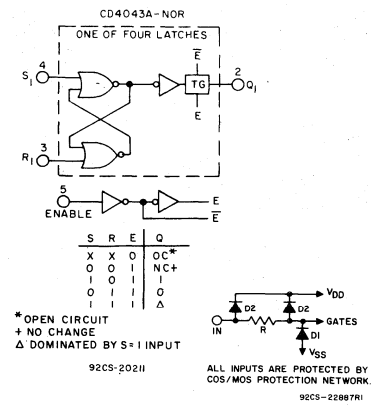
- **3-Level outputs with common output ENABLE**
- **Separate SET and RESET inputs for each latch**
- **NOR and NAND configurations**
- **Quiescent current specified to 15 V**
- **Maximum input leakage of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
  PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
  PACKAGE TYPE E . . . . . –40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
  (Voltages referenced to V_{SS} Terminal): . . . . . –0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):
  FOR T_A = –40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
  FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
  FOR T_A = –55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
  FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
  FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ± 1/32 inch (1.59 ±0.79 mm) from case for 10 s max . . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D,F,K,H Packages		*E Package*		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package Temperature Range	–	3	12	3	12	V
Set or Reset Pulse Width, t_W	5 10	200 100	– –	225 110	– –	ns



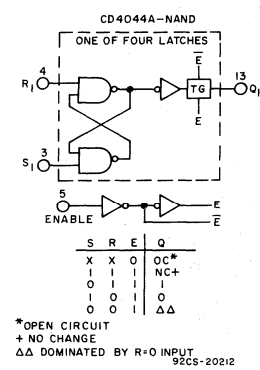


Fig. 1 — Logic diagrams and truth tables.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				E Package				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	1	0.005	1	60	10	0.01	10	140	μA
	–	–	10	2	0.005	2	120	20	0.02	20	280	
	–	–	15	25	0.25	25	1000	250	2.5	250	2500	
Output Voltage: Low-Level, V_{OL}	–	0,5	5	0 Typ.; 0.05 Max.								V
	–	0,10	10	0 Typ.; 0.05 Max.								
High Level, V_{OH}	–	0,5	5	4.95 Min.; 5 Typ.								
	–	0,10	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.;								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: n-Channel (Sink), I_DN Min.	0.5	–	5	0.25	0.5	0.2	0.19	0.12	0.5	0.1	0.09	mA
	0.5	–	10	0.61	1	0.5	0.35	0.3	1	0.25	0.22	
p-Channel (Source), I_DP Min.	4.5	–	5	-0.22	-0.5	-0.175	-0.12	-0.11	-0.5	-0.09	-0.08	
	9.5	–	10	-0.5	-1	-0.4	-0.28	-0.24	-1	-0.2	-0.18	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		15	$\pm 10^{-5}$ Typ.; ±1 Max.								μA

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS D,F,K,H Packages Typ.	LIMITS D,F,K,H Packages Max.	LIMITS E Package Typ.	LIMITS E Package Max.	UNITS
Propagation Delay Time: t_{PHL}, t_{PLH} SET or RESET to Q	5	175	350	175	400	ns
	10	75	175	75	200	
3-State Propagation Delay Time: ENABLE to Q t_{PHZ}, t_{PZH}	5	100	200	100	200	ns
	10	50	100	50	100	
t_{PLZ}, t_{PZL}	5	80	160	80	160	ns
	10	40	80	40	80	
Transition Time: t_{THL}, t_{PLH}	5	100	200	100	250	ns
	10	50	100	50	125	
Minimum SET or RESET Pulse Width, t_W	5	80	200	80	225	ns
	10	40	100	40	110	
Average Input Capacitance, C_I (Any Input)	–	5	–	5	–	pF

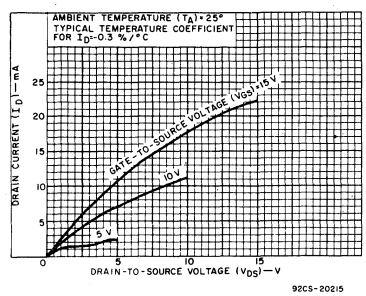


Fig.2 — Typical output n-channel drain characteristics.

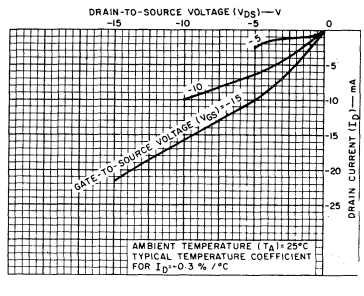


Fig. 3 — Typical output p-channel drain characteristics.

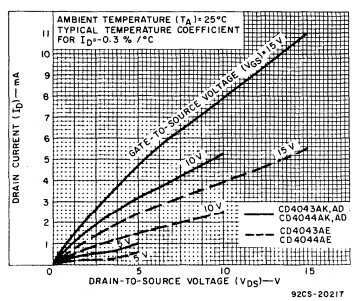


Fig. 4 — Minimum n-channel drain characteristics.

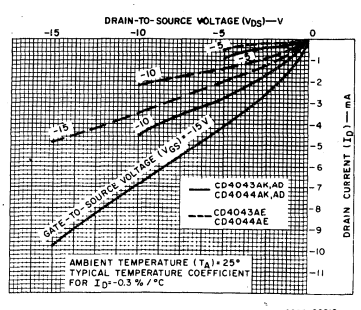


Fig. 5 — Minimum p-channel drain characteristics.

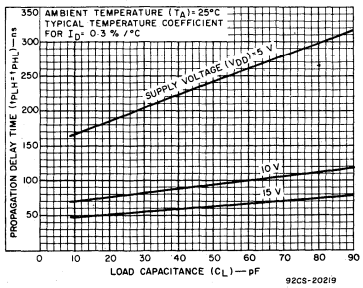


Fig. 6 – Typical propagation delay time vs. C_L.

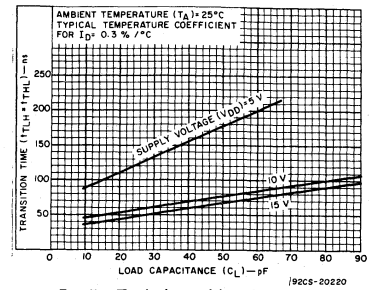


Fig. 7 – Typical transition time vs. C_L.

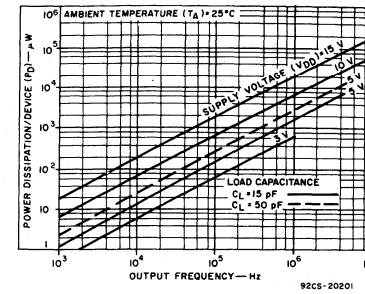


Fig. 8 – Typical dissipation characteristics.

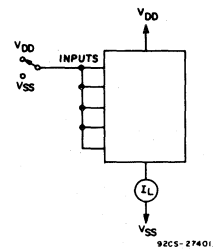


Fig. 9 – Quiescent device current test circuit.

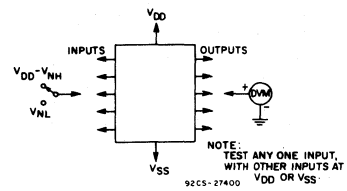


Fig. 10 – Noise immunity test circuit.

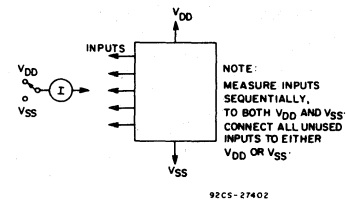


Fig. 11 – Input leakage current test circuit.

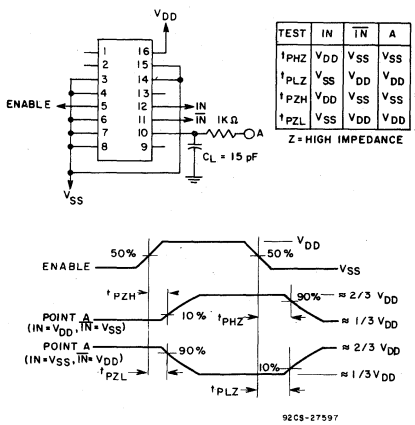


Fig. 12 – ENABLE propagation delay time test circuit and waveforms.

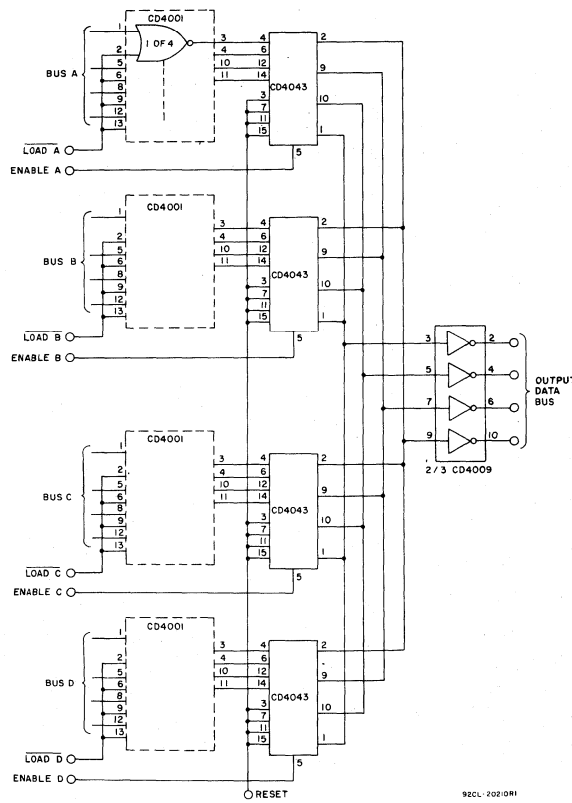


Fig. 14 – Multiple bus storage.

APPLICATIONS

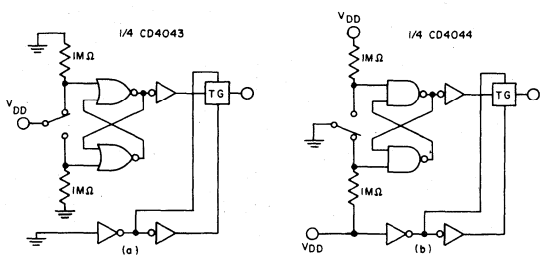


Fig. 13 – Switch bounce eliminator.

COS/MOS 21-Stage Counter

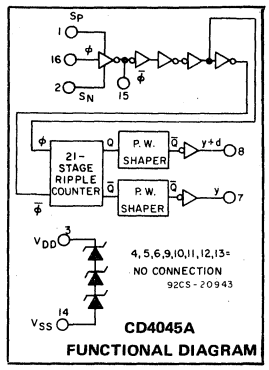
The RCA-CD4045A is a timing circuit consisting of 21 counter stages, two output-shaping flip-flops, two inverter output drivers, three 5.5-V zener diodes (providing transient protection at 16.5 V), and input inverters for use in a crystal oscillator. The CD4045A configuration provides 21 flip-flop counting stages, and two flip-flops for shaping the output waveform for a 3.125% duty cycle. Push-pull operation is provided by the inverter output drivers.

The first inverter is intended for use as a crystal oscillator/amplifier. However, it may be used as a normal logic inverter if desired. A crystal oscillator circuit can be made less sensitive to voltage-supply variations by the use of source resistors. In this device, the sources of the p and n transistors have been brought out to package terminals. If external resistors are not required, the sources must be shorted to their respective substrates (S_p to V_{DD}, S_n to V_{SS}). See Fig. 3.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

Applications:

- **Digital equipment in which ultra-low dissipation and/or operation using a battery source are primary design requirements.**
- **Accurate timing from a crystal oscillator for timing applications such as wall clocks, table clocks, automobile clocks, and digital timing references in any circuit requiring accurately timed outputs at various intervals in the counting sequence.**
- **Driving miniature synchronous motors, stepping motors, or external bipolar transistors in push-pull fashion.**



Features:

- **Microwatt quiescent dissipation . . . . . 2.5 μW (typ.) @ V_{DD} = 5 V; 10 μW (typ.) @ V_{DD} = 10 V**
- **Very low operating dissipation . . . . . 1 mW (typ.); @ V_{DD} = 5 V, fϕ = 1 MHz**
- **Output drivers with sink or source capability . . . . . 7 mA (typ.) @ V_O = 0.5 V, V_{DD} = 5 V (sink) 5 mA (typ.) @ V_O = 4.5 V, V_{DD} = 5 V (source)**
- **Medium speed (typ.) . . . . . fϕ = 5 MHz @ V_{DD} = 5 V fϕ = 10 MHz @ V_{DD} = 10 V**
- **16.5 V zener diode transient protection on chip for automotive use**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C

PACKAGE TYPE E . . . . . –40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal): . . . . . –0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = –40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = –55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max . . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D,F,K,H Packages		*E Package*		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)		3	12	3	12	V
Input-Pulse Width, t_W	5 10	115 60	– –	140 75	– –	ns
Input-Pulse Frequency, fϕ	5 10	dc dc	4.4 8.5	dc dc	3.5 6.5	MHz
Input-Pulse Rise or Fall Time, $t_r\phi$, $t_f\phi$	5 10	– –	15 10	– –	15 10	μs

NOTE 1: To minimize power dissipation in the zener diodes, and to ensure device dissipation less than 200 mW, a 150 Ω current-limiting resistor must be placed in series with the power supply for V_{DD} > 13 V.

NOTE 2: Observe power-supply terminal connections, V_{DD} is terminal No. 3 and V_{SS} is terminal No. 14 (not 16 and 8 respectively, as in all other CD4000A Series 16-lead devices).

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		D,F,K,H Packages			*E Package*			
	V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
Propagation Delay Time: ϕ to y or y+d out t_{PLH}, t_{PHL}	5	–	2.2	4.4	–	2.2	5.5	μs
	10	–	1.2	2.4	–	1.2	3.3	
Transition Time: t_{THL}, t_{TLH}	5	–	450	800	–	450	900	ns
	10	–	375	650	–	375	750	
Maximum Input-Pulse Frequency, $f_{m\phi}$	5	4.4	5	–	3.5	5	–	MHz
	10	8.5	10	–	6.5	10	–	
Minimum Input-Pulse Width, t_W	5	–	100	115	–	100	140	ns
	10	–	50	60	–	50	75	
Input-Pulse Rise & Fall Time; $t_r\phi$, $t_f\phi$	5	–	–	15	–	–	15	μs
	10	–	–	10	–	–	10	
Average Input Capacitance, C_I	Any Input	–	5	–	–	5	–	pF

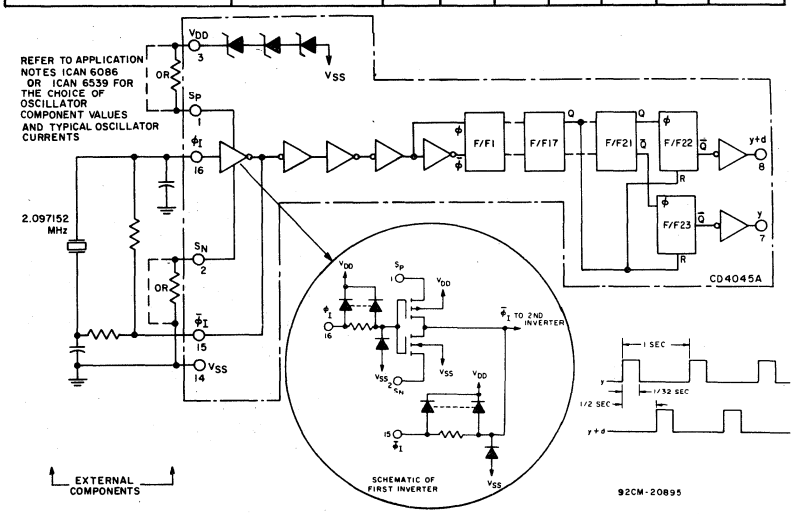


Fig. 3 – CD4045A and outboard components in a typical 21-stage counter application.

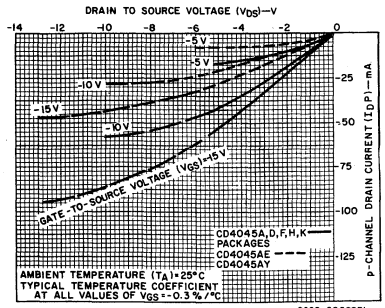


Fig. 5 – Minimum output p-channel drain characteristics.

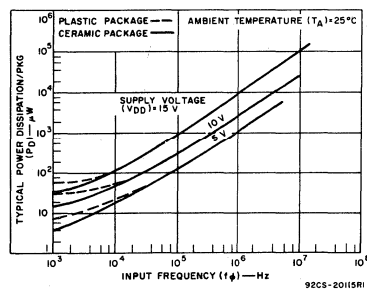


Fig. 6 – Typical dissipation vs input frequency (21 counting stages).

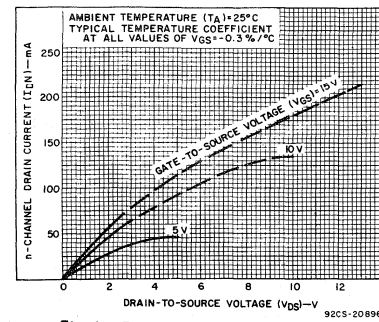


Fig. 1 – Typical output n-channel drain characteristics.

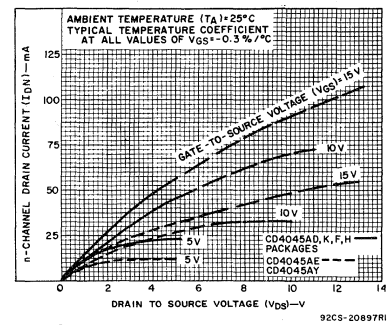


Fig. 2 – Minimum output n-channel drain characteristcs.

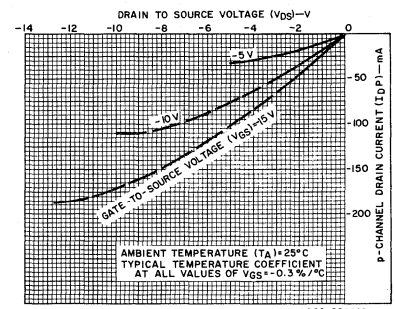


Fig. 4 – Typical output p-channel drain characteristics.

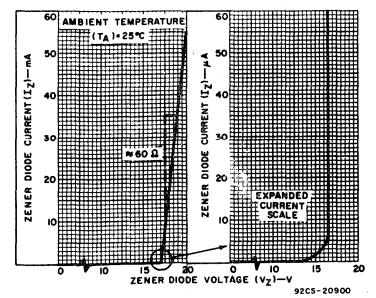


Fig. 7 – Typical zener diode characteristics.

CD4045A Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				E Package				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current I_L Max.	–	–	5	15	0.5	15	900	50	1	50	700	μA
	–	–	10	25	1	25	1500	100	2	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: n-Channel (Sink) I_{DN} Min.	0.5	–	5	4.4	7	3.5	2.5	2.2	7	1.8	1.3	mA
	0.5	–	10	6.9	11	5.5	3.9	3.5	11	2.8	2	
p-Channel (Source): I_{DP} Min.	4.5	–	5	−3.1	−5	−2.5	−1.8	−1.6	−5	−1.3	−0.9	
	9.5	–	10	−5.6	−9	−4.5	−3.2	−2.8	−9	−2.3	−1.6	
Input Leakage Current, I_{IL}, I_{IH}	Any Input –	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								μA
Zener Breakdown Voltage, $V_{(BR)Z}$	1–100 μA		Min.	13.3	–	13.5	13.7	13.3	–	13.5	13.6	V
			Typ.	–	16.5	–	–	–	16.5	–	–	
			Max.	17.8	–	18	18.2	17.8	–	18	18.1	

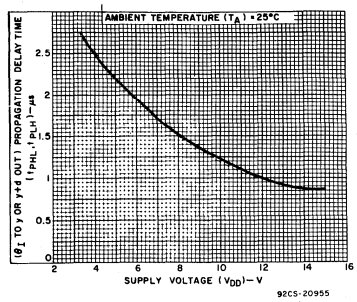


Fig. 8 – Typical propagation delay (ϕ_1 to y or y+d out) vs V_{DD}.

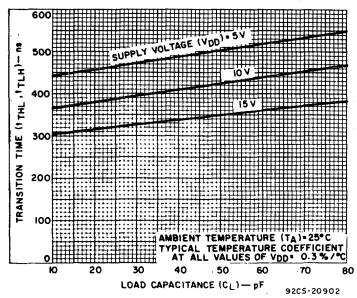


Fig. 9 – Typical transition time vs C_L.

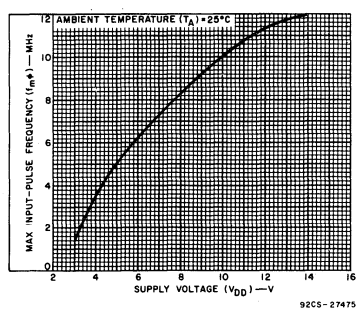


Fig. 10 – Typical maximum input-pulse frequency.

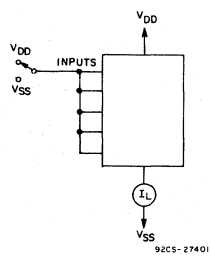


Fig. 11 – Quiescent-device-current test circuit.

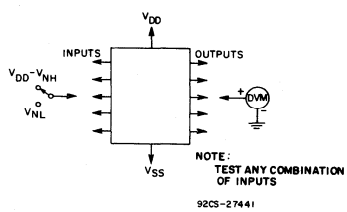


Fig. 12 – Noise-immunity test circuit.

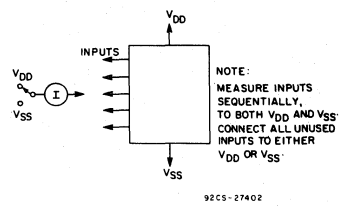


Fig. 13 – Input-leakage-current test circuit.

COS/MOS Micropower Phase-Locked Loop

The RCA-CD4046A COS/MOS Micropower Phase-Locked Loop (PLL) consists of a low-power, linear voltage-controlled oscillator (VCO) and two different phase comparators having a common signal-input amplifier and a common comparator input. A 5.2-V zener diode is provided for supply regulation if necessary. The CD4046A is supplied in a 16-lead dual-in-line ceramic package (CD4046AD), a 16-lead dual-in-line plastic package (CD4046AE), and a 16-lead flat pack (CD4046AK). It is also available in chip form (CD4046AH).

VCO Section

The VCO requires one external capacitor C1 and one or two external resistors (R1 or R1 and R2). Resistor R1 and capacitor C1 determine the frequency range of the VCO and resistor R2 enables the VCO to have a frequency offset if required. The high input impedance ($10^{12}\Omega$) of the VCO simplifies the design of low-pass filters by permitting the designer a wide choice of resistor-to-capacitor ratios. In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided at terminal 10 (DEMODULATED OUTPUT). If this terminal is used, a load resistor (R_S) of 10 kΩ or more should be connected from this terminal to V_{SS}. If unused this terminal should be left open. The VCO can be connected either directly or through frequency dividers to the comparator input of the phase comparators. A full COS/MOS logic swing is available at the output of the VCO and allows direct coupling to COS/MOS frequency dividers such as the RCA-CD4024, CD4018, CD4020, CD4022, CD4029, and CD4059. One or more CD4018 (Preset-table Divide-by-N Counter) or CD4029 (Presettable Up/Down Counter), or CD4059A (Programmable Divide-by-"N" Counter), together with the CD4046A (Phase-Locked Loop) can be used to build a micropower low-frequency synthesizer. A logic 0 on the INHIBIT input "enables" the VCO and the source follower, while a logic 1 "turns off" both to minimize stand-by power consumption.

Phase Comparators

The phase-comparator signal input (terminal 14) can be direct-coupled provided the signal swing is within COS/MOS logic levels [logic "0" ≤30% ($V_{DD}-V_{SS}$), logic "1" ≥ 70% ($V_{DD}-V_{SS}$)]. For smaller swings the signal must be capacitively coupled to the self-biasing amplifier at the signal input.

Phase comparator I is an exclusive-OR network; it operates analagously to an overdriven balanced mixer. To maximize the lock range, the signal- and comparator-input frequencies must have a 50% duty cycle. With no signal or noise on the signal input, this phase comparator has an average output voltage equal to $V_{DD}/2$. The low-pass filter connected to the output of phase comparator I supplies the averaged voltage to the VCO input, and causes the VCO to oscillate at the center frequency (f_o).

The frequency range of input signals on which the PLL will lock if it was initially out of lock is defined as the frequency capture range ($2f_C$).

The frequency range of input signals on which the loop will stay locked if it was initially in lock is defined as the frequency lock range ($2f_L$). The capture range is ≤ the lock range.

With phase comparator I the range of frequencies over which the PLL can acquire lock (capture range) is dependent on the low-pass-filter characteristics, and can be made as large as the lock range. Phase-comparator I enables a PLL system to remain in lock in spite of high amounts of noise in the input signal.

One characteristic of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the VCO center-frequency. A second characteristic is that the phase angle between the signal and the comparator input varies between 0° and 180°, and is 90° at the center frequency. Fig. 2 shows the typical, triangular, phase-to-output response characteristic

Features:

- **Very low power consumption: 70 μW (typ.) at VCO f_o = 10 kHz, V_{DD} = 5 V**
- **Operating frequency range up to 1.2 MHz (typ.) at V_{DD} = 10 V**
- **Wide supply-voltage range: $V_{DD} - V_{SS}$ = 5 to 15 V**
- **Low frequency drift: 0.06%/°C (typ.) at V_{DD} = 10 V**
- **Choice of two phase comparators:**
  1. **Exclusive-OR network**
  2. **Edge-controlled memory network with phase-pulse output for lock indication**
- **High VCO linearity: 1% (typ.)**
- **VCO inhibit control for ON-OFF keying and ultra-low standby power consumption**
- **Source-follower output of VCO control input (Demod. output)**
- **Zener diode to assist supply regulation**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**

Applications:

- **FM demodulator and modulator**
- **Frequency synthesis and multiplication**
- **Frequency discriminator**
- **Data synchronization**
- **Voltage-to-frequency conversion**
- **Tone decoding**
- **FSK — Modems**
- **Signal conditioning**
- **(See ICAN-6101) "RCA COS/MOS Phase-Locked Loop — A Versatile Building Block for Micropower Digital and Analog Applications"**

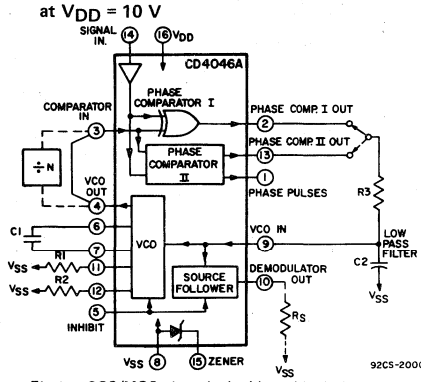


Fig.1 — COS/MOS phase-locked loop block diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) ..... −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H ..... −55 to +125°C

PACKAGE TYPE E ..... −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal) ..... −0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = −40 to +60°C (PACKAGE TYPE E) ..... 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) ..... Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) ..... 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply Voltage Range (For T_A = Full Package Temperature Range	3	12	V

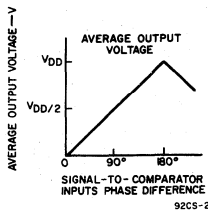


Fig.2 – Phase-comparator I characteristics at low-pass filter output.

of phase-comparator I. Typical waveforms for a COS/MOS phase-locked-loop employing phase comparator I in locked condition of f_o is shown in Fig. 3.

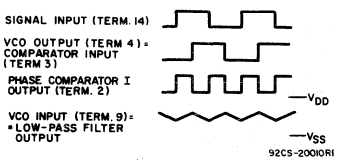


Fig.3 – Typical waveforms for COS/MOS phase-locked loop employing phase comparator I in locked condition of f_o.

Phase-comparator II is an edge-controlled digital memory network. It consists of four flip-flop stages, control gating, and a three-state output circuit comprising p- and n-type drivers having a common output node. When the p-MOS or n-MOS drivers are ON they pull the output up to V_{DD} or down to V_{SS}, respectively. This type of phase comparator acts only on the positive edges of the signal and comparator inputs. The duty cycles of the signal and comparator inputs are not important since positive transitions control the PLL system utilizing this type of comparator. If the signal-input frequency is higher than the comparator-input frequency, the p-type output driver is maintained ON most of the time, and both the n and p drivers OFF (3 state) the remainder of the time. If the signal-input frequency is lower than the comparator-input frequency, the n-type output driver is maintained ON most of the time, and both the n and p drivers OFF (3 state) the remainder of the time. If the signal- and comparator-input frequencies are the same, but the signal input lags the comparator input in phase, the n-type output driver is maintained ON for a time corresponding to the phase difference. If the signal- and comparator-input frequencies are the same, but the comparator input lags the signal in phase, the p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the capacitor voltage of the low-pass filter connected to this phase comparator is adjusted until the signal and comparator inputs are equal in both phase and frequency. At this stable point both p- and n-type output drivers remain OFF and thus the phase comparator output becomes an open circuit and holds the voltage on the capacitor of the low-pass filter constant.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

Characteristic	Test Conditions	V_O Volts	V_{DD} Volts	Limits All Package Types D,E,F,H,K Min.	Typ.	Max.	Units
Phase Comparator Section							
Operating Supply Voltage, $V_{DD}-V_{SS}$	VCO Operation		–	5	–	15	V
	Comparators only		–	3	–	15	
Total Quiescent Device Current, I_L: Term. 14 Open	Term. 15 open, Term. 5 at V_{DD}, Terms. 3 & 9 at V_{SS}		5	–	25	55	μA
			10	–	200	410	
Term. 14 at V_{SS} or V_{DD}			5	–	5	15	
			10	–	25	60	
			15	–	50	500	
Term. 14 (SIGNAL IN) Input Impedance, Z_{14}			5	1	2	–	MΩ
			10	0.2	0.4	–	
			15	–	0.2	–	
AC-Coupled Signal Input Voltage Sensitivity* (peak-to-peak)	See Fig.7		5	–	200	400	mV
			10	–	400	800	
			15	–	700	–	
DC-Coupled Signal Input and Comparator Input Voltage Sensitivity Low Level			5	1.5	2.25	–	V
			10	3	4.5	–	
			15	4.5	6.75	–	
High Level		V_O Volts	5	–	2.75	3.5	
			10	–	5.5	7	
			15	–	8.25	–	
Output Drive Current: n-Channel (Sink), I_{DN}	Phase Comparator I & II Term. 2 & 13	0.5	5	0.43	0.86	–	mA
		0.5	10	1.3	2.5	–	
	Phase Pulses	0.5	5	0.23	0.47	–	
		0.5	10	0.7	1.4	–	
p-Channel (Source), I_{DP}	Phase Comparator I & II Term. 2 & 13	4.5	5	−0.3	−0.6	–	
		9.5	10	−0.9	−1.8	–	
	Phase Pulses	4.5	5	−0.08	−0.16	–	
		9.5	10	−0.25	−0.5	–	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		15	–	$\pm10^{-5}$	±1	μA

* For sine wave, the frequency must be greater than 1 kHz for Phase Comparator II.

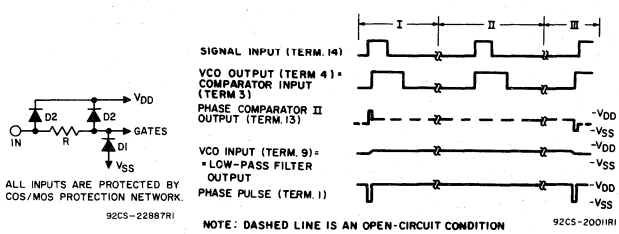


Fig.4 – Typical waveforms for COS/MOS phase-locked loop employing phase comparator II in locked condition.

Moreover the signal at the "phase pulses" output is a high level which can be used for indicating a locked condition. Thus, for phase comparator II, no phase difference exists between signal and comparator input over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both the p- and n-type output drivers are OFF for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator II. Fig. 4 shows typical waveforms for a COS/MOS PLL employing phase comparator II in a locked condition.

DESIGN INFORMATION

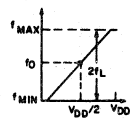
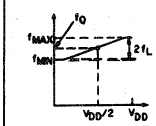
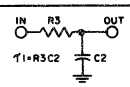
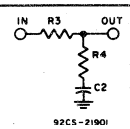
This information is a guide for approximating the values of external components for the CD4046A in a Phase-Locked-Loop system. The selected external components must be within the following ranges:

$10\ k\Omega \leqslant R1, R2, R_S \leqslant 1\ M\Omega$

$C1 \geqslant 100\ pF$ at $V_{DD} \geqslant 5\ V$;

$C1 \geqslant 50\ pF$ at $V_{DD} \geqslant 10\ V$

In addition to the given design information refer to Fig.5 for R1, R2, and C1 component selections.

Characteristics	Phase Comparator Used	Design Information	
VCO Frequency	1	VCO WITHOUT OFFSET $R_2 = \infty$	VCO WITH OFFSET
		 VCO INPUT VOLTAGE	 VCO INPUT VOLTAGE 92CS-20012RI
	2	Same as for No.1	
For No Signal Input	1	VCO will adjust to center frequency, f_o	
	2	VCO will adjust to lowest operating frequency, f_{min}	
Frequency Lock Range, $2f_L$	1	$2f_L$ = full VCO frequency range	
		$2f_L = f_{max} - f_{min}$	
	2	Same as for No.1	
Frequency Capture Range, $2f_C$	1	 $\tau 1 = R3C2$	(1), (2) $2f_C \approx \frac{1}{\pi}\sqrt{\frac{2\pi f_L}{\tau 1}}$
Loop Filter Component Selection		 92CS-21901	For $2f_C$, see Ref. (2)
	2	$f_C = f_L$	
Phase Angle Between Signal and Comparator	1	90^o at center frequency (f_o) approximating 0^o and 180^o at ends of lock range ($2f_L$)	
	2	Always 0^o in lock	

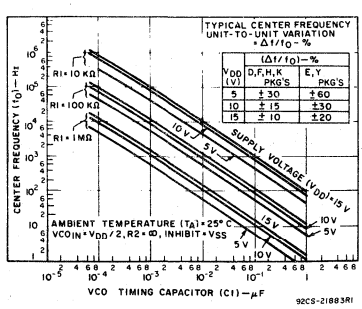


Fig.5(a) — Typical center frequency vs C1 for R1 = 10 kΩ, and 1 MΩ and $f_o \sim 1/R1\ C1$.

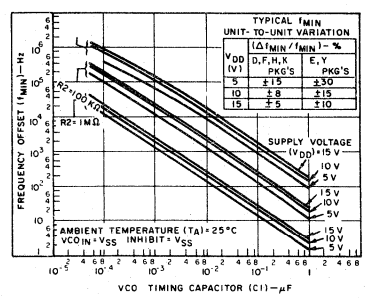


Fig.5(b) — Typical frequency offset vs C1 for R2 = 10 kΩ, 100 kΩ, and 1 MΩ.

NOTE: Lower frequency values are obtainable if larger values of C1 than shown in Figs. 5(a) and 5(b) are used.

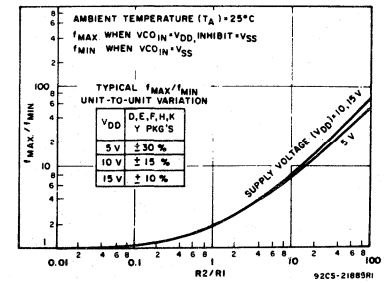


Fig.5(c) — Typical f_{max}/f_{min} vs R2/R1.

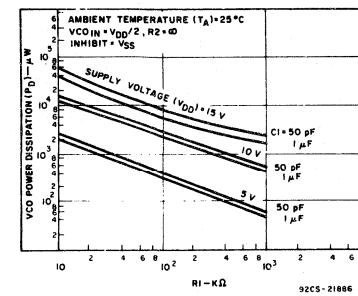


Fig.6(a) — Typical VCO power dissipation at center frequency vs R1.

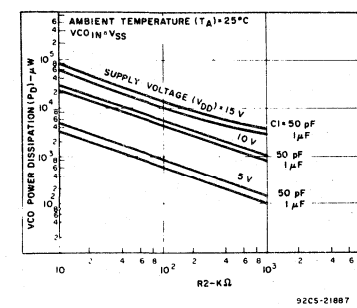


Fig.6(b) — Typical VCO power dissipation at f_{min} vs R2.

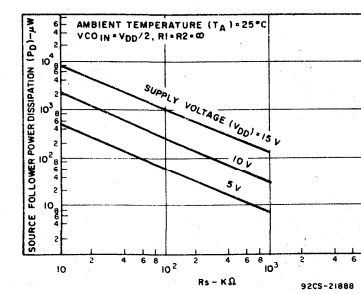


Fig.6(c) — Typical source follower power dissipation vs R_S.

NOTE: To obtain approximate total power dissipation of PLL system for no-signal input

P_D (Total) = P_D (f_o) + P_D (f_{MIN}) + P_D (R_S) — Phase Comparator I

P_D (Total) = P_D (f_{MIN}) — Phase Comparator II

ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$

Characteristic	Test Conditions	V_O Volts	V_{DD} Volts	Limits (All Package Types D,E,F,H,K) Min.	Typ.	Max.	Units
VCO Section							
Operating Supply Voltage $V_{DD}-V_{SS}$	As fixed oscillator only			3	–	15	V
	Phase-lock-loop operation			5	–	15	
Operating Power Dissipation, P_D	f_o = 10 kHz, R_1 = 1 MΩ, R_2 = ∞, $VCO_{IN} = \frac{V_{DD}}{2}$		5	–	70	–	μW
			10	–	600	–	
			15	–	2400	–	
Maximum Operating Frequency, f_{max}	R1 = 10 kΩ, R_2 = ∞, $VCO_{IN} = V_{DD}$, C1 = 100 pF		5	0.25	0.5	–	MHz
			10	0.6	1.2	–	
	C1 = 50 pF		15	–	1.5	–	
Center Frequency (f_o) and Frequency Range, $f_{max}-f_{min}$	Programmable with external components R1, R2, and C1 *See Design Information*						
Linearity	VCO_{IN} = 2.5 V ± 0.3 V, R1 > 10 kΩ		5	–	1	–	%
	= 5 V ± 2.5 V, R1 > 400 kΩ		10	–	1	–	
	= 7.5 V ± 5 V, R1 = 1 MΩ		15	–	1	–	
Temperature-Frequency Stability●: No Frequency Offset $f_{MIN} = 0$	$\%/^oC \propto \frac{1}{f \cdot V_{DD}}$, R2 = ∞		5	–	0.12–0.24	–	%/°C
			10	–	0.04–0.08	–	
			15	–	0.015–0.03	–	
Frequency Offset $f_{MIN} \neq 0$	$\%/^oC \propto \frac{1}{f \cdot V_{DD}}$		5	–	0.06–0.12	–	
			10	–	0.05–0.1	–	
			15	–	0.03–0.06	–	
Input Resistance of VCO_{IN} (Term 9), R_I			5,10,15	–	10^{12}	–	Ω
VCO Output Voltage (Term 4) Low Level, V_{OL}	Driving COS/MOS-Type Load (e.g. Term 3 Phase Comparator Input)		5,10,15	–	–	0.01	V
High Level, V_{OH}			5	4.99	–	–	
			10	9.99	–	–	
			15	14.99	–	–	
VCO Output Duty Cycle			5,10,15	–	50	–	%
VCO Output Transition Times, t_{THL}, t_{TLH}		V_O Volts	5	–	75	150	ns
			10	–	50	100	
			15	–	40	–	
VCO Output Drive Current: n-Channel (Sink), I_{DN}		0.5	5	0.43	0.86	–	mA
		0.5	10	1.3	2.6	–	
p-Channel (Source), I_DP		4.5	5	–0.3	–0.6	–	
		9.5	10	–0.9	–1.8	–	
Source-Follower Output (Demodulated Output): Offset Voltage ($VCO_{IN}-V_{DEM}$)	R_S > 10 kΩ		5,10	–	1.5	2.2	V
			15	–	1.5	–	
Linearity	R_S>50kΩ, VCO_{IN} = 2.5±0.3 V		5	–	0.1	–	%
	= 5±2.5 V		10	–	0.6	–	
	= 7.5±5 V		15	–	0.8	–	
Zener Diode Voltage (V_Z): CD4046AD,AF,AK	I_Z = 50 μA			4.7	5.2	5.7	V
CD4046AE,AY				4.5	5.2	6.1	
Zener Dynamic Resistance, R_Z	I_Z = 1 mA			–	100	–	Ω

● Positive coefficient.

DESIGN INFORMATION (Cont'd):

Characteristics	Phase Comparator Used	Design Information	
Locks On Harmonic of Center Frequency	1	Yes	
	2	No	
Signal Input Noise Rejection	1	High	
	2	Low	
VCO Component Selection	1	VCO WITHOUT OFFSET $R_2 = \infty$ – Given: f_o – Use f_o with Fig.5a to determine R1 and C1	VCO WITH OFFSET – Given: f_o and f_L – Calculate f_{min} from the equation $f_{min} = f_o - f_L$ – Use f_{min} with Fig.5b to determine R2 and C1 – Calculate $\frac{f_{max}}{f_{min}}$ from the equation $\frac{f_{max}}{f_{min}} = \frac{f_o + f_L}{f_o - f_L}$ – Use $\frac{f_{max}}{f_{min}}$ with Fig.5c to determine ratio R2/R1 to obtain R1
	2	– Given: f_{max} – Calculate f_o from the equation $f_o = \frac{f_{max}}{2}$ –Use f_o with Fig.5a to determine R1 and C1	– Given: f_{min} & f_{max} – Use f_{min} with Fig.5b to determine R2 and C1 – Calculate $\frac{f_{max}}{f_{min}}$ – Use $\frac{f_{max}}{f_{min}}$ with Fig.5c to determine ratio R2/R1 to obtain R1

For further information, see

(1) F. Gardner, "Phase-Lock Techniques" John Wiley and Sons, New York, 1966

(2) G. S. Moschytz, "Miniaturized RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.

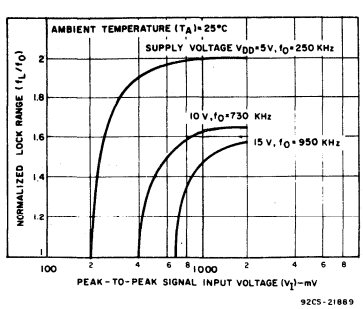
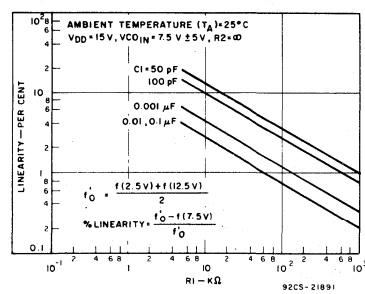


Fig.7 – Typical lock range vs signal input amplitude.



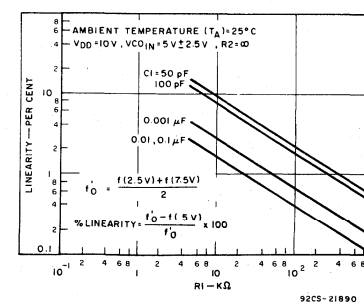


Fig.8(a) and (b) – Typical VCO linearity vs R1 and C1.

COS/MOS Low-Power Monostable/Astable Multivibrator

The RCA-CD4047A consists of a gatable astable multivibrator with logic techniques incorporated to permit positive or negative edge-triggered monostable multivibrator action with retriggering and external counting options.

Inputs include +TRIGGER, −TRIGGER, ASTABLE, $\overline{\text{ASTABLE}}$, RETRIGGER, and EXTERNAL RESET. Buffered outputs are Q, $\overline{Q}$, and OSCILLATOR. In all modes of operation an external capacitor must be connected between C-Timing and RC-Common terminals, and an external resistor must be connected between the R-Timing and RC-Common terminals.

Astable operation is enabled by a high level on the ASTABLE input. The period of the square wave at the Q and $\overline{Q}$ Outputs in this mode of operation is a function of the external components employed. "True" input pulses on the ASTABLE input or "Complement" pulses on the $\overline{\text{ASTABLE}}$ input allow the circuit to be used as a gatable multivibrator. The OSCILLATOR output period will be half of the Q terminal output in the astable mode. However, a 50% duty cycle is not guaranteed at this output.

In the monostable mode, positive-edge triggering is accomplished by application of a leading-edge pulse to the +TRIGGER input and a low level to the −TRIGGER input. For negative-edge triggering, a trailing-edge pulse is applied to the −TRIGGER and a high level is applied to the +TRIGGER. Input pulses may be of any duration relative to the output pulse. The multivibrator can be retriggered (on the leading edge only) by applying a common pulse to both the RETRIGGER and +TRIGGER inputs. In this mode the output pulse remains high as long as the input pulse period is shorter than the period determined by the RC components.

An external countdown option can be implemented by coupling "Q" to an external "N" counter and resetting the counter with the trigger pulse. The counter output pulse is fed back to the $\overline{\text{ASTABLE}}$ input and has a duration equal to N times the period of the multivibrator.

A high level on the EXTERNAL RESET input assures no output pulse during an "ON" power condition. This input can also be activated to terminate the output pulse at any time. In the monostable mode, a high-level or power-on reset pulse, must be applied to the EXTERNAL RESET whenever V_{DD} is applied.

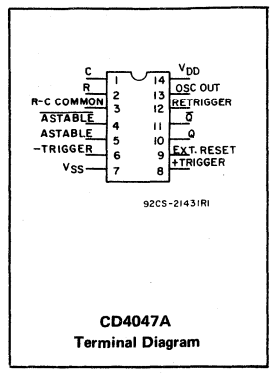
These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- **Low power consumption: special COS/MOS oscillator configuration**
- **Monostable (one-shot) or astable (free-running) operation**
- **True and complemented buffered outputs**
- **Only one external R and C required**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Monostable Multivibrator Features:

- **Positive- or negative-edge trigger**
- **Output pulse width independent of trigger pulse duration**
- **Retriggerable option for pulse width expansion**
- **Long pulse widths possible using small RC components by means of external counter provision**
- **Fast recovery time essentially independent of pulse width**
- **Pulse-width accuracy maintained at duty cycles approaching 100%**



CD4047A
Terminal Diagram

Astable Multivibrator Features:

- **Free-running or gatable operating modes**
- **50% duty cycle**
- **Oscillator output available**
- **Good astable frequency stability:**
  Frequency deviation:
  =±2% + 0.03%/°C @ 100 kHz
  =±0.5% + 0.015%/°C @ 10 kHz
  (circuits "trimmed" to frequency V_{DD} = 10 V ± 10%)

Applications :

Digital equipment where low-power dissipation and/or high noise immunity are primary design requirements:

- **Envelope detection**
- **Frequency multiplication**
- **Frequency division**
- **Frequency discriminators**
- **Timing circuits**
- **Time-delay applications**

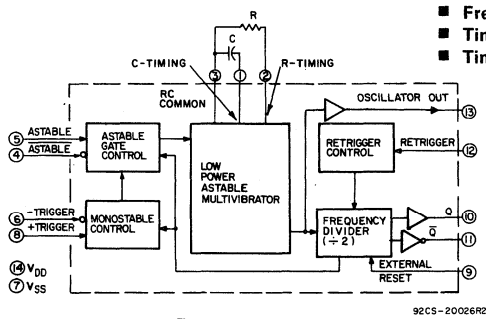


Fig. 1 – CD4047A logic block diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C

PACKAGE TYPE E . . . . . −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal): . . . . . −0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D)

FOR T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max . . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A= 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD}	LIMITS				UNITS
		D,F,K,H Packages		*E Package*		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A=Full Package- Temperature Range)		3	12	3	12	V
Input Pulse Width, t_W (Any Input)	5 10	1000 400	— —	1300 600	— —	ns
Trigger, Retrigger Rise or Fall Time, t_r , t_f	5 10	— —	15 5	— —	15 5	μs

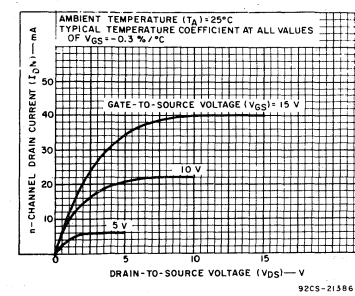


Fig. 2 — Typical output n-channel drain characteristics for Q and $\overline{Q}$ buffers.

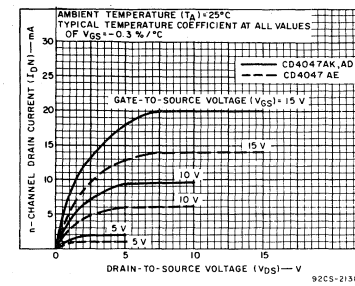


Fig. 3 — Minimum output n-channel drain characteristics for Q and $\overline{Q}$ buffers.

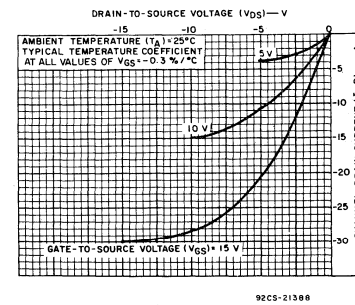


Fig. 4. — Typical output p-channel drain characteristics for Q and $\overline{Q}$ buffers.

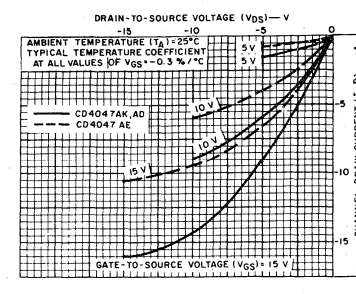


Fig. 5 — Minimum output p-channel drain characteristics for Q and $\overline{Q}$ buffers.

STATIC ELECTRICAL CHARACTERISTICS

Characteristics	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				*E Package*				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current I_L Max.	—	—	5	5	0.03	5	300	50	0.1	50	700	μA
	—	—	10	10	0.05	10	600	100	0.2	100	1400	
	—	—	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	—	5	5	0 Typ.; 0.05 Max.								V
	—	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	—	0	5	4.95 Min.; 5 Typ.								
	—	0	10	9.95 Min., 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	—	5	1.5 Min.; 2.25 Typ.								V
	9	—	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	—	5	1.5 Min.; 2.25 Typ.								
	1	—	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5		5	1 Min.								V
	9		10	1 Min.								
Inputs High, V_{NMH}	0.5		5	1 Min.								
	1		10	1 Min.								
Output Drive Current: (Q,$\overline{Q}$ Outputs) n-channel (Sink), I_DN Min.	0.5	—	5	0.5	0.8	0.4	0.28	0.34	0.8	0.28	0.23	mA
	0.5	—	10	1.25	2	1	0.7	0.85	2	0.7	0.6	
p-Channel (Source): I_DP Min.	4.5	—	5	-0.5	-0.8	-0.4	-0.28	-0.34	-0.8	-0.28	-0.23	
	9.5	—	10	-1.25	-2	-1	-0.7	-0.85	-2	-0.7	-0.6	
Input Leakage Current, I_{IL},I_{IH}	Any Input	—	15	$\pm 10^{-5}$ Typ., ±1 Max.								μA

CD4047A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTICS	TEST CONDITIONS	LIMITS							UNITS
			D,F,K,H Packages			*E Package*			
		V_{DD} (Volts)	Min.	TYP.	MAX.	MIN.	TYP.	MAX.	
Propagation Delay Time: t_{PHL}, t_{PLH} Astable, $\overline{\text{Astable}}$ to Osc. Out		5	–	200	400	–	200	550	ns
		10	–	100	200	–	100	275	
Astable, $\overline{\text{Astable}}$ to Q, $\overline{Q}$		5	–	550	900	–	550	1200	
		10	–	250	500	–	250	650	
+Trigger, –Trigger to Q, $\overline{Q}$		5	–	700	1200	–	700	1600	
		10	–	300	600	–	300	800	
+Trigger, Retrigger to Q, $\overline{Q}$		5	–	300	600	–	300	800	
		10	–	175	300	–	175	400	
External Reset to Q, $\overline{Q}$		5	–	300	600	–	300	800	
		10	–	125	250	–	125	350	
Transition Time: t_{THL}, t_{TLH} Q, $\overline{Q}$		5	–	75	125	–	75	150	ns
		10	–	45	75	–	45	100	
Osc. Out		5	–	75	150	–	75	180	
		10	–	45	100	–	45	130	
Minimum Input Pulse Width (any input), t_W*		5	–	500	1000	–	500	1300	ns
		10	–	200	400	–	200	600	
+Trigger, Retrigger Rise & Fall Time, t_r, t_f		5	–	–	15	–	–	15	μs
		10	–	–	5	–	–	5	
Average Input Capacitance, C_I	Any Input	–	–	5	–	–	5	–	pF

* Input pulse widths below the minimum specified may cause malfunction of the unit. See Application Note ICAN - 6230

CD4047A FUNCTIONAL TERMINAL CONNECTIONS
NOTE: IN ALL CASES EXTERNAL RESISTOR BETWEEN TERMINALS 2 AND 3▲
EXTERNAL CAPACITOR BETWEEN TERMINALS 1 AND 3▲

FUNCTION	TERMINAL CONNECTIONS			OUTPUT PULSE FROM	OUTPUT PERIOD OR PULSE WIDTH
	TO V_{DD}	TO V_{SS}	INPUT PULSE TO		
Astable Multivibrator:					
Free Running	4,5,6,14	7,8,9,12	–	10,11,13	t_A(10,11)=4.40 RC
True Gating	4,6,14	7,8,9,12	5	10,11,13	t_A(13)=2.20 RC
Complement Gating	6,14	5,7,8,9,12	4	10,11,13	
Monostable Multivibrator:					
Positive-Edge Trigger	4,14	5,6,7,9,12	8	10,11	t_M(10,11)=2.48 RC
Negative-Edge Trigger	4,8,14	5,7,9,12	6	10,11	
Retriggerable	4,14	5,6,7,9	8,12	10,11	
External Countdown*	14	5,6,7,8,9,12	–	10,11	

* Input Pulse to Reset of External Counting Chip External Counting Chip Output To Terminal 4 ▲ See Text.

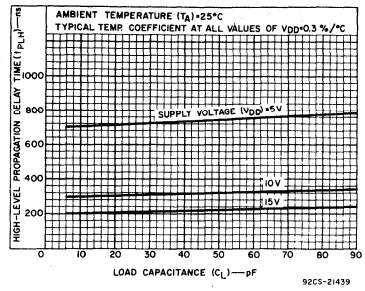


Fig. 6 – Typical low-to-high level propagation delay time vs load capacitance for Q and $\overline{Q}$ buffers.

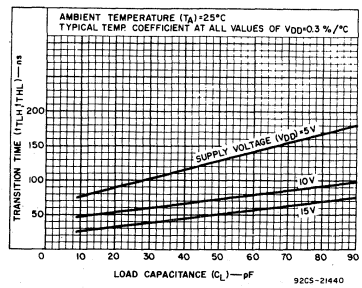


Fig. 7 – Typical transition time vs load capacitance for Q and $\overline{Q}$ buffers.

I. Astable Mode Design Information

A. Unit-to-Unit Transfer-Voltage Variations.

The following analysis presents worst-case variations from unit to unit as a function of transfer-voltage (V_{TR}) shift (33%–67% V_{DD}) for free-running (astable) operation.

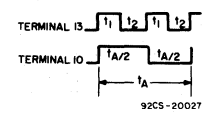


Fig. 8 – Astable mode waveforms.

$$t_1 = -RC \ln \frac{V_{TR}}{V_{DD} + V_{TR}}$$

$$t_2 = -RC \ln \frac{V_{DD} - V_{TR}}{2V_{DD} - V_{TR}}$$

$$t_A = 2(t_1 + t_2)$$

$$= -2\,RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_{TR})(2V_{DD} - V_{TR})}$$

Typ: $V_{TR} = 0.5\,V_{DD}$ $t_A = 4.40\,RC$
Min: $V_{TR} = 0.33\,V_{DD}$ $t_A = 4.62\,RC$
Max: $V_{TR} = 0.67\,V_{DD}$ $t_A = 4.62\,RC$

thus if $\boxed{t_A = 4.40\,RC}$ is used, the maximum variation will be (+5.0%,–0.0%).

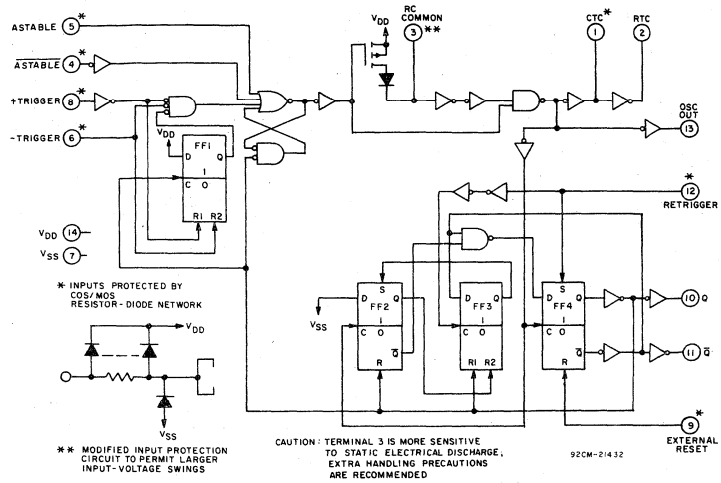


Fig. 9 – CD4047A logic diagram.

B. Variations Due to V_{DD} and Temperature Changes

In addition to variations from unit to unit, the astable period may vary as a function of frequency with respect to V_{DD} and temperature. Typical variations are presented in graphical form in Figs. 10 to 20 with 10 V as reference for voltage variation curves and 25°C as reference for temperature variation curves.

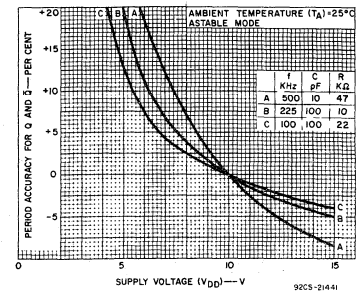


Fig. 10 – Typical Q-and-$\bar{Q}$-period accuracy vs supply voltage (high frequency).

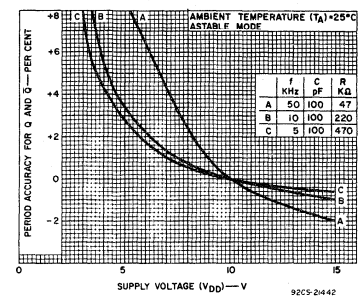


Fig. 11 – Typical Q-and-$\bar{Q}$-period accuracy vs supply voltage (medium frequency)

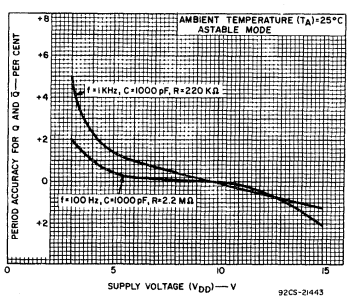


Fig. 12 – Typical Q-and-$\bar{Q}$-period accuracy vs supply voltage (low frequency).

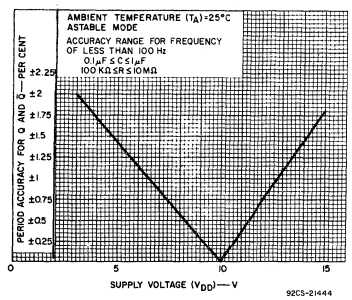


Fig. 13 – Typical Q-and-$\bar{Q}$- period accuracy vs supply voltage (very low frequency).

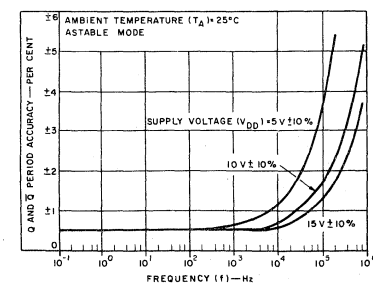


Fig. 14 – Typical Q-and $\bar{Q}$-period accuracy vs frequency for V_{DD} variation of ±10% from value indicated.

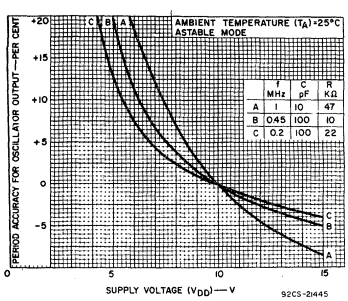


Fig. 15 – Typical oscillator-output-period accuracy vs supply voltage (high frequency).

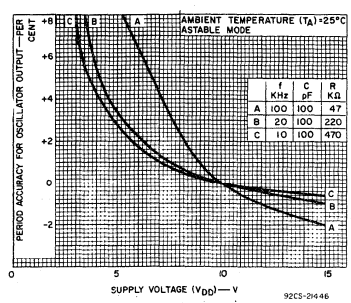


Fig. 16 – Typical oscillator-output-period accuracy vs supply voltage (medium frequency).

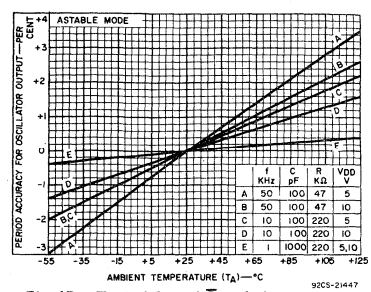


Fig. 17 – Typical Q- and $\bar{Q}$-period accuracy vs temperature (medium frequency).

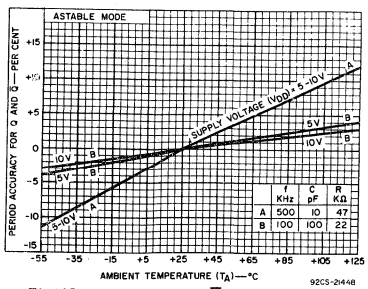


Fig. 18 – Typical Q- and Q̄-period accuracy vs temperature (high frequency).

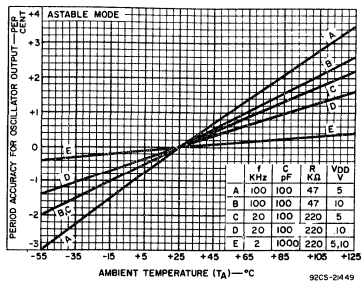


Fig. 19 – Typical oscillator-period accuracy vs temperature (medium frequency).

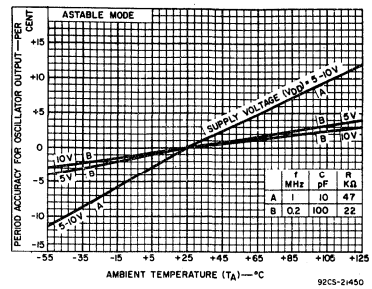


Fig. 20 – Typical oscillator-period accuracy vs temperature (high frequency).

II. Monostable Mode Design Information

The following analysis presents worst-case variations from unit to unit as a function of transfer-voltage (V_{TR}) shift (33% – 67% V_{DD}) for one-shot (monostable) operation.

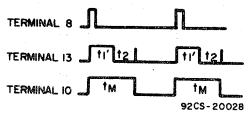


Fig. 21 – Monostable waveforms.

$$t_1' = -RC \ln \frac{V_{TR}}{2V_{DD}}$$

$$t_M = (t_1' + t_2)$$

$$t_M = -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(2V_{DD} - V_{TR})(V_{DD})}$$

where t_M = Monostable mode pulse width. Values for t_M are as follows:

Typ: $V_{TR} = 0.5\ V_{DD}$ $t_M = 2.48\ RC$
Min: $V_{TR} = 0.33\ V_{DD}$ $t_M = 2.71\ RC$
Max. $V_{TR} = 0.67\ V_{DD}$ $t_M = 2.48\ RC$

Thus if $\boxed{t_M = 2.48\ RC}$ is used, the maximum variation will be (+9.3%, –0.0%).

Note:

In the astable mode, the first positive half cycle has a duration of T_M; succeeding durations are $t_A/2$.

In addition to variations from unit to unit, the monostable pulse width may vary as a function of frequency with respect to V_{DD} and temperature. These variations are presented in graphical form in Fig. 22 to 27 with 10 V as reference for voltage-variation curves and 25°C as reference for temperature-variation curves.

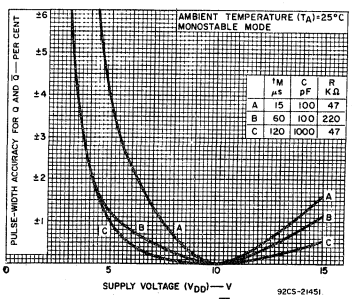


Fig. 22 – Typical Q- and Q̄-pulse-width accuracy vs supply voltage (t_M = 15, 60, 120 µs).

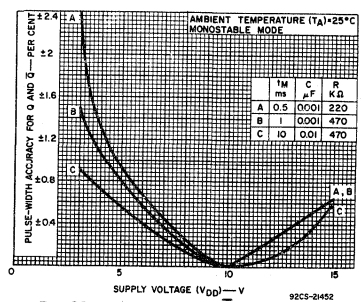


Fig. 23 – Typical Q- and Q̄-pulse-width accuracy vs supply voltage (t_M = 0.5, 1, 10 ms).

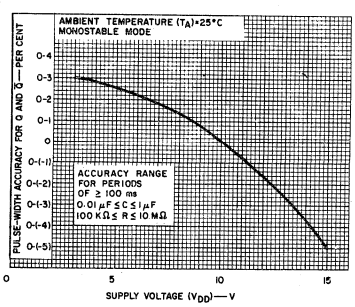


Fig. 24 – Typical Q- and Q̄-pulse-width accuracy vs supply voltage ($t_M \geq 100$ ms).

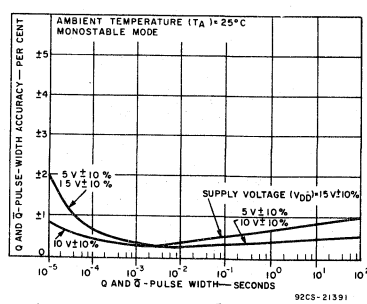


Fig. 25 – Typical Q- and Q̄ pulse-width accuracy vs Q and Q̄ pulse width for a variation of ± 10% from value indicated.

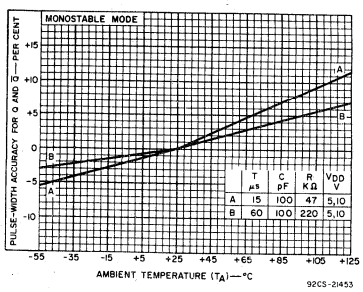


Fig. 26 – Typical Q and Q̄ pulse-width accuracy vs temperature (high frequency).

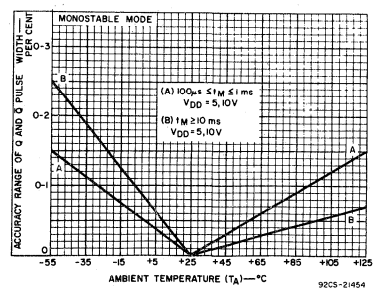


Fig. 27 – Typical Q and Q̄ pulse-width accuracy range vs temperature.

III. Retrigger Mode Operation

The CD4047A can be used in the retrigger mode to extend the output-pulse duration, or to compare the frequency of an input signal with that of the internal oscillator. In the retrigger mode the input pulse is applied to terminals 8 and 12, and the output is taken from terminal 10 or 11. As shown in Fig. 28, normal monostable action is obtained when one retrigger pulse is applied. Extended pulse duration is obtained when more than one pulse is applied. For two input pulses, $t_{RE}=t_1' + t_1 + 2t_2$. For more than two pulses, t_{RE} (Q OUTPUT), terminates at some variable time, t_D, after the termination of the last retrigger pulse, t_D is variable because t_{RE} (Q OUTPUT) terminates after the second positive edge of the oscillator output appears at flip-flop 4 (see Fig. 8).

IV. External Counter Option

Time t_M can be extended by any amount with the use of external counting circuitry. Advantages include digitally controlled pulse duration, small timing capacitors for long time periods, and extremely fast recovery time. A typical implementation is shown in Fig. 29. The pulse duration at the output is

$$t_{ext} = (N-1)(t_A) + (t_M + t_A/2)$$

where t_{ext}= pulse duration of the circuitry, and N is the number of counts used.

V. Timing-Component Limitations

The capacitor used in the circuit should be non-polarized and have low leakage(i.e. the parallel resistance of the capacitor should be an order of magnitude greater than the external resistor used). There is no upper or lower limit for either R or C value to maintain oscillation.

However, in consideration of accuracy, C must be much larger than the inherent stray capacitance in the system (unless this capacitance can be measured and taken into account). R must be much larger than the COS/MOS "ON" resistance in series with it, which typically is hundreds of ohms. In addition, with very large values of R, some short-term instability with respect to time may be noted.

The recommended values for these components to maintain agreement with previously calculated formulas without trimming should be:

$C \geqslant 100$ pF, up to any practical value, for astable modes;

$C \geqslant 1000$ pF, up to any practical value for monostable modes.

$10\ k\Omega \leqslant R \leqslant 1\ M\Omega$

VI. Power Consumption

In the standby mode (Monostable or Astable), power dissipation will be a function of leakage current in the circuit, as shown in the static electrical characteristics. For dynamic operation, the power needed to charge the external timing capacitor C is given by the following formulae:

Astable Mode: $P = 2CV^2f$. (Output at terminal No. 13)
$P = 4CV^2f$. (Output at terminal Nos. 10 and 11)

Monostable Mode:

$$P = \frac{(2.9CV^2)\ (\text{Duty Cycle})}{T}$$

(Output at terminal Nos. 10 and 11)

The circuit is designed so that most of the total power is consumed in the external components. In practice, the lower the values of frequency and voltage used, the closer the actual power dissipation will be to the calculated value.

Because the power dissipation does not depend on R, a design for minimum power dissipation would be a small value of C. The value of R would depend on the desired period (within the limitations discussed above). See Figs. 30–32 for typical power consumption in astable mode.

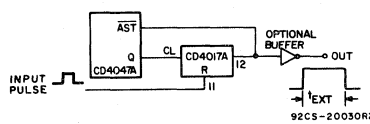


Fig. 28 – Implementation of external counter option.

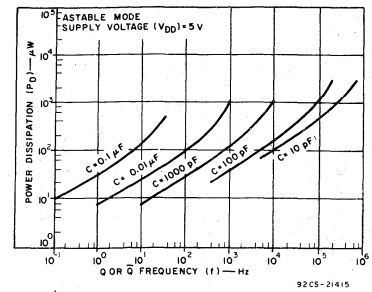


Fig. 30 – Power dissipation vs output frequency (V_{DD} = 5 V).

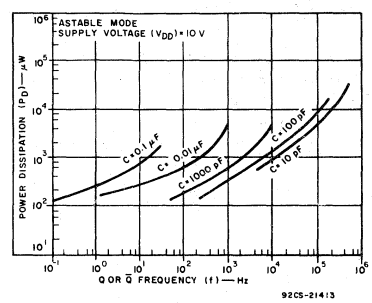


Fig. 31 – Power dissipation vs output frequency (V_{DD} = 10 V).

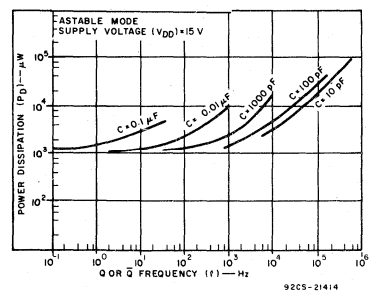


Fig. 32 – Power dissipation vs output frequency (V_{DD} = 15 V).

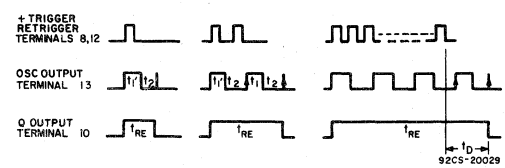


Fig. 29 – Retrigger-mode waveforms.

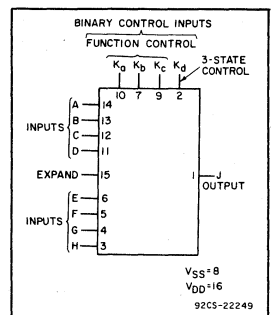
COS/MOS Multi-Function Expandable 8-Input Gate

The RCA-CD4048A is an 8-input gate having four control inputs. Three binary control inputs – Ka, Kb, and Kc – provide the implementation of eight different logic functions. These functions are OR, NOR, AND, NAND, OR/AND, OR/NAND, AND/OR, and AND/NOR.

A fourth control input –Kd – provides the user with 3-state outputs. When control input Kd is high the output is either a logic 1 or a logic 0 depending on the input states. When control input Kd is low, the output is an open circuit. This feature enables the user to connect this device to a common bus line.

In addition to the eight input lines, an EXPAND input is provided that permits the user to increase the number of inputs to one CD4048A, (see Fig. 6). For example, two CD4048A's can be cascaded to provide a 16-input multifunction gate. When the EXPAND input is not used, it should be connected to V_{SS}.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).



CD4048A Functional Diagram

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
PACKAGE TYPE E . . . . . –40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): . . . . . –0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A = –40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = –55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max . . . . . +265°C

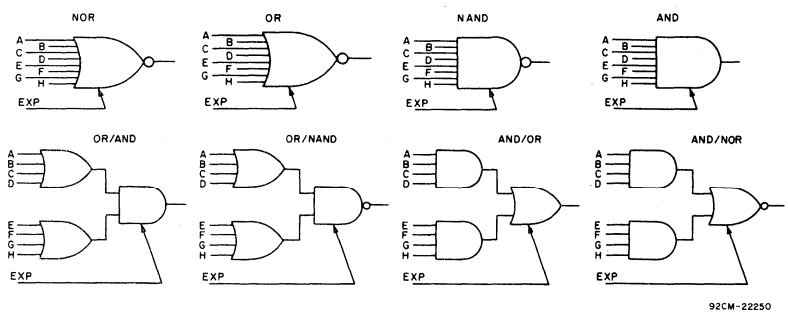


Fig. 1 – Basic logic configurations.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D,F,K,H Packages		E Package		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V

Features:

- **Medium-power TTL drive capability**
- **Three-state output**
- **High current source and sink capability 9 mA (typ.) @ V_{DS} = 0.5 V, V_{DD} = 10 V**
- **Many logic functions available in one package**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Selection of up to 8 logic functions**
- **Digital control of logic**
- **General-purpose gating logic**
  - **Decoding**
  - **Encoding**

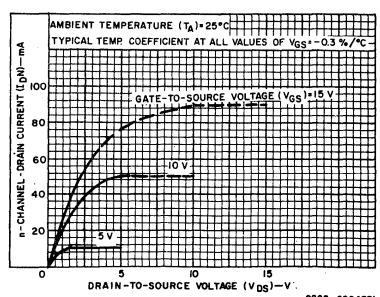


Fig. 2– Typical output n-channel drain characteristics.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				E Package				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current I_L Max.	–	–	5	1	0.005	1	60	10	0.01	10	140	μA
	–	–	10	2	0.01	2	120	20	0.02	20	280	
	–	–	15	25	0.5	25	1000	250	2.5	250	2500	
Output Voltage: Low Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: n-Channel (Sink) I_DN Min.	0.4	–	4.5	2	3.2	1.6	1.1	1.9	3.2	1.6	1.3	mA
	0.5	–	10	5.6	9	4.5	3.1	5.4	9	4.5	3.7	
p-channel (Source), I_DP Min.	4.6	–	5	−2	−3.2	−1.6	−1.1	−1.9	−3.2	−1.6	−1.3	
	9.5	–	10	−5.6	−9	−4.5	−3.1	−3.8	−9	−3.15	−2.6	
Input Leakage Current, I_{IL},I_{IH}	Any Input			± 10^{-5} Typ., ± 1 Max.								μA
	–	–	15									
3-State Output Leakage Current I_{OL},I_{OH}	Forced (Output Disabled)			±10^{-4} Typ., ±2 Max.								μA
	–	–	15									

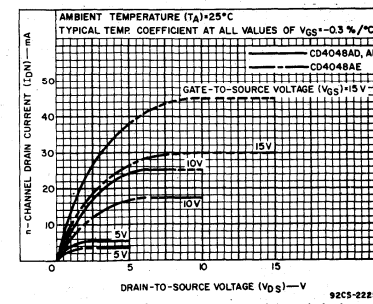


Fig. 3— Minimum output n-channel drain characteristics .

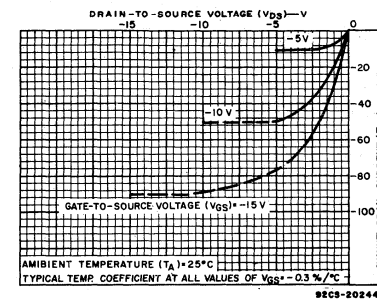


Fig. 4— Typical output p-channel drain characteristics.

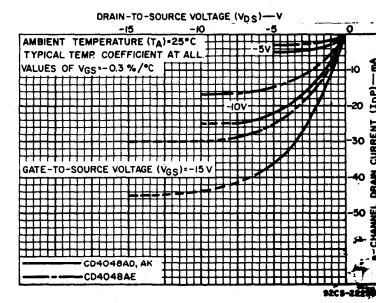


Fig. 5— Minimum output p-channel drain characteristics.

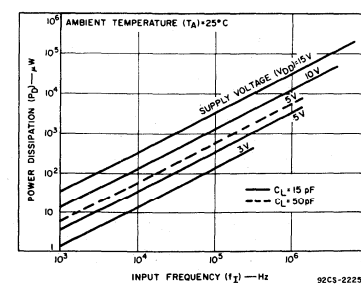


Fig. 6— Typical power dissipation as a function of input frequency.

DYNAMIC ELECTRICAL CHARACTERISTCS at T_A = 25°C and C_L = 15 pF and 50 pF,
Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C R_L = 200 kΩ

C_L = 15 pF

CHARACTERISTIC	TEST CONDITIONS		LIMITS				UNITS
			D,F,K,H Packages		*E Package*		
		V_{DD} (Volts)	TYP.	MAX.*	TYP.	MAX.*	
Propagation Delay Time t_{PHL}		5	750	1300	750	1600	ns
		10	225	400	225	500	
Transition Time: High-to-Low Level t_{THL}		5	90	140	90	170	ns
		10	30	50	30	65	
Low-to-High Level t_{TLH}		5	130	250	130	300	ns
		10	40	60	40	75	
Input Capacitance C_I	Any Input		5	—	5	—	pF
C_L = 50 pF							
Propagation Delay Time t_{PLH},t_{PHL}		5	775	1350	775	1650	ns
		10	240	430	240	530	
Transition Time: High-to-Low Level t_{THL}		5	105	170	105	200	ns
		10	40	70	40	85	
Low-to-High Level t_{TLH}		5	145	280	145	330	ns
		10	50	80	50	95	
Input Capacitance C_I	Any Input		5	—	5	—	pF

* Max. Limits represent worst-case limits for worst-case modes of operation shown in Figs. 15, 16, and 17.

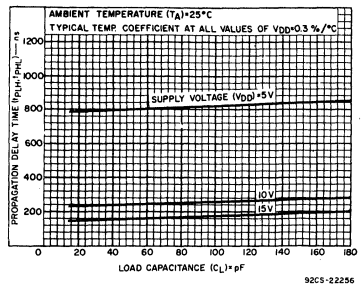


Fig. 7— Typical propagation delay time as a function of load capacitance.

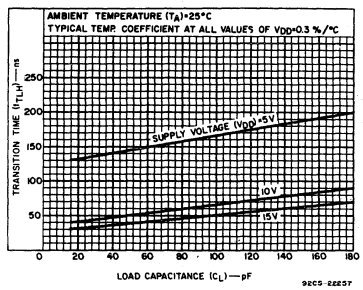


Fig. 8— Typical low-to-high level transition time as a function of load capacitance.

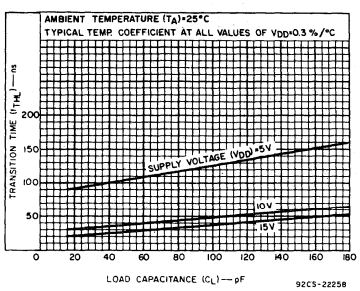


Fig. 9— Typical high-to-low level transition time as a function of load capacitance.

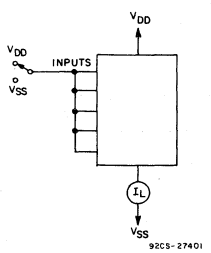


Fig. 10— Quiescent-device-current test circuit.

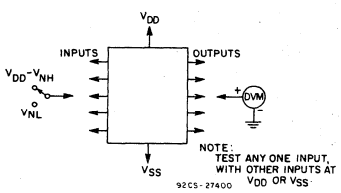


Fig. 11— Noise-immunity test circuit.

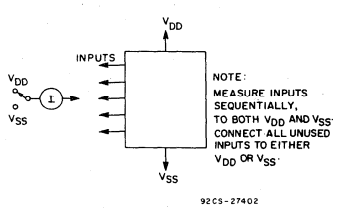
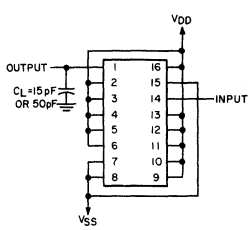


Fig. 12— Input-leakage-current test circuit.



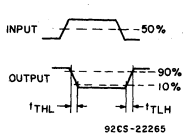


Fig. 13— t_{THL}, t_{TLH} — AND/NOR.

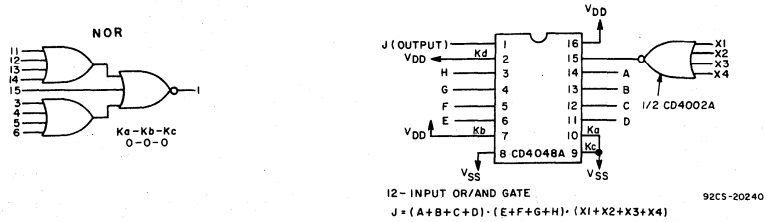


Fig. 14(a) - 12-input OR/AND gate.

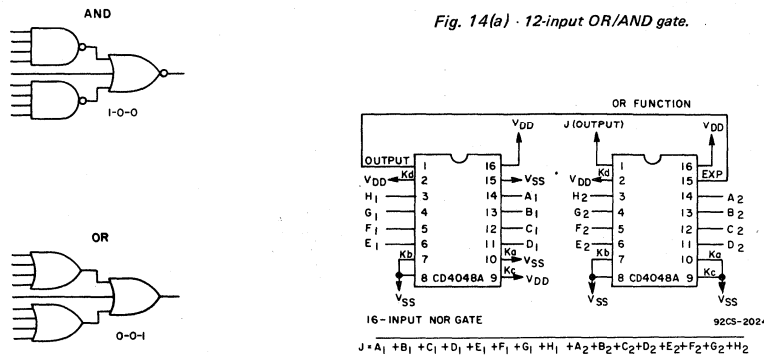


Fig. 14(b) 16-input NOR gate.

Applications of Expand Input

IMPLEMENTATION OF EXPAND INPUT FOR 9 OR MORE INPUTS

OUTPUT FUNCTION	FUNCTION NEEDED AT EXPAND INPUT	OUTPUT BOOLEAN EXPRESSION
NOR	OR	$J=\overline{(A+B+C+D+E+F+G+H)+(EXP)}$
OR	OR	$J=(A+B+C+D+E+F+G+H)+(EXP)$
AND	NAND	$J=(ABCDEFGH)\cdot(EXP)$
NAND	NAND	$J=\overline{(ABCDEFGH)\cdot(EXP)}$
OR/AND	NOR	$J=(A+B+C+D)\cdot(E+F+G+H)\cdot(EXP)$
OR/NAND	NOR	$J=\overline{(A+B+C+D)\cdot(E+F+G+H)\cdot(EXP)}$
AND/NOR	AND	$J=\overline{(ABCD)+(EFGH)+(EXP)}$
AND/OR	AND	$J=(ABCD)+(EFGH)+(EXP)$

Note: (EXP) designates the EXPAND function (i.e., $X_1+X_2+\ldots X_N$).

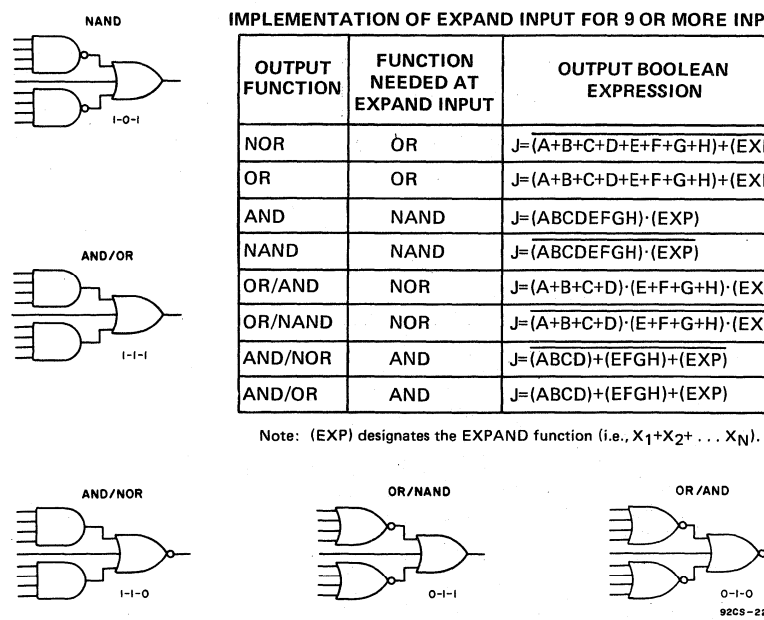


Fig. 14(c) Actual-circuit logic configurations.

Fig. 14— Expansion logic and truth table.

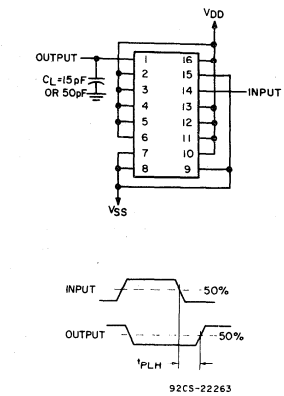


Fig. 15— t_{PLH} — NAND.

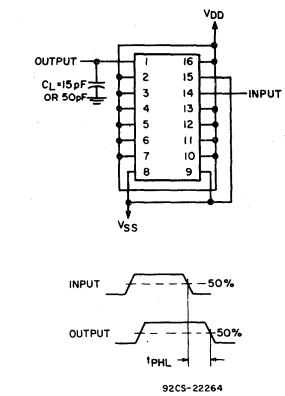
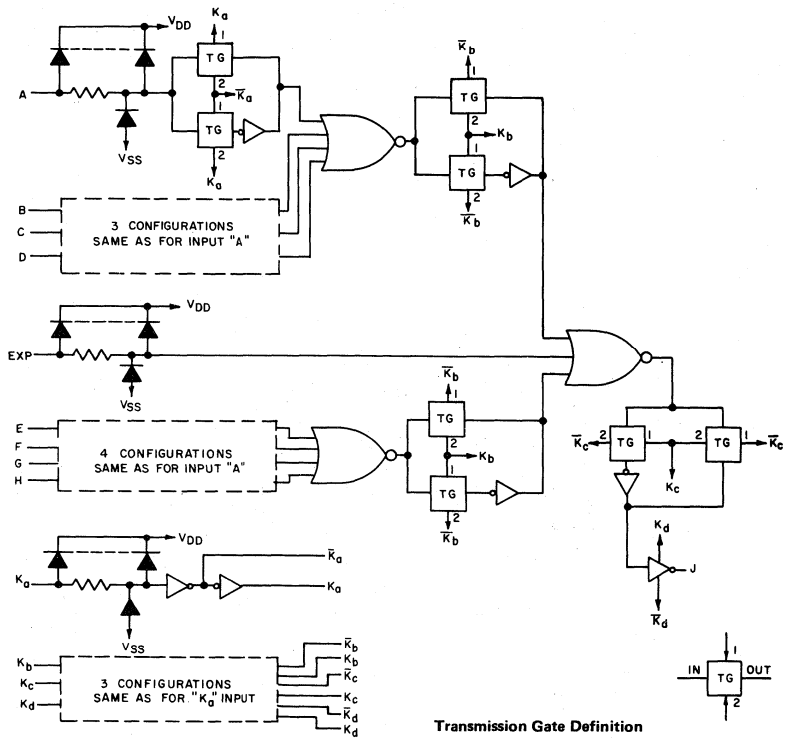


Fig. 16— t_{PHL} — AND.



Transmission Gate Definition

TG = Transmission Gate
Input to Output is:

a) A bidirectional low impedance when control input 1 is low and control 2 is high.

b) An open circuit when control input 1 is high and control input 2 is low.

92CM-22251R1

FUNCTION TRUTH TABLE

OUTPUT FUNCTION	BOOLEAN EXPRESSION	K_a	K_b	K_c	UNUSED INPUT*
NOR	$J=\overline{A+B+C+D+E+F+G+H}$	0	0	0	V_{SS}
OR	$J=A+B+C+D+E+F+G+H$	0	0	1	V_{SS}
OR/AND	$J=(A+B+C+D)\cdot(E+F+G+H)$	0	1	0	V_{SS}
OR/NAND	$J=\overline{(A+B+C+D)\cdot(E+F+G+H)}$	0	1	1	V_{SS}
AND	$J=ABCDEFGH$	1	0	0	V_{DD}
NAND	$J=\overline{ABCDEFGH}$	1	0	1	V_{DD}
AND/NOR	$J=\overline{ABCD+EFGH}$	1	1	0	V_{DD}
AND/OR	$J=ABCD+EFGH$	1	1	1	V_{DD}

K_d=1 Normal Inverter Action
K_d=0 High Impedance Output

EXPAND Input=0

*See Figs. 1 and 7.

Fig. 17– Logic diagram and truth table.

COS/MOS Hex Buffer/Converters

CD4049A—Inverting Type
CD4050A—Non-Inverting Type

The CD4049A and CD4050A are inverting and non-inverting hex buffers, respectively, and feature logic-level conversion using only one supply voltage (V_{CC}). The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage when these devices are used for logic-level conversions. These devices are intended for use as COS/MOS to DTL/TTL converters and can drive directly two DTL/TTL loads. (V_{CC}=5 V, $V_{OL} \geqslant$0.4 V, and $I_DN \geqslant$3.2 mA.)

The CD4049A and CD4050A are designated as replacements for CD4009A and CD4010A, respectively. Because the CD4049A and CD4050A require only one power supply, they are preferred over the CD4009A and CD4010A and should be used in place of the CD4009A and CD4010A in all inverter, current driver, or logic-level conversion applications. In these applications the CD4049A and CD4050A are pin compatible with the CD4009A and CD4010A respectively, and can be substituted for these devices in existing as well as in new designs. Terminal No. 16 is not connected internally on the CD4049A or CD4050A, therefore, connection to this terminal is of no consequence to circuit operation. For applications not requiring high sink-current or voltage conversion, the CD4069 Hex Inverter is recommended.

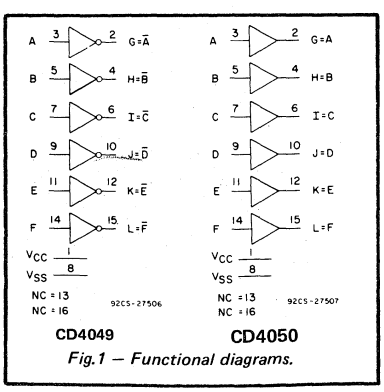
These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- **High sink current for driving 2 TTL loads**
- **High-to-low level logic conversion**
- **Quiescent current specified to 15 V**
- **Maximum input leakage of 1 μA at 15 V (full package-temperature range)**

Applications:

- **COS/MOS to DTL/TTL hex converter**
- **COS/MOS current "sink" or "source" driver**
- **COS/MOS high-to-low logic-level converter**



CD4049 **CD4050**

Fig.1 — Functional diagrams.

RECOMMENDED OPERATING CONDITIONS at T_A=25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (V_{CC}) (For T_A=Full Package-Temperature Range)	3	12	V
Input Voltage Range (V_I)	V_{CC}*	12	V

*The CD4049 and CD4050 have high-to-low-level voltage conversion capability but not low-to-high-level; therefore it is recommended that $V_I \geqslant V_{CC}$.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				*E Package*				
	V_O (V)	V_{IN} (V)	V_{CC} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	0.3	0.01	0.3	20	3	0.03	3	42	μA
	–	–	10	0.5	0.01	0.5	30	5	0.05	5	70	
	–	–	15	10	0.02	10	100	50	0.05	50	500	
Output Voltage: Low-Level, V_{OL}	–	0, 5	5	0 Typ.; 0.05 Max.								V
	–	0, 10	10	0 Typ.; 0.05 Max.								
High-Level, V_{OH}	–	0, 5	5	4.95 Min.; 5 Typ.								
	–	0, 10	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL} CD4050A	3.6	–	5	1.5 Min.; 2.25 Typ.								V
	7.2	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH} All Types	1.4	–	5	1.5 Min.; 2.25 Typ.								
	2.8	–	10	3 Min.; 4.5 Typ.								
Inputs Low, V_{NL} CD4049A	3.6	–	5	1 Min.; 1.5 Typ.								
	7.2	–	10	2 Min.; 3 Typ.								
Noise Margin: Inputs Low, V_{NML} Min. CD4050A	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH} Min. CD4050A	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink), I_DN Min.	0.4	–	4.5	3.3	5.2	2.6	1.8	3.1	5.2	2.6	2.1	mA
	0.4	–	5	3.75	6	3	2.1	3.6	6	3	2.5	
	0.5	–	10	10	16	8	5.6	9.6	16	8	6.6	
P-Channel (Source), I_DP Min.	4.5	–	5	−0.62	−1	−0.5	−0.35	−0.6	−1	−0.5	−0.4	
	2.5	–	5	−1.85	−2.5	−1.25	−0.9	−1.5	−2.5	−1.25	−1	
	9.5	–	10	−1.85	−2.5	−1.25	−0.9	−1.5	−2.5	−1.25	−1	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		15	$\pm 10^{-5}$ Typ., ±1 Max.								μA

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) ..... −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H ..... −55 to +125°C

PACKAGE TYPE E ..... −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{CC})

(Voltages referenced to V_{SS} Terminal) ..... −0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = −40 to +60°C (PACKAGE TYPE E) ..... 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) ..... Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) ..... 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

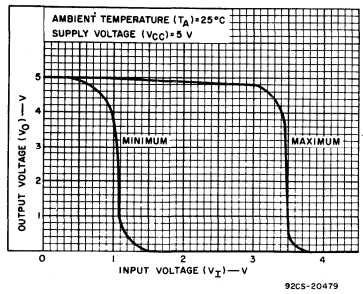


Fig. 2—Minimum and maximum voltage transfer characteristics for CD4049A.

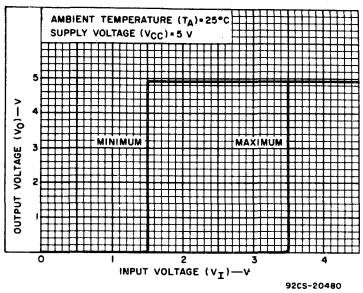


Fig. 3—Minimum and maximum voltage transfer characteristics for CD4050A.

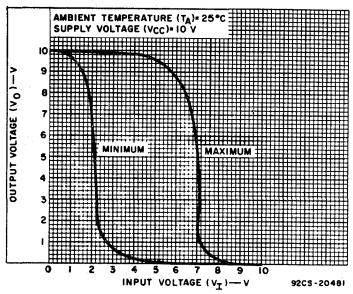


Fig. 4—Minimum and maximum voltage transfer characteristics for CD4049A.

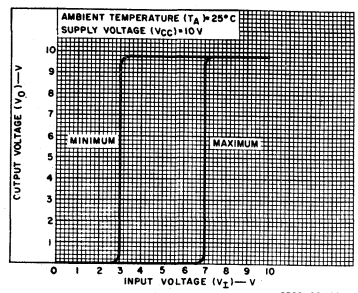


Fig. 5—Minimum and maximum voltage transfer characteristics for CD4050A.

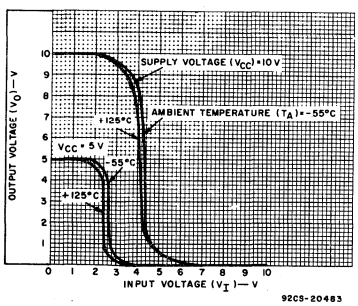


Fig. 6—Typical voltage transfer characteristics as a function of temperature for CD4049A.

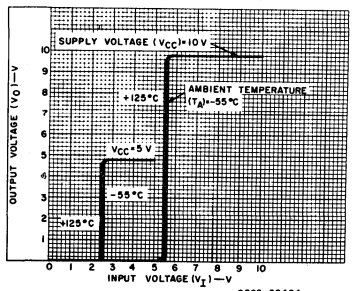


Fig. 7—Typical voltage transfer characteristics as a function of temperature for CD4050A.

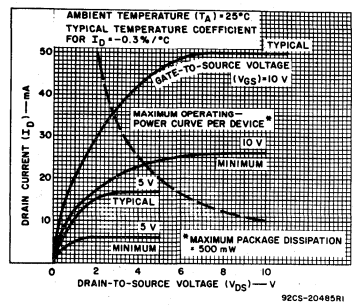


Fig. 8—Typical and minimum n-channel drain characteristics as a function of gate-to-source voltage (V_{GS}) for CD4049A, CD4050A.

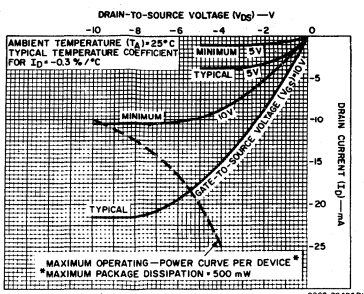


Fig. 9—Typical and minimum p-channel drain characteristics as a function of gate-to-source voltage (V_{GS}) for CD4049A, CD4050A.

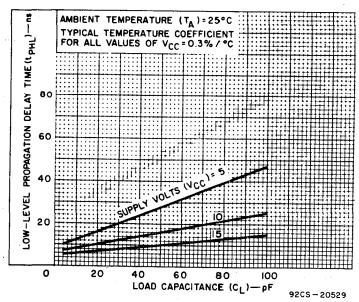


Fig. 10—Typical high-to-low level propagation delay time vs. C_L for CD4049A.

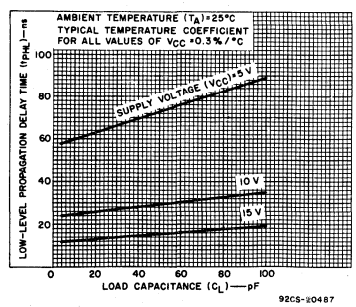


Fig. 11—Typical high-to-low level propagation delay time vs. C_L for CD4050A.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C; Input t_r,t_f=20 ns, C_L=15 pF, R_L=200 kΩ

CHARACTERISTIC	CONDITIONS		LIMITS ALL PKGS.		UNITS
	V_I	V_{CC}	Typ.	Max.	
Propagation Delay Time:					
Low-to-High, t_{PLH}					
CD4049A	5	5	50	80	ns
	10	10	25	55	
CD4050A	5	5	75	140	
	10	10	35	85	
High-to-Low, t_{PHL}					
CD4049A	5	5	15	55	ns
	10	10	10	30	
CD4050A	5	5	55	110	
	10	10	25	55	
Transition Time:					
Low-to-High, t_{TLH}	5	5	50	100	ns
	10	10	30	60	
High-to-Low, t_{THL}	5	5	20	45	
	10	10	16	40	
Input Capacitance, C_I					pF
CD4049A	–	–	15	–	
CD4050A	–	–	5	–	

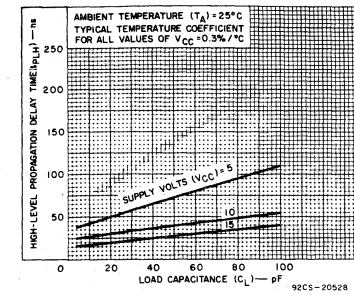


Fig. 12—Typical low-to-high level propagation delay time vs. C_L for CD4049A.

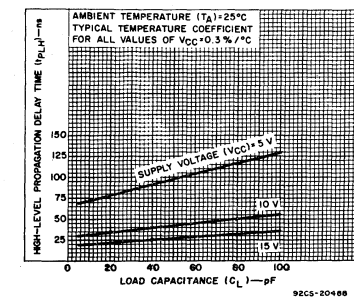


Fig. 13—Typical low-to-high level propagation delay time vs. C_L for CD4050A.

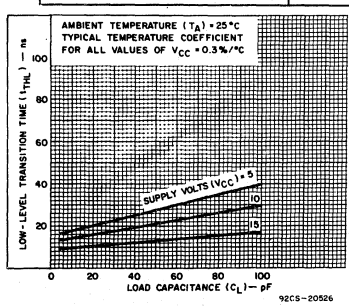


Fig. 14—Typical high-to-low level transition time vs. C_L for CD4049A, CD4050A.

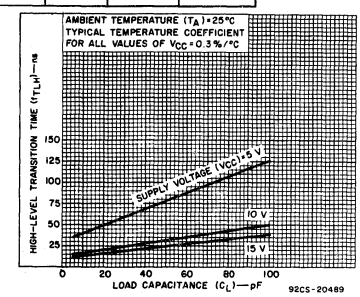


Fig. 15—Typical low-to-high level transition time vs. C_L for CD4049A, CD4050A.

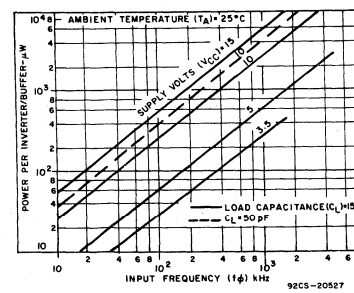


Fig. 16—Typical dissipation characteristics for CD4049A, CD4050A.

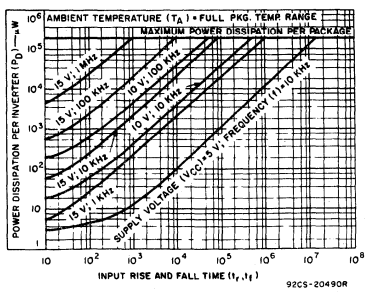


Fig. 17—Typical power dissipation vs. transition time per inverter CD4049A.

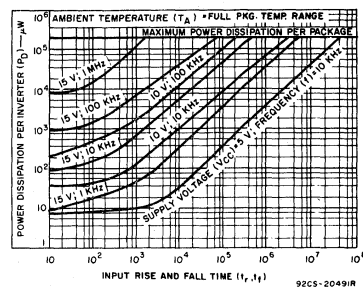


Fig. 18—Typical power dissipation vs. transition time per inverter CD4050A.

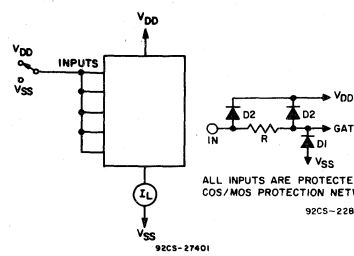


Fig. 21—Quiescent device current test circuit.

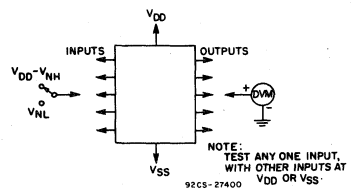


Fig. 19—Noise immunity test circuit.

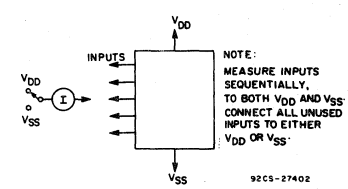


Fig. 20—Input leakage current test circuit.

CD4057A Types

COS/MOS LSI 4-Bit Arithmetic Logic Unit

The RCA-CD4057A is a low-power arithmetic logic unit (ALU) designed for use in LSI computers. An arithmetic system of virtually any size can be constructed by wiring together a number of CD4057A ALU's. The CD4057A provides 4-bit arithmetic operations, time sharing of data terminals, and full functional decoding for all control lines. The distributed control system of this device provides great flexibility in system designs by allowing hard-wired connection of N units in 4^N unique combinations. Four control lines provide 16 instructions which include Addition, Subtraction, Bidirectional and Cycle Shifts, Up-Down Counting, AND, OR, and Exclusive-OR logic operations.

Two mode control lines allow the CD4057A to function as any 4-bit section of a larger arithmetic unit by controlling the bidirectional serial transfer of data to adjacent arithmetic arrays. By means of three "Conditional Control" lines Overflow, All Zeros, and Negative State conditions may be detected and used to establish a conditional operation. Predetermined operation of the CD4057A on a conditional basis allows greater ALU flexibility. Although especially applicable as a parallel arithmetic unit, the CD4057A also finds use in virtually any application requiring one or more of its 16 basic instructions. The CD4057A is supplied in a hermetically sealed 28-lead dual-in-line ceramic package (CD4057AD), in a flat-pack (CD4057AK), and in chip form (CD4057AH).

Applications:

- **Parallel Arithmetic Units**
- **Process Controllers**
- **Remote Data Sets**
- **Graphic Display Terminals**

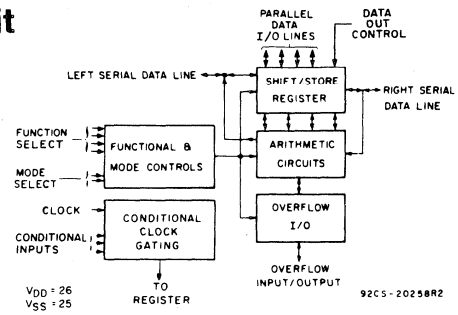


Fig. 1 – Block diagram – CD4057A.

Features:

- **LSI Complexity on a Single Chip**
- **16-Instruction Capability**
  - **-Add, Subtract, Count**
  - **-AND, OR, Exclusive-OR**
  - **-Right, Left, or Cyclic Shifts**
- **Bidirectional Data Busses**
- **Instruction Decoding on Chip**
- **Fully Static Operation**
- **Single-Phase Clocking**
- **Easily Expandable to 8, 12, 16,. . . . Bit Operation**
- **Low Quiescent Device Dissipation . . . . . 10 μW (typ.)**
- **Conditional-Operation Controls on Chip**
- **Add Time (Data In-To Sum Out) =375 ns (typ) at 10V**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, K, H . . . . . −55 to +125°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = −55 to +100°C (PACKAGE TYPES D, K) . . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, K) . . . . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	V
Setup Time, t_S DATA	5	40	–	ns
	10	20	–	
OP CODE	5	4590	–	
	10	1320	–	
Clock Pulse Width, t_W	5	1200	–	ns
	10	375	–	
Clock Input Frequency, f_{CL} Count Mode	5	0.13	–	MHz
	10	0.46	–	
Shift Mode	5	0.33	–	
	10	1.4	–	
Clock Rise or Fall Time, t_rCL, t_fCL	5	–	15	μs
	10	–	15	

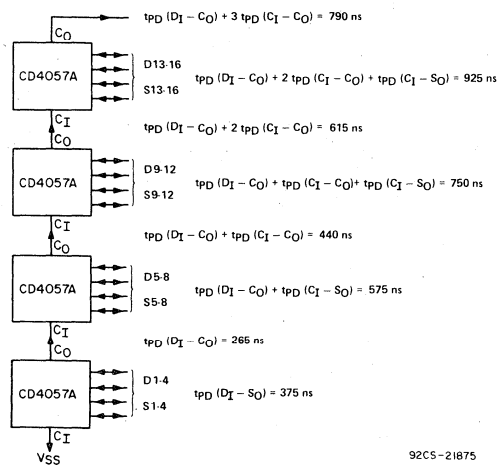


Fig. 2 – Typical speed characteristics of a 16-bit ALU at V_{DD} = 10 V.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			Limits at Indicated Temperatures (°C)							UNITS
				CD4057AD, CD4057AK, CD4057AH							
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55°C		25°C			125°C		
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
Quiescent Device Current I_L	–	–	5	–	5	–	0.5	5	–	150	μA
	–	–	10	–	10	–	1	10	–	300	
	–	–	15	–	50	–	1	50	–	2000	
Output Voltage; Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.							V
	–	10	10	0 Typ.; 0.05 Max.							
High Level, V_{OH}	–	0	5	4.95 Min.; 5 Typ.							V
	–	0	10	9.95 Min.; 10 Typ.							
Noise Immunity (All Inputs) V_{NL}, V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.							V
	1	–	10	3 Min.; 4.5 Typ.							
	4.2	–	5	1.5 Min.; 2.25 Typ.							
	9	–	10	3 Min.; 4.5 Typ.							
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.							V
	9	–	10	1 Min.							
Inputs High, V_{NMH}	0.5	–	5	1 Min.							
	1	–	10	1 Min.							
Output Drive Current: I_DN, I_DP Zero Indicator	0.5	–	5	0.11	–	0.09	0.16	–	0.06	–	mA
n-channel	0.5	–	10	0.12	–	0.10	0.16	–	0.07	–	
p-channel	3	–	5	0.04	–	0.03	0.06	–	0.02	–	
	7	–	10	0.08	–	0.07	0.13	–	0.05	–	
Negative Indicator	0.5	–	5	0.11	–	0.09	0.30	–	0.06	–	
n-channel	0.5	–	10	0.12	–	0.10	0.40	–	0.07	–	
p-channel	4.5	–	5	0.07	–	0.06	0.19	–	0.04	–	
	9.5	–	10	0.12	–	0.10	0.30	–	0.07	–	
Overflow Indicator	0.5	–	5	0.25	–	0.20	0.50	–	0.14	–	
n-channel	0.5	–	10	0.37	–	0.30	0.90	–	0.21	–	
p-channel	4.5	–	5	0.08	–	0.07	0.21	–	0.05	–	
	9.5	–	10	0.12	–	0.10	0.38	–	0.07	–	
All Other Outputs	0.5	–	5	0.11	–	0.09	0.10	–	0.06	–	
n-channel	0.5	–	10	0.06	–	0.05	0.12	–	0.03	–	
p-channel	4.5	–	5	0.02	–	0.02	0.05	–	0.01	–	
	9.5	–	10	0.06	–	0.05	0.08	–	0.03	–	
Input Leakage Current I_{IL}, I_{IH}	Any Input		15	$\pm 10^{-5}$ Typ., ± 1 Max.							μA

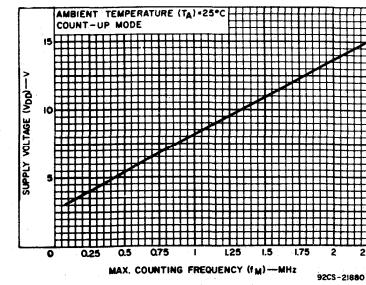


Fig. 3 — Maximum counting frequency vs. supply voltage for a typical CD4057A.

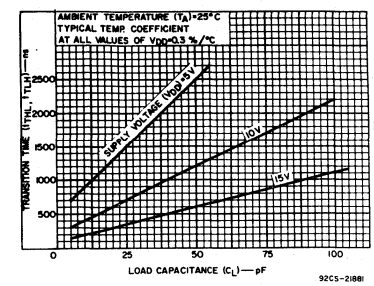


Fig. 4 — Transition time vs. load capacitance for data outputs (D1-D4).

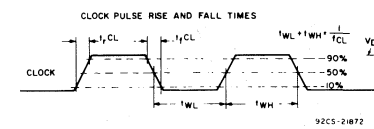


Fig. 5 — Clock pulse rise and fall times.

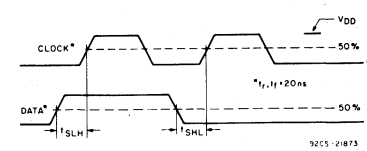


Fig. 6 — Data setup time.

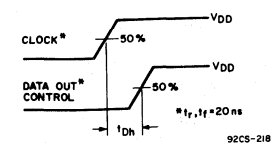


Fig. 7 — Data hold time.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$ and $C_L = 15$ pF, $R_L = 200$ kΩ, $t_r, t_f = 20$ ns

Typical Temperature Coefficient at all values of $V_{DD} = 0.3\%/°C$

CHARACTERISTICS	TEST CONDITIONS V_{DD}	LIMITS CD4057AD, CD4057AK Min.	Typ.	Max.	UNITS
Propagation Delay Time: t_{PLH}, t_{PHL} DATA IN-to-SUM OUT	5	–	1430	3900	ns
	10	–	375	720	
CARRY IN-to-SUM OUT	5	–	915	2550	
	10	–	310	840	
DATA IN-to-CARRY OUT	5	–	950	2580	
	10	–	265	720	
CARRY IN-to-CARRY OUT	5	–	485	1320	
	10	–	175	480	
ZI Input -to- ZI Output	5	–	1980	5400	
	10	–	750	2040	
	5	–	265	720	
	10	–	110	300	
Transition Time: t_{TLH}, t_{THL} ZI Output	5	–	3700	10350	ns
	10	–	1650	4500	
	5	–	420	1140	
	10	–	220	600	
Negative Indicator and Overflow Indicator	5	–	300	825	
	10	–	165	450	
All Other Outputs	5	–	1000	2775	
	10	–	475	1275	
Minimum Clock Pulse Width, t_W	5	–	400	1200	ns
	10	–	125	375	
Clock Rise and Fall Time, t_rCL, t_fCL	5	–	–	15	μs
	10	–	–	15	
Minimum Set Up Time : t_{SLH}, t_{SHL} DATA	5	–	20	40	ns
	10	–	10	20	
OP CODE	5	–	1675	4590	ns
	10	–	485	1320	
Minimum Data Hold Time, t_{HLH}, t_{HHL}	5	–	20	40	ns
	10	–	10	20	
Maximum Clock Frequency: f_{CL} Count Mode	5	0.13	0.36	–	MHz
	10	0.46	1.35	–	
Shift Mode	5	0.33	0.90	–	
	10	1.4	3.8	–	
Input Capacitance, C_I	ANY INPUT	–	5	–	pF

LOGIC DESCRIPTION

OPERATIONAL MODES

The CD4057A arithmetic logic unit operates in one of four possible modes. These modes control the transfer of information, either serial data or arithmetic operation carries, to and from the serial-data lines. Fig. 8 shows the manner in which the four modes control the data on the serial-data lines.

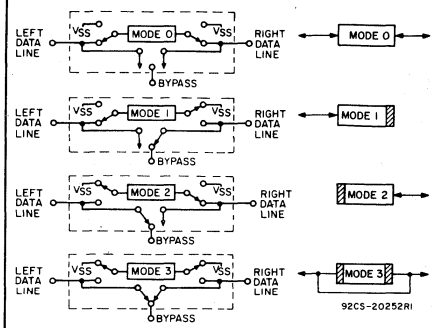


Fig. 8 – Schematic of "Mode" concept.

In MODE 0, data can enter or leave from either the left or the right serial-data line.

In MODE 1, data can enter or leave only on the left serial-data line.

In MODE 2, data can enter or leave only on the right serial-data line.

In MODE 3, serial data can neither enter nor leave the register,regardless of the nature of the operation. Furthermore, the register is by-passed electrically, i.e., there is an electrical bidirectional path between the right and left serial data terminals.

The two input lines labeled C1 and C2 in the terminal assignment diagram define one of four possible modes shown in Table I. Through the use of mode control, individual arithmetic arrays can be cascaded to form one large processor or many processors of various lengths.

TABLE I – MODE DEFINITION

C2	C1	MODE
0	0	0
0	1	1
1	0	2
1	1	3

Examples of how one " hard-wired " combination of three ALU's can form (a) a 12-bit parallel processor, (b) one 8-bit and one 4-bit parallel processor, or (c) three 4-bit parallel processors, merely by changes in the modes of each ALU are shown in Fig. 10.

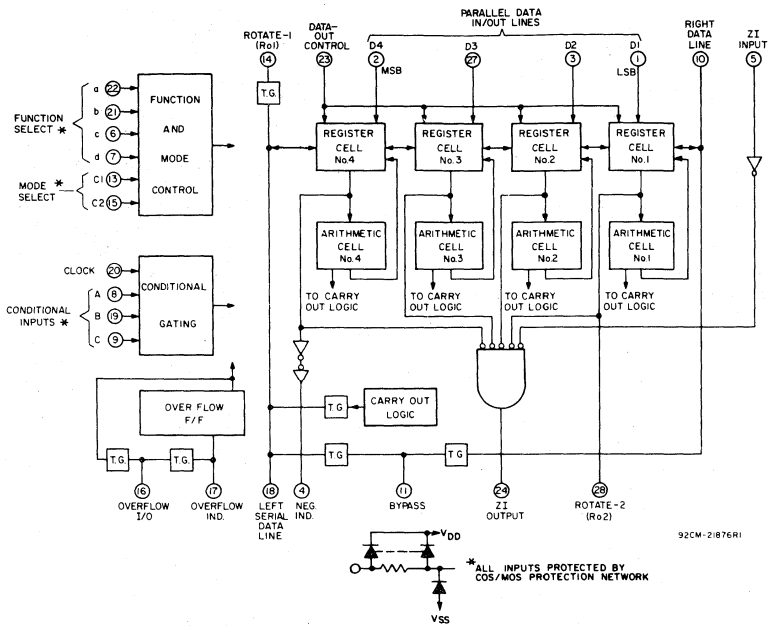


Fig. 9 – Simplified logic diagram.

Data-flow interruptions are shown by shaded areas. With these three ALU's and the four available modes, 61 more system combinations can be formed. If 4 ALU's are used, 4^4 combinations (256) are possible. *Fig.11* shows a diagram of 4 CD4057A's interconnected to form a 16-bit parallel processor.

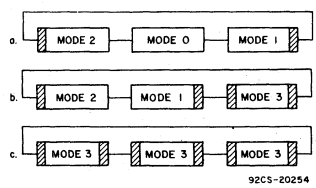


Fig. 10 – "Mode" connections for parallel processor:
(a) 12-bit unit,
(b) one 8-bit and one 4-bit unit
(c) three 4-bit units.

NOTE: The BYPASS terminal of the "most significant" CD4057A is connected to the bypass terminal of the "least significant" CD4057A. The bypass terminals on all other CD4057A's are left floating. This interconnection is performed whenever more than one CD4057A are used to form a processor.

INSTRUCTION REPERTOIRE

Four encoded lines are used to represent 16 instructions. Encoded instructions are as follows:

a	b	c	d	
0	0	0	0	NO-OP (Operational Inhibit)
0	0	0	1	AND
0	0	1	0	Count down
0	0	1	1	Count up
0	1	0	0	Subtract Stored number from zero (SMZ)
0	1	0	1	Subtract from parallel data lines (SM) (stored number from parallel data lines)
0	1	1	0	Add (AD)
0	1	1	1	Subtract (SUB) (Parallel data lines from stored number)
1	0	0	0	Set to all ones (SET)
1	0	0	1	Clear to all zeroes (CLEAR)
1	0	1	0	Exclusive-OR
1	0	1	1	OR
1	1	0	0	Input Data (From parallel data lines)
1	1	0	1	Left shift
1	1	1	0	Right shift
1	1	1	1	Rotate (cycle) right

All instructions are executed on the positive edge of the clock.

PARALLEL COMMANDS

a. **CLEAR** – sets register to zero.
b. **SET** –sets register to all ones.
c. **OR** –processes contents of register with value on parallel-data lines in a logical OR function.
d. **AND** –processes contents of register with value on parallel-data lines in a logical AND function.
e. **Exclusive-OR** – processes contents of register with data on parallel-data lines in a logical Exclusive-OR function.
f. **IN** –loads data on parallel-data lines into register.
g. **DATA OUT CONTROL** – unloads contents of register and overflow flip-flop onto parallel data lines and overflow I/O independent of all other controls.
h. **SUB:**
   In Mode 0, adds to the contents of the register the one's complement of the data on the parallel-data lines. Carries can enter on the right serial data line and can leave on the left serial data line. The overflow indicator does not change state.
   In Mode 1, adds to the contents of the register the two's complement of the data on the parallel-data lines. Generated carries can leave on the left serial line. The CARRY IN is set to zero. The overflow indicator does not change state.
   In Mode 2, same as Mode 0, except carries cannot leave on the right serial-data line.The absence or presence of an overflow is registered.
   In Mode 3, same as Mode 1, except carries cannot leave on the left serial-date line. The absence or presence of an overflow is registered.
i. **COUNT UP:**
   In Mode 0, adds to the contents of the register the data on the right serial-data line and permits any resulting carry to leave on the left serial-data line. No data enters the parallel-data lines.
   In Mode 1, internally adds a one to the contents of the register and permits any resulting carry to leave on the left serial-data line. No data enters or leaves the right serial-data line.
   In Mode 2, adds to the contents of the register the data on the right serial-data line. No data enters or leaves the left serial-data line.
   In Mode 3, internally adds a one to the contents of the register No data enters or leaves the register on any serial-data or parallel-data line.
   In all modes, with the DATA OUT control high

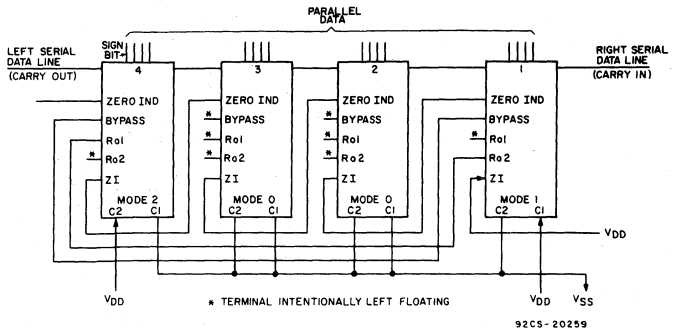


Fig. 11 — Connection for 16-bit arithmetic logic unit.

the count is presented on the parallel data lines (D1-D4).

j. COUNT DOWN:

In Mode 0, subtracts a one (2's complement form) from the contents of the register and adds to this result the data on the right serial-data line and permits any resulting carry to leave on the left serial-data line. No data enters on the parallel-data lines.

In Mode 1, internally subtracts a one from the contents of the register and permits any resulting carry to leave on the left serial-data line. No data enters or leaves the right serial-data line.

In Mode 2, subtracts a one from the contents of the register and adds to this result the data on the right serial-data line. No data enters or leaves on the left serial-data line.

In Mode 3, internally subtracts a one from the contents of the register. No data enters or leaves on the serial-data lines.

In all modes, with the DATA OUT control high the count is presented on the parallel data lines (D1-D4).

k. ADD(AD):

In Mode 0, adds the contents of the register to the data on the parallel-data lines and the right serial-data line. Any resulting carry can leave on the left serial-data line. The overflow indicator does not change state.

In Mode 1, adds the contents of the register to the data on the parallel-data lines and allows any resulting carry to leave on the left serial-data line. The right serial-data line is open-circuited. The overflow indicator does not change state. The CARRY-IN is set to zero.

In Mode 2, adds the contents of the register to the data on the parallel data lines and the right serial-data line. Any overflow sets the overflow indicator. The left serial-data line is open-circuited. The absence or presence of an overflow is registered.

In Mode 3, adds contents of the register to the data on the parallel-data lines. Any resulting carry sets the overflow indicator. The two serial-data lines are open circuited. The absence or presence of an overflow is registered. The CARRY-IN is set to zero.

l. SM — same operation as AD except the contents of the register are two's complemented during addition in Mode 1 and Mode 3. In Mode 0 or Mode 2, the contents of the register are one's complemented and added to the data on the right serial-data line and the parallel-data lines. Overflows occurring in Mode 1 or Mode 0 do not alter the overflow indicator. The presence or absence of overflows is registered on the overflow indicator in Mode 2 or Mode 3.

m. SMZ:

In Mode 0, one's complements the contents of the register and adds the data on the right serial-data line to the contents of the register. Any resulting carry can leave on the left serial-data line. The overflow indicator does not change state.

In Mode 1, two's complements the contents of the register and permits any carry to leave on the left serial-data line. No data can enter the right serial-data line. The overflow indicator does not change state. The CARRY-IN is set to zero.

In Mode 2, one's complements the contents of the register and adds the data on the right serial-data line to the contents of the register. Carries cannot leave the left serial data line. The absence or presence of an overflow alters the overflow indicator.

In Mode 3, two's complements the contents of the register. Serial data can neither enter the right serial-data line nor leave the left serial-data line. The overflow indicator is at zero. The CARRY-IN is set to zero.

n. NO-OP — no operation takes place, The clock input is inhibited and the state of all registers and indicators remains unchanged.

SERIAL-SHIFT OPERATIONS

a. ROTATE (cycle) RIGHT — This operation is internal. The contents of the register shift to the right, cyclic fashion with the leftmost stage accepting data from the rightmost stage regardless of the mode. Data can leave the register serially on the right data line only while the register is in Mode 1 or Mode 0. Data can enter the left data line serially while the register is in Mode 1 or Mode 0. The Ro1 terminal of the "Most Significant" CD4057A must be connected to the Ro2 terminal of the "Least Significant" CD4057A. All other Ro1 and Ro2 terminals must be left floating. When only one CD4057A is used, Ro1 must be connected to Ro2.

b. RIGHT SHIFT — The contents of the register shift to the right and serial operations are as follows:

In Mode 0, data can enter serially on the left data line, shift through the register, and leave on the right data line.

In Mode 1, data can enter serially on the left data line. The right data line effectively is open - circuited.

In Mode 2, data can leave serially on the right data line. The left data line effectively is open-circuited. Vacant spaces are filled with zeros.

In Mode 3, serial data can neither enter nor leave the register; however,the contents shift to the right and vacated places are filled with zeros.

In all modes, with the DATA OUT control high the data is presented on the parallel data lines (D1-D4).

c. **LEFT SHIFT** – The contents of the register shift to the left and serial operations are as follows;

In Mode 0, data can enter the right data line, shift through the register, and leave on the left data line.

In Mode 1, data can leave serially on the left data line. The right data line effectively is open-circuited. All vacant positions are filled with zeros.

In Mode 2, data can enter serially on the right data line. The left data line effectively is open-circuited.

In Mode 3, data can neither enter nor leave the register; however, the contents shift to the left, and vacated places are filled with zeros.

In all modes, with the DATA OUT control high the data is presented on the parallel data lines (D1-D4).

Because the "DATA OUT" control instruction is independent of the other 16 instructions, care must be taken not to activate this control when data are to be loaded into the processor. This instruction should only be activated when the processor is executing a NO-OP, any SHIFT, SMZ, COUNT UP or DOWN, CLEAR, or SET.

If a data line, serial or parallel, is used as an input and the logic state of that line is not defined (i.e., the line is an open circuit),then the result of any operation using that line is undefined.

OPERATIONAL SEQUENCE FOR ARITHMETIC ADD CYCLE

1. Apply IN Instruction and Word A on Parallel Data Lines (D1–D4).
2. Apply CLOCK to load Word A into the register.
3. Apply OP CODE Instruction and Word B on Data Lines.
4. Apply CLOCK to load resulting function of A and B into the register.
5. Apply "DATA OUT" control to present result to Parallel Data Lines.

NOTE: Transitions of Step 2 and Step 3 may occur almost simultaneously: i.e. separated by only one data-hold time.

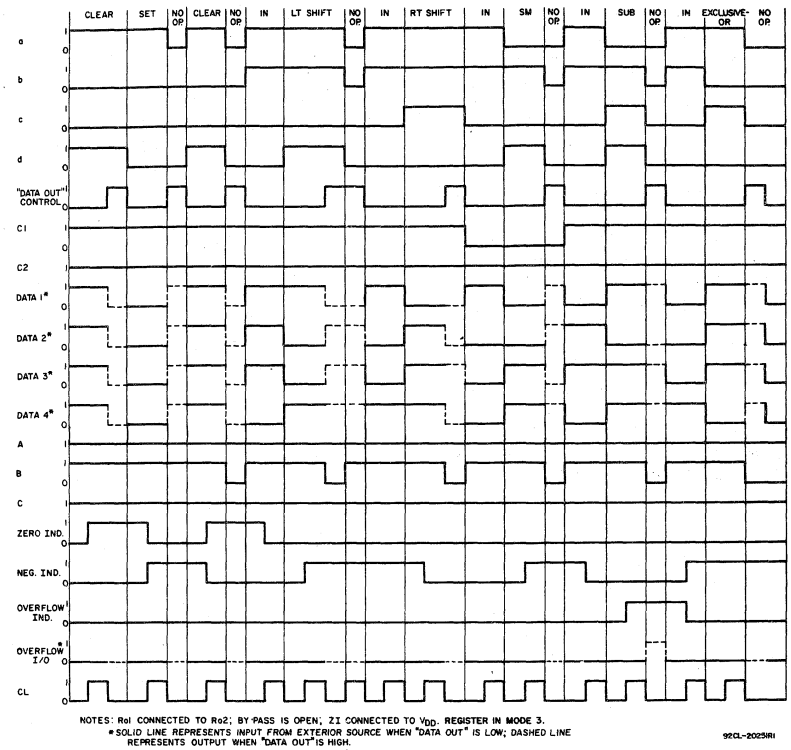


Fig. 12 – Timing diagram.

NEGATIVE-NUMBER DETECTION

The NEG IND terminal of the CD4057A is connected to the output of the flip-flop that is in the most significant bit position. A "1" on the NEG IND terminal indicates a negative number is in the register. This detection is also independent of modes.

ZERO DETECTION

The condition of "all zeros" is indicated by a "1" on the Zero Indicator terminal of the "Most Significant" CD4057A. As shown in Fig. 11, terminal ZI of the CD4057A containing the least significant set of bits is connected to V_{DD}. Zero indication is independent of modes.

COMPLEMENTING NUMBERS

1. One's complement of number in ALU register.
   a) ALU must be in MODE 0 or MODE 2.
   b) Zero on Rt. Data Line.
   c) Execute an SMZ instruction.

(Continued)

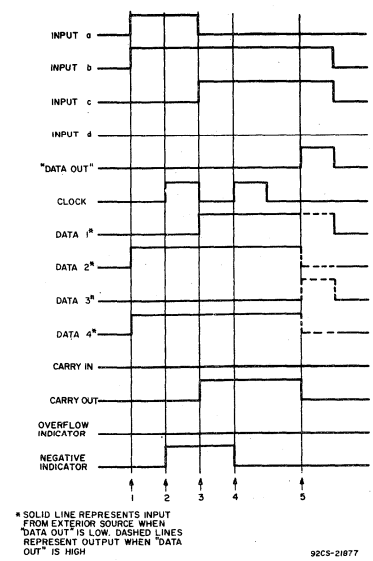
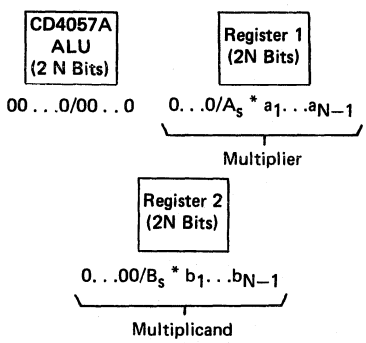


Fig. 13 – Add cycle waveforms.

2. One's complement of number to be loaded into ALU register.
   a) If zero indicator output is low, execute a CLEAR instruction, and make Rt. Data Line = 0.
   b) ALU must be in MODE 0 or MODE 2.
   c) Execute an SUB instruction.
3. Two's complement of number in ALU register.
   a) ALU must be in MODE 1 or MODE 3.
   b) Execute an SMZ instruction.
4. Two's complement of number to be loaded into ALU register.
   a) If zero indicator output is low, execute a CLEAR instruction, and make Rt. Data Line = 0.
   b) ALU must be in MODE 1 or MODE 3.
   c) Execute an SUB instruction.

The following algorithms are given as a general guideline to demonstrate some of the capabilities of the CD4057A.

MULTIPLICATION OF TWO N-BIT NUMBERS

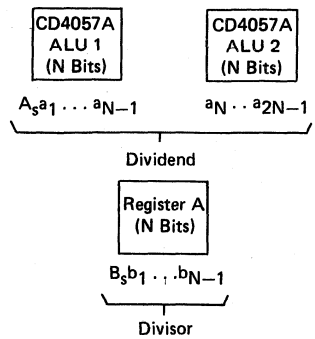


*A_s and B_s are sign bits

Multiplication Algorithm

1. Clear ALU to Zero
2. Store $A_s \oplus B_s$ in External Flip-Flop.
3. If A_s = 1, Complement Register 1.
4. If B_s = 1, Complement Register 2.
5. Load Register 2 into ALU.
6. Do shift Left on ALU N Times (N = number of bits).
7. Do N Times:
   (1)
   a) If MSB of ALU = 1 (Negative Indicator = High), Then shift ALU left 1 bit; add Register 1 to ALU.
   b) If MSB of ALU = 0 (Negative Indicator = Low) Then shift ALU left 1 bit.
8. If $A_s \oplus B_s$ = 1, then Complement ALU.
9. Answer in ALU.

Division Algorithm



1. Store $A_s \oplus B_s$ in External Flip-Flop.
2. If A_s = 1, complement ALU 1 and ALU 2.
3. If B_s = 1, complement Register A.
4. Check for Divisor = 0
   a) If Divisor = 0; stop, indicates division by 0.
   b) If Divisor $\neq$ 0; continue.
5. Apply SUB instruction to ALU 1 and Register A to ALU 1 data lines.
   a) If C_o = 0 (Dividend < Divisor), Stop, indicates overflow.
   b) If C_o = 1 (Dividend $\geq$ Divisor), Continue.
6. Put a zero on RT data line of ALU 2 and shift ALU 1 & ALU 2 left 1 bit.
7. Do "N" times.
   a) If C_o = 1, then clock ALU 1, and put a 1 on right data line of ALU 2.
   b) If C_o = 0, then no clock, and put a 0 on right data line of ALU 2.
8. If sign Flip Flop = 1, complement ALU 2.
9. Answer in ALU 2.

CONDITIONAL OPERATION

Inhibition of the clock pulse can be accomplished with a programmed NO-OP instruction or through conditional input terminals A,B,and C.In a system of many CD4057A's, each CD4057A can be made to automatically control its own operation or the operation of any other CD4057A in the system in conjunction with the Overflow, Zero, or Negative (Number) indicators. Table II, the conditional inputs, truth table, defines the interactions among A,B, and C.

TABLE II – CONDITIONAL-INPUTS TRUTH TABLE

A	B	C	OPERATION PERMITTED
0	X	X	Yes
1	0	0	Yes
1	0	1	No
1	1	0	No
1	1	1	Yes

X = don't care

Two examples of how the conditional operation can be used are as follows:

1) For the Multiplication Algorithm
   A = 1, for step 7 (1)
   A = 0, for step 7 (2)
   B = 1
   C = negative Indicator
2) For the Division Algorithm
   A = 1, for step 7 (1)
   A = 0, for step 7 (2)
   B = 1
   C = C_o (left data line)

OVERFLOW DETECTION

The CD4057A is capable of detecting and indicating the presence or absence of an arithmetic two's-complement overflow. A two's-complement overflow is defined as having occurred if the signs of the two initial words are the same and the sign of the result is different while performing a carry-generating instruction.

For example:
$$\begin{array}{rr} & 0.011 \\ (+) & \underline{0.110} \\ & 1.001 \end{array}$$

Overflows can be detected and indicated only during operation in Mode 2 or Mode 3 and can occur for only four instructions (AD, SMZ, SM, and SUB). If an overflow is detected and stored in the overflow flip-flop, any one of the five instructions AD, SMZ, SM, SUB, or IN can change the overflow indicator.

When any of the three subtraction instructions is used, the sign bit of the data being subtracted is complemented and this value is used as one of the two initial signs to detect overflows. If an overflow has occurred, the final sign of the sum or difference is one's complemented and stored in the most-significant-bit position of the register.

The overflow flip-flop is updated at the same time the new result is stored in the CD4057A. Whenever data on the parallel-data lines are loaded into the CD4057A, whatever is on the Overflow I/O line is loaded into the overflow flip-flop. Also, whenever data are dumped on the parallel data lines from the CD4057A, the contents of the overflow flip-flop are dumped on the Overflow I/O line. Thus overflows may be stored elsewhere and then fed into the CD4057A at another time.

OPERATIONAL SEQUENCE AND WAVEFORMS FOR PROPAGATION-DELAY MEASUREMENTS

1. DATA-IN-to-CARRY OUT and DATA IN-to-SUM OUT
   - A. Apply Word A and IN instruction
   - B. Apply Clock to load word A into register
   - C. Apply AD instruction
   - D. Apply Word B (data in)
   - E. Apply Clock to load result (sum out)
   - F. Apply DATA OUT CONTROL to look at result
2. CARRY IN-to-CARRY OUT and CARRY IN-to-SUM OUT
   - A. Apply Word A and IN instruction
   - B. Apply Clock to load word A into register
   - C. Apply AD instruction
   - D. Apply Word B
   - E. Apply CARRY IN (carry in)
   - F. Apply Clock to load result (sum out)
   - G. Apply DATA OUT CONTROL to look at result

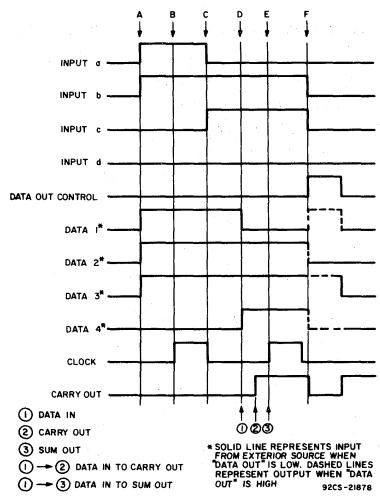


Fig. 14(a) — DATA IN-to-CARRY OUT and DATA IN-to-SUM OUT.

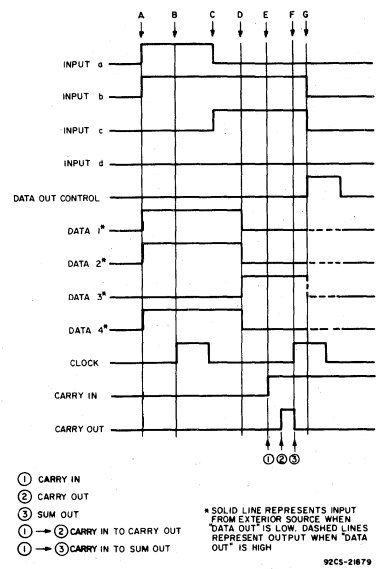


Fig. 14(b) — CARRY IN-to-CARRY OUT and CARRY IN-to-SUM OUT.

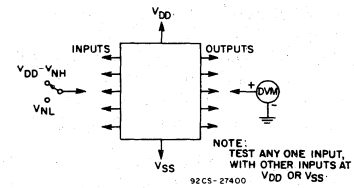


Fig. 15 — Noise-immunity test circuit.

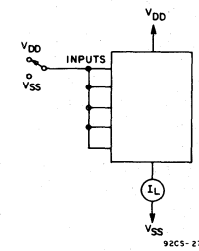


Fig. 16 — Quiescent-device-current test circuit

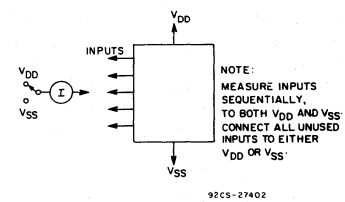


Fig. 17 — Input-leakage-current test circuit.

TYPICAL APPLICATION

The CD4057A has been designed for use as a parallel processor in flexible, programmable, easily expandable, special or general purpose computers, where minimization of external connections and data busing are primary design goals. The block diagram of Fig. 18 is an example of a computer that processes 8 bits in parallel.

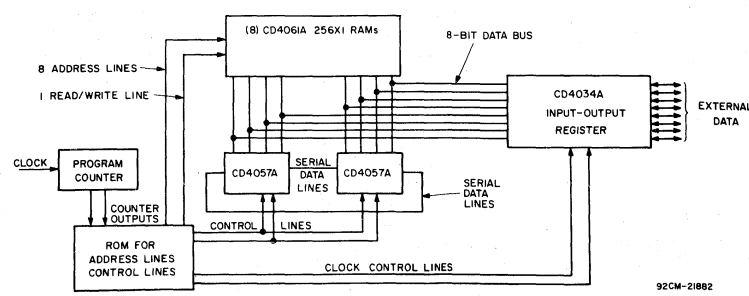


Fig. 18 — Example of computer organization using CD4057A.

COS/MOS Programmable Divide-by-"N" Counter

Standard "A"-Series Types (3-to-15-Volt Rating)

RCA-CD4059 standard "A"-Series types are divide-by-N down-counters that can be programmed to divide an input frequency by any number "N" from 3 to 15,999. The output signal is a pulse one clock-cycle wide occurring at a rate equal to the input frequency divided by N. This single output has TTL drive capability. The down-counter is preset by means of 16 jam inputs.

The three Mode-Select Inputs Ka, Kb, and Kc determine the modulus ("divide-by" number) of the first and last counting sections in accordance with the truth table shown in Table I. Every time the first (fastest) counting section goes through one cycle, it reduces by 1 the number that has been preset (jammed) into the three decades of the intermediate counting section and into the last counting section, which consists of flip-flops that are not needed for operating the first counting section. For example, in the ÷ 2 mode, only one flip-flop is needed in the first counting section. Therefore the last counting section has three flip-flops that can be preset to a maximum count of seven with a place value of thousands. If ÷ 10 is desired for the first section, Ka is set to 1, Kb to 1, and Kc to 0. Jam Inputs J1, J2, J3, and J4 are used to preset the first counting section and there is no last counting section. The intermediate counting section consists of three cascaded BCD decade (÷ 10) counters presettable by means of Jam Inputs J5 through J16.

The Mode-Select Inputs permit frequency-synthesizer channel separations of 10, 12.5, 20, 25, or 50 parts. These inputs set the maximum value of N at 9999 (when the first counting section divides by 5 or 10) or 15,999 (when the first counting section divides by 8, 4, or 2).

The three decades of the intermediate counting section can be preset to a binary 15 instead of a binary 9, while their place values are still 1, 10, and 100, multiplied by the number of the ÷ N mode. For example, in the ÷ 8 mode, the number from which counting-down begins can be preset to:

3rd decade:	1500
2nd decade:	150
1st decade:	15
Last counting section	1000

The total of these numbers (2665) times 8 equals 21,320. The first counting section can be preset to 7. Therefore, 21,327 is the maximum possible count in the ÷ 8 mode.

The highest count of the various modes is shown in the column entitled Extended Counter Range of Table 1. Control inputs Kb and Kc can be used to initiate and lock the counter in the "master preset" state. In this condition the flip-flops in the counter are preset in accordance with the jam inputs and the counter remains in that state as long as Kb and Kc both remain low. The counter begins to count down from the preset state when a counting mode other than the master preset mode is selected.

The counter should always be put in the master preset mode before the ÷5 mode is selected.

Whenever the master preset mode is used, control signals Kb=0 and Kc=0 must be applied for at least 3 full clock pulses.

After the Master Preset Mode inputs have been changed to one of the ÷ modes, the next positive-going clock transition changes an internal flip-flop so that the countdown can begin at the second positive-going clock transition. Thus, after an MP (Master Preset) mode, there is always one extra count before the output goes high. Fig.1 illustrates a total count of 3 (÷ 8 mode). If the Master Preset mode is started two clock cycles or less before an output pulse, the output pulse will appear at the time due. If the Master Preset Mode is not used the counter jumps back to the "JAM" count when the output pulse appears.

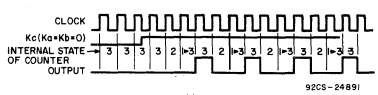
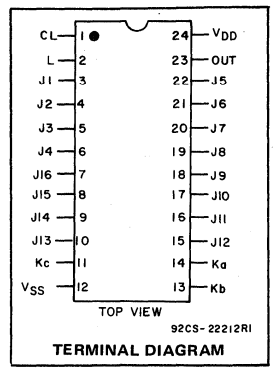


Fig.1 – Total count of 3.

A "1" on the Latch Enable input will cause the counter output to remain high once an output pulse occurs, and to remain in the high state until the latch input returns to "0". If the Latch Enable is "0", the output pulse will remain high for only 1 cycle of the clock-input signal.

As illustrated in the sample applications, this device is particularly advantageous in communication digital frequency synthesis (VHF, UHF, FM, AM, etc.) where programmable divide-by-"N" counters are an integral part of the synthesizer phase-locked-loop subsystem. The CD4059A can also be used to perform the synthesizer "Fixed Divide-by-R" counting function. It is also useful in general-purpose counters for instrumentation functions such as totalizers, production counters, and "time out" timers.



TERMINAL DIAGRAM

Operational and Performance Features:

- **Synchronous Programmable ÷ N Counter: N = 3 to 9999 or 15,999**
- **Presettable down-counter**
- **Fully static operation**
- **Mode-select control of initial decade counting function (÷ 10,8,5,4,2)**
- **T^2L drive capability**
- **Master preset initialization**
- **Latchable ÷ N output**
- **Quiescent current specified to 15 volts**
- **Max. input leakage current of 1 μA at 15 volts, full package-temperature range**
- **1 volt noise margin, full package-temperature range**
- **5-V and 10-V parametric ratings**

Applications

- **Communications digital frequency synthesizers: VHF, UHF, FM, AM, etc.**
- **Fixed or programmable frequency division**
- **"Time out" timer for consumer-application industrial controls**
- **Companion Application Note, ICAN-6374, "Application of the COS/MOS CD4059A Programmable Divide-by-N Counter in FM and Citizens Band Transceiver Digital Tuners"**

The CD4059A series types are available in a 24-lead ceramic dual-in-line package, 24-lead dual-in-line plastic package, 24-lead ceramic flat pack, and in chip form.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, V_{DD} (Voltages referenced to V_{SS} terminal) . . . . −0.5 to +15 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (Package Type E) . . . . . 500 mW
For T_A = +60 to +85°C (Package Type E) . . . . . Derate Linearly to 200 mW
For T_A = −55 to +100°C (Package Types D,K,H) . . . . . 500 mW
For T_A = +100 to +125°C (Package Types D,K,H) Derate Linearly to 100 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full package-temperature range (All package types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
Package Types D,K,H . . . . . −55 to +125°C
Package Type E . . . . . −40 to +85°C
STORAGE-TEMPERATURE RANGE (T_{STG}) . . . . . −65 to 150°C
LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

OPERATING CONDITIONS AT T_A = 25°C (Unless otherwise specified)

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V_{DD}	Min.	Max.	Units
Supply Voltage Range (over full temp. range)	—	3	12	V
Clock Pulse Width	5 10	200 100	— —	ns
Clock Input Frequency	5 10	— —	1.5 3	MHz
Clock Input Rise and Fall Time	5 10	— —	15 5	μs

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions V_O (V)	Conditions V_{IN} (V)	Conditions V_{DD} (V)	Limits *Values at −55°C,+25°C,+125°C Apply to D,K,H Packages; Values at −40°C,+25°C,+85°C Apply to E Packages* −55°	−40°	+85°	+125°	+25° Min.	+25° Typ.	+25° Max.	Units
Quiescent Device Current, I_L Max.			5	10	10	700	300	—	0.02	10	μA
			10	20	20	200	400	—	0.02	20	
			15	—	—	—	—	—	—	500	
Output Voltage: Low Level, V_{OL} Max.		0,5	5	0.05				—	0	0.05	V
		0,10	10	0.05				—	0	0.05	
High Level, V_{OH} Min.		0,5	5	4.95				4.95	5	—	
		0,10	10	9.95				9.95	10	—	
Noise Immunity: Inputs Low, V_{NL} Min.			5	1.5				1.5	2.25	—	V
			10	3				3	4.5	—	
Inputs High, V_{NH} Min.			5	1.5				1	2.25	—	
			10	3				3	4.5	—	
Noise Margin: Inputs Low, V_{NML} Min.	4.5		5	1							V
	9		10	1							
Inputs High, V_{NMH} Min.	0.5		5	1							
	1		10	1							
Output Drive Current: N-Channel (Sink) I_{DN} Min.	0.4		5	2.5	2.3	1.6	1.4	2	4	—	mA
	0.5		10	5	4.7	3.3	2.8	4	9	—	
P-Channel (Source) I_{DP} Min.	2.5		5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	—	
	4.6		5	−0.5	−0.45	−0.36	−0.3	−0.4	−0.8	—	
	9.5		10	−1.1	−1	−0.75	−0.65	−0.9	−1.8	—	
Input Leakage Current:* I_{IL}, I_{IH} Max.			15	±1					$\pm 10^{-5}$	±1	μA

* Any Input

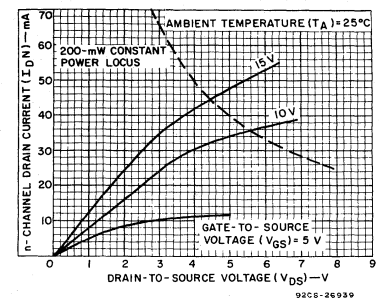


Fig.2 — Minimum output n-channel drain characteristics.

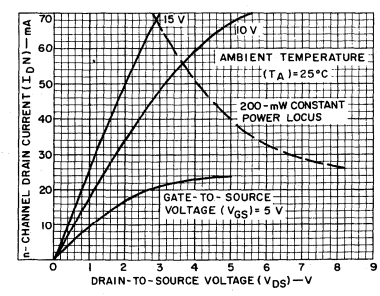


Fig.3 — Typical output n-channel drain characteristics.

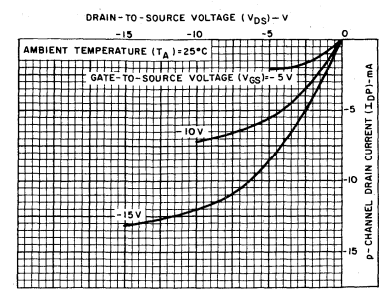
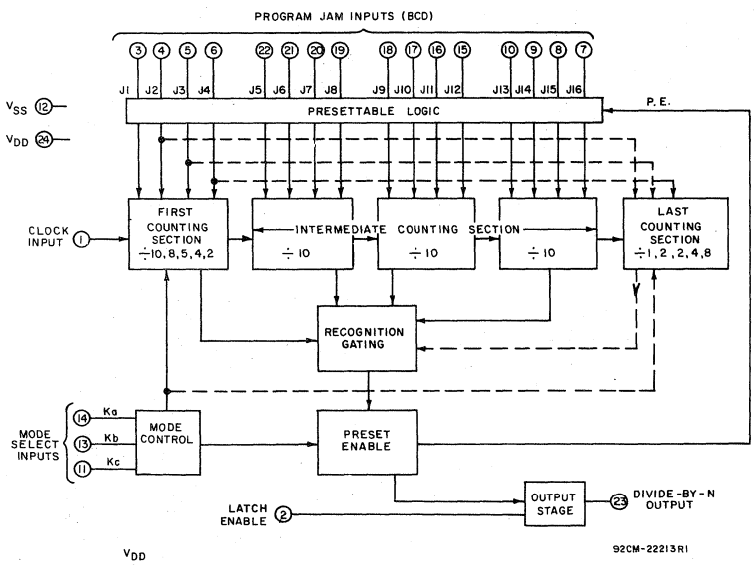
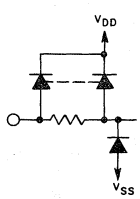


Fig.4 — Minimum output p-channel drain characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS AT $T_A = 25^oC$, $C_L = 50$ pF, Input $t_r, t_f = 20$ ns, $R_L = 200$ kΩ

CHARACTERISTIC	CONDITIONS V_{DD} (V)	LIMITS ALL PACKAGES Min.	Typ.	Max.	UNITS
Propagation Delay Time; t_{PHL}, t_{PLH}	5	–	180	360	ns
	10	–	90	180	
Transition Time:					
t_{THL}	5	–	35	70	ns
	10	–	20	40	
t_{TLH}	5	–	100	200	
	10	–	50	100	
Maximum Clock Input Frequency, f_{CL}	5	1.5	3	–	MHz
	10	3	6	–	
Average Input Capacitance, C_I (any input)	–	–	5	–	pF





ALL INPUTS (TERMS. 1-11, 13-22) PROTECTED BY COS/MOS PROTECTION NETWORK

Fig.5 – Functional block diagram.

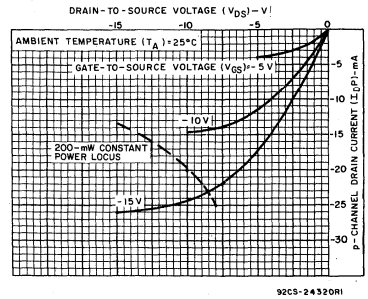


Fig.6 – Typical output p-channel drain characteristics.

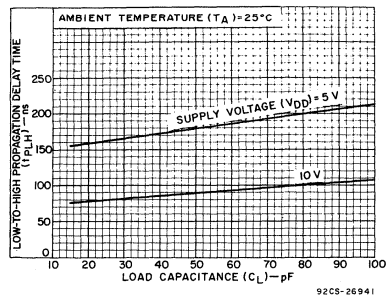


Fig.7 – Typical low-to-high propagation delay time vs. load capacitance.

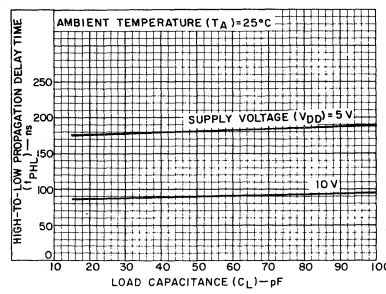


Fig.8 – Typical high-to-low propagation delay time vs. load capacitance.

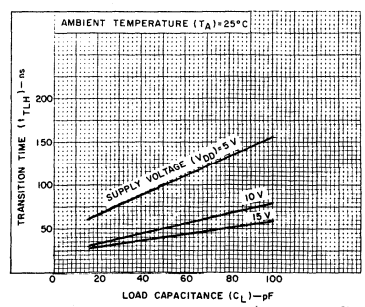


Fig.9 – Typical low-to-high transition time vs. load capacitance.

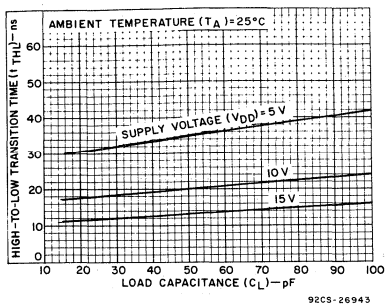


Fig.10 – Typical high-to-low transition time vs. load capacitance.

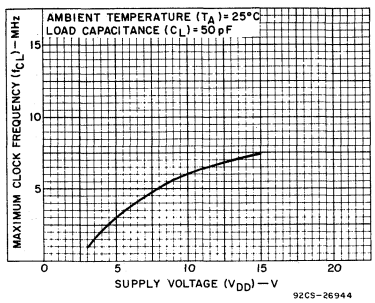


Fig.11 – Typical max. clock frequency vs. supply voltage.

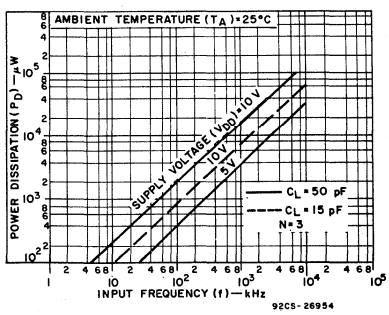


Fig.12 – Typical power dissipation vs. input frequency.

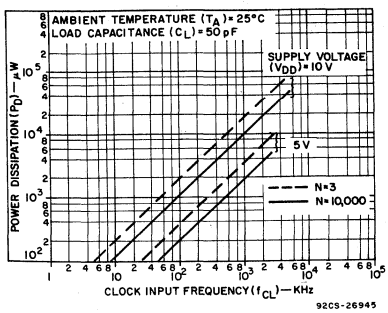


Fig.13 – Typical power dissipation vs. clock input frequency.

TABLE I

MODE SELECT INPUT			FIRST COUNTING SECTION			LAST COUNTING SECTION			COUNTER RANGE	
									DESIGN	EXTENDED
Ka	Kb	Kc	MODE Di-vides by:	Can be preset to a max of:	Jam▲ inputs used:	MODE Di-vides by:	Can be preset to a max of:	Jam▲ inputs used:	Max.	Max.
1	1	1	2	1	J1	8	7	J2,J3,J4	15,999	17,331
0	1	1	4	3	J1,J2	4	3	J3,J4	15,999	18,663
1	0	1	5#	4	J1,J2,J3	2	1	J4	9,999	13,329
0	0	1	8	7	J1,J2,J3	2	1	J4	15,999	21,327
1	1	0	10	9	J1,J2,J3,J4	1	0	–	9,999	16,659
X	0	0	MASTER PRESET			MASTER PRESET			–	–

X = Don't Care

▲ J1 = Least significant bit.
J4 = Most significant bit.

#Operation in the ÷5 mode (1st counting section) requires going through the Master Preset mode prior to going into the ÷5 mode. At power turn-on, kc must be a logic "O" for a period of 3 input clock pulses after V_{DD} reaches a minimum of 3 volts.

HOW TO PRESET THE CD4059A TO DESIRED ÷ N

The value N is determined as follows:

N = [MODE*] [1000 x Decade 5 Preset + 100X Decade 4 Preset + 10X Decade 3 Preset + 1X Decade 2 Preset] + Decade 1 Preset (1)

* MODE= First counting section divider (10, 8, 5, 4 or 2)

To calculate preset values for any N count, divide the N count by the Mode.

The resultant is the corresponding preset values of the 5th through 2nd decade with the remainder being equal to the 1st decade value.

$$\text{Preset Value} = \frac{N}{\text{Mode}} \quad (2)$$

Examples:

A) N = 8479, Mode = 5

1695 + 4 ← Preset Values

5 | 8479

Mode N

MODE SELECT = 5

Ka	Kb	Kc
1	0	1

PROGRAM JAM INPUTS (BCD)

4			1	5			9				6			
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
0	0	1	1	1	0	1	0	1	0	0	1	0	1	1	0

To verify the results use equation 1 :

N = 5 (1000X 1 + 100 X 6 + 10 X 9 + 1 X 5) + 4

N = 8479

B) N = 12382, Mode = 8

1547 + 6

8 | 12382

MODE SELECT = 8

Ka	Kb	Kc
0	0	1

PROGRAM JAM INPUTS

6			1	7				4				5			
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
0	1	1	1	1	1	1	0	0	0	1	0	1	0	1	0

To verify:

N = 8 (1000 X 1 + 100 X 5 + 10 X 4 + 1 X 7) + 6

N = 12382

MODE SELECT = 10

C) N = 8479, Mode = 10

$10 \overline{)8479}$ = 0847 + 9

Ka	Kb	Kc
1	1	0

PROGRAM JAM INPUTS

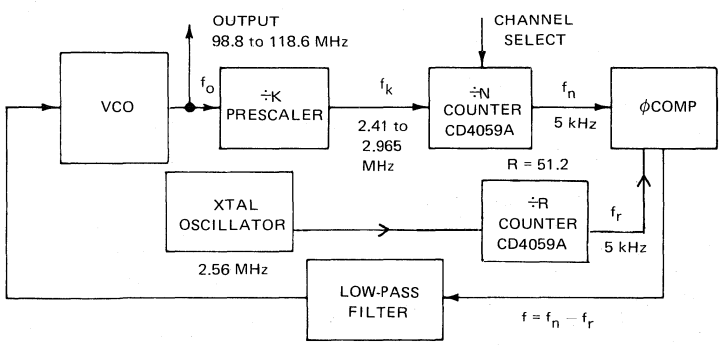
9				7				4				8			
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
1	0	0	1	1	1	1	0	0	0	1	0	0	0	0	1

To Verify:

N = 10 (1000 X 0 + 100 X 8 + 10 X 4 + 1 X 7) + 9

N = 8479

DIGITAL PHASE-LOCKED LOOP (PLL) FOR FM BAND SYNTHESIZER



1) Calculating Min & Max "N" Values :

Output Freq. Range (f_O) = 98.8 to 118.6 MHz

Channel Spacing Freq. (f_C) = 200 kHz

Division Factor (k) = 40

$$\text{Reference Freq. (fr)} = \frac{f_C}{k} = \frac{200}{40}\ \text{kHz} = 5\ \text{kHz}$$

$$f_k = \frac{f_o}{40} \quad : \quad f_k\text{Max.} = \frac{118.6\ \text{MHz}}{40} = 2.965\ \text{MHz}; \quad f_k\text{Min} = \frac{98.8\ \text{MHz}}{40} = 2.47\ \text{MHz}$$

$$\therefore N = \frac{f_o}{f_c}$$

$$N_{Max} = \frac{118.6\ \text{MHz}}{200\ \text{kHz}} = 593 \qquad N_{Min} = \frac{98.8\ \text{MHz}}{200\ \text{kHz}} = 494 \qquad R = \frac{2.56\ \text{MHz}}{5\ \text{kHz}} = 512$$

"CASCADING" VIA OTHER COUNTERS

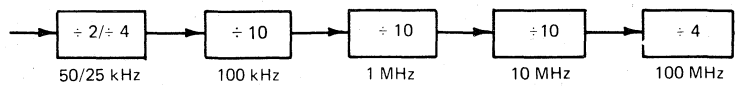
Fig. 14 shows a BCD-switch compatible arrangement suitable for ÷ 8 and ÷ 5 modes, which can be adapted, with slight changes, to the other divide-by-modes. In order to be able to preset to any number from three to about 256,000, while preserving the BCD-switch compatible character of the jam inputs, a rather complex cascading scheme is required. Such a cascading scheme is necessary because the CD4059A can never be preset to a count less than 3 and logic is needed to detect the condition that one of the numbers to be preset in the CD4059A is rather small. In order to simplify the detection logic, only that condition is detected where the jam inputs to terminals 6, 7, and 9 would be low during one count. If such a condition is detected, and if at least 1 is expected to be jammed into the MSB counter, the detection logic removes one from the number to be jammed into the MSB counter (with a place value of 2000 times the divide-by-mode) and jams the same 2000 into the CD4059A by forcing terminals 6, 7, and 9 high.

The clock of the CD4013A may be driven directly from the output of the CD4059A, as shown by dashed option (1), or by the inverted output of the CD4059A, option (2). If option (2) is used the CD4029A cannot count cycles shorter than 3. If option (1) is used propagation delay problems may occur at high counting speeds.

The general circuit in Fig.14 can be simplified considerably if the range of the cascaded counters does not have to start at a very low value. Fig.15 shows an arrangement in the ÷ 4 mode, where the counting range extends in a BCD-switch compatible manner from 88,003 to 103,999. The arrangement shown in Fig.15 is easy to follow; once during each cycle, the less significant digits are jammed in (14,712 in this case) and then 11,000 (4 x 2750) is jammed in eight times in succession, by forcing jam inputs high or low, as required.

Numbers larger than the extended counter range can also be produced by cascading the CD4059A with some other counting device. Fig.16 shows such an arrangement where only one fixed divide-by number is desired which is close to three times the extended counter range as shown in the last column of Table I. The dual flip-flop wired to produce a ÷ 3 count, can be replaced by other counters such as the CD4029, CD4510, CD4516, CD4017, or the CD4022. In Fig.16 the ÷ N subsystem is preset once to a number smaller than the desired divide-by number. This smaller number represents the less significant digits of the divide-by number. The subsystem is then preset one or more times to a round number (e.g. 1000, 2000) and multiplied by the number of the divide-by mode (÷ 2 in the example of Fig.16). It is important that the second counting device has an output that is high or low, as the case may be, during only one of its counting states.

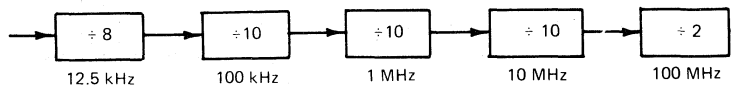
2) ÷ N Counter Configuration for UHF – 220 to 400 MHz
Channel Spacing: 50 kHz or 25 kHz



$$N_{Max} = \frac{400\ MHz}{25\ kHz} = 16{,}000 \qquad N_{Max} = \frac{400\ MHz}{50\ kHz} = 8{,}000$$

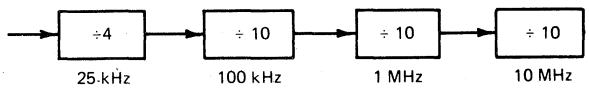
$$N_{Min} = \frac{220\ MHz}{25\ kHz} = 8{,}800 \qquad N_{Min} = \frac{220\ MHz}{50\ kHz} = 4{,}400$$

3) ÷ N Counter Configuration to VHF – 116 MHz
Channel Spacing = 12.5 kHz



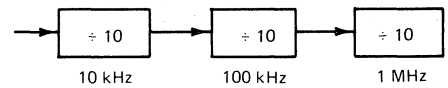
$$N_{Max} = \frac{160\ MHz}{12.5\ kHz} = 12{,}800 \qquad N_{Min} = \frac{116\ MHz}{12.5\ kHz} = 9{,}300$$

4) ÷ N Counter Configuration for VHF – 30 to 80 MHz
Channel Spacing: 25 kHz



$$N_{Max} = \frac{80\ MHz}{25\ kHz} = 3{,}200 \qquad N_{Min} = \frac{30\ MHz}{25\ kHz} = 1200$$

5) ÷ N Counter Configuration for AM – 995 to 2055 kHz
Channel Spacing = 10 kHz



$$N_{Max} = \frac{2055\ kHz}{10\ kHz} = 205 \qquad N_{Min} = \frac{995\ kHz}{10\ kHz} = 99$$

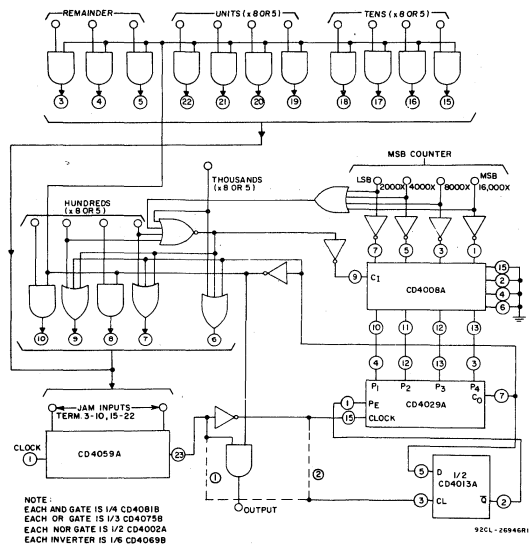


Fig.14 – BCD switch-compatible ÷N system of the most general kind.

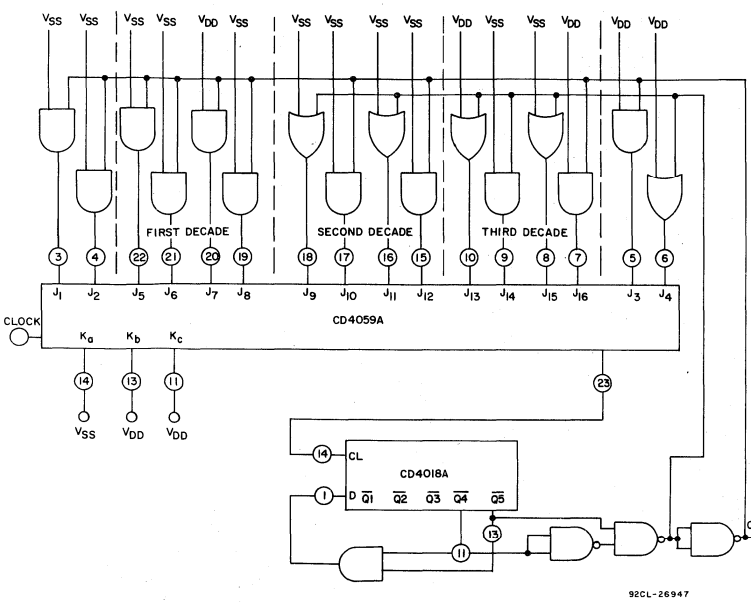
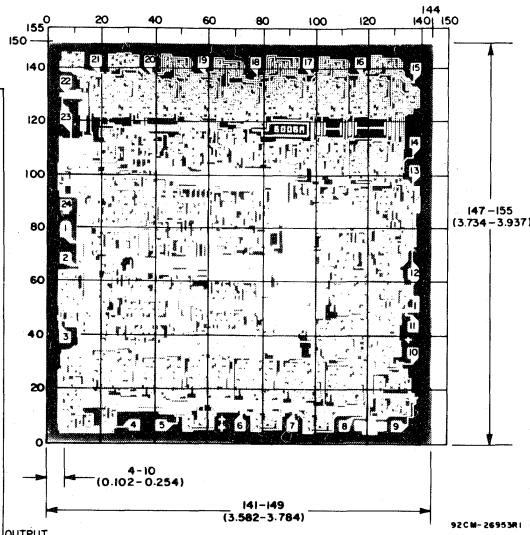


Fig.15 – Dividing by any number from 88,003 to 103,999.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Dimensions and pad layout for CD4059AH.

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

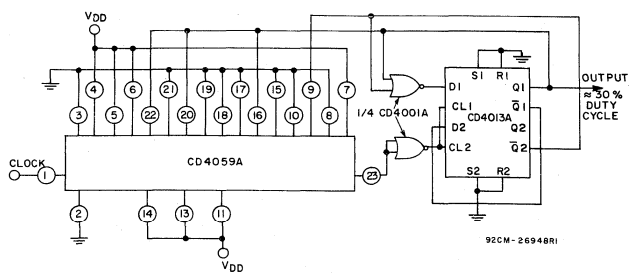


Fig.16 – Division by 47,690 in ÷2 mode.

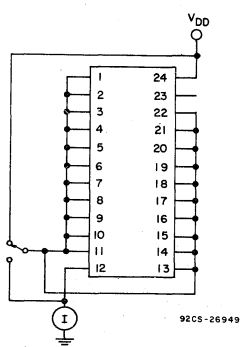


Fig.17 – Quiescent device current test circuit.

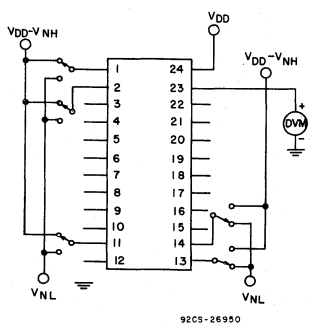


Fig.18 – Noise immunity test circuit.

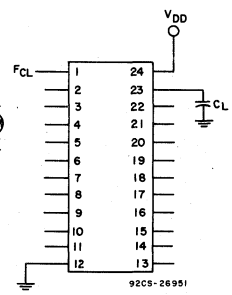


Fig.19 – Power dissipation test circuit (all ÷ modes).

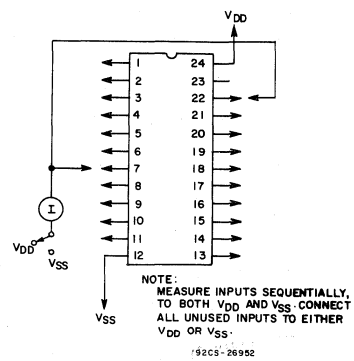


Fig.20 – Input leakage current test circuit.

COS/MOS 14-Stage Ripple-Carry Binary Counter/Divider and Oscillator

The RCA-CD4060A consists of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. A RESET input is provided which resets the counter to the all-O's state and disables the oscillator. A high level on the RESET line accomplishes the reset function. All counter stages are master-slave flip-flops. The state of the counter is advanced one step in binary order on the negative transition of $\phi_I(\phi_O)$. All inputs and outputs are fully buffered.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

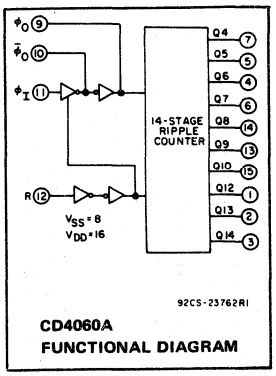
- 4-MHz operating frequency (typ.) at $V_{DD} - V_{SS}$ = 10 V
- Common reset
- Fully static operation
- 10 buffered outputs available
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Oscillator Features:

- All active components on chip
- RC or crystal oscillator configuration

Applications:

- Timers
- Frequency dividers



CD4060A FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
PACKAGE TYPE E . . . . . –40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): . . . . . –0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A = –40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = –55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max . . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D,F,K,H Packages		*E Package*		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Input-Pulse Width, t_W f = 100 kHz	5	400	–	500	–	ns
	10	110	–	125	–	
Input-Pulse Rise & Fall Time, $t_{r\phi}$, $t_{f\phi}$	5	–	15	–	15	μs
	10	–	7.5	–	7.5	
Input-Pulse Frequency, f_ϕ	5	–	1	–	0.9	MHz
	10	–	3	–	2.75	
Reset Pulse Width, t_W	5	1000	–	1250	–	ns
	10	500	–	600	–	

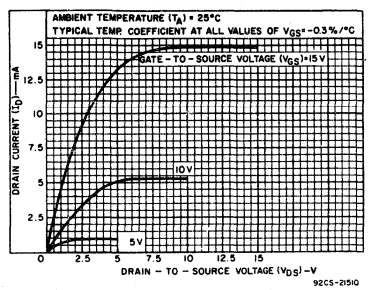


Fig. 1 – Typical n-channel drain characteristics.

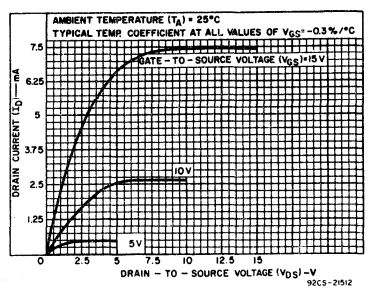


Fig. 2 – Minimum n-channel drain characteristics.

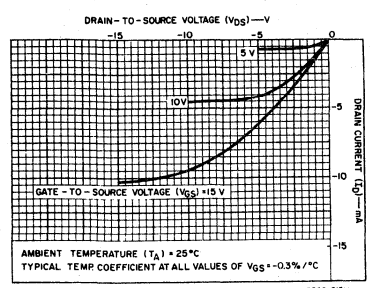


Fig. 3 – Typical p-channel drain characteristics.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				E Package				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current I_L Max.	—	—	5	15	0.5	15	900	50	1	50	700	μA
	—	—	10	25	1	25	1500	100	2	100	1400	
	—	—	15	50	2.5	50	2000	500	5	500	5000	
Output Voltage: Low Level, V_{OL}	—	5	5	0 Typ.; 0.05 Max.								V
	—	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	—	0	5	4.95 Min.; 5 Typ.								
	—	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	—	5	1.5 Min.; 2.25 Typ.								V
	9	—	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	—	5	1.5 Min.; 2.25 Typ.								
	10	—	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	—	5	1 Min.								V
	9	—	10	1 Min.								
Inputs High, V_{NMH}	0.5	—	5	1 Min.								
	1	—	10	1 Min.								
Output Drive Current:* n-Channel (Sink), I_DN Min.	0.5	—	5	0.22	0.36	0.18	0.125	0.21	0.36	0.18	0.15	mA
	0.5	—	10	0.44	0.75	0.36	0.25	0.42	0.75	0.36	0.3	
p-Channel (Source), I_DP Min.	4.5	—	5	-0.15	-0.25	-0.125	-0.085	-0.145	-0.25	-0.125	-0.1	
	9.5	—	10	-0.3	-0.5	-0.25	-0.175	-0.29	-0.5	-0.25	-0.2	
Input Leakage Current, I_{IL}, I_{IH}	Any Input											μA
	—	—	15	$\pm 10^{-5}$ Typ., ±1 Max.								

* Data not applicable to Terminal 9 or 10

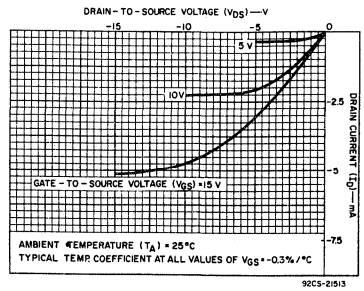


Fig. 4 – Minimum p-channel drain characteristics.

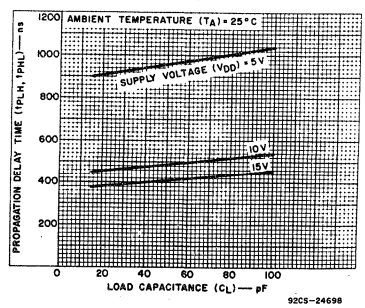


Fig. 5 – Typical propagation delay time vs. load capacitance (ϕ_I to Q4 output).

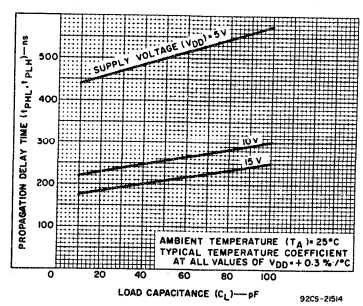


Fig. 6 – Typical propagation delay time vs. load capacitance (Q_n to Q_{n+1}).

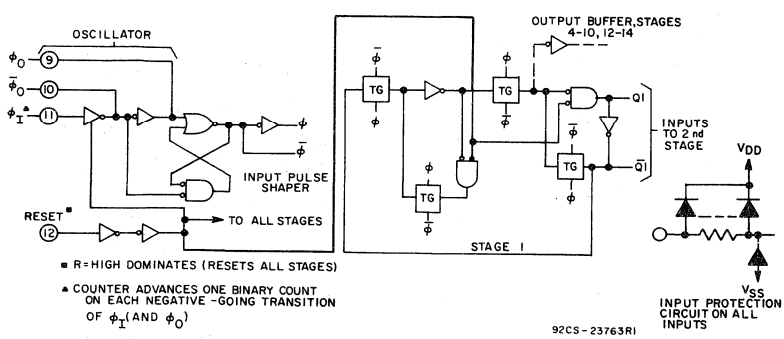


Fig. 7 – Logic diagram of CD4060A oscillator, pulse shaper, and 1 of 14 counter stages.

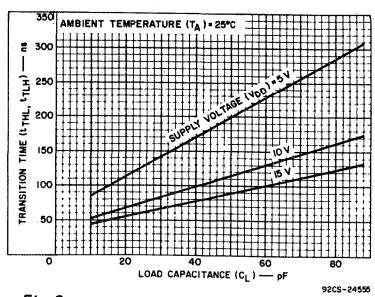


Fig. 8 – Typical output transition time vs. load capacitance.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
			D,F,K,H Packages			*E Package*			
		V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input-Pulse Operation									
Propagation Delay Time, ϕ_I to Q4 Out; t_{PHL}, t_{PLH}		5	–	900	1800	–	900	1900	ns
		10	–	450	900	–	450	950	
Propagation Delay Time, Q_n to Q_{n+1}; t_{PHL}, t_{PLH}		5	–	450	900	–	450	950	ns
		10	–	225	450	–	225	475	
Transition Time, t_{THL}, t_{TLH}		5	–	150	300	–	150	350	ns
		10	–	75	150	–	75	175	
Min. Input-Pulse Width t_W	f=100 kHz	5	–	200	400	–	200	500	ns
		10	–	75	110	–	75	125	
Input-Pulse Rise & Fall Time, $t_{r\phi}$, $t_{f\phi}$		5	–	–	15	–	–	15	μs
		10	–	–	7.5	–	–	7.5	
Max. Input-Pulse Frequency, f_ϕ		5	1	1.75	–	0.9	1.75	–	MHz
		10	3	4	–	2.75	4	–	
Input Capacitance, C_I	Any Input		–	5	–	–	5	–	pF
Reset Operation									
Propagation Delay Time, t_{PHL}		5	–	500	1000	–	500	1250	ns
		10	–	250	500	–	250	600	
Minimum Reset Pulse Width, t_W		5	–	500	1000	–	500	1250	ns
		10	–	250	500	–	250	600	

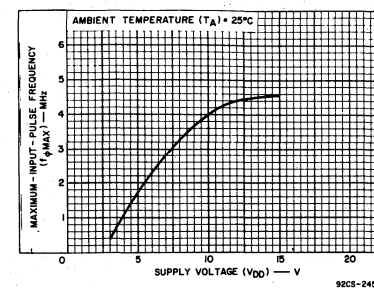


Fig. 9 – Typical maximum-input-pulse frequency vs. supply voltage.

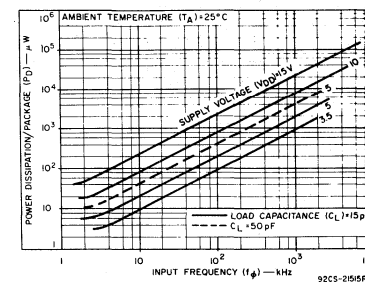


Fig. 10 – Typical dynamic power dissipation characteristics.

TEST PERFORMED WITH UNIT IN ALL "0's" STATE AND ALL "1's" STATE AND INPUTS AT 10 V AND GROUND

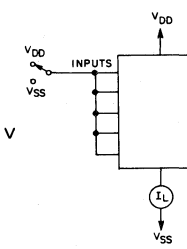


Fig. 11 – Quiescent-device current test circuit.

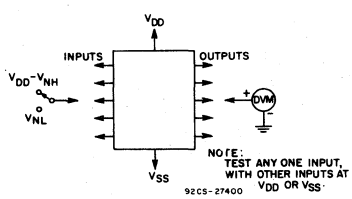


Fig. 12 – Noise-immunity test circuit.

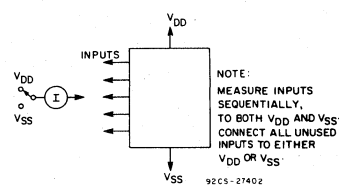


Fig. 13 – Input-leakage-current test circuit.

CD4061A Types

COS/MOS 256-Word by 1-Bit Static Random-Access Memory

The RCA-CD4061A is a single monolithic integrated circuit containing a 256-word by 1-bit fully static, random-access, NDRO memory. The memory is fully decoded and requires 8 address input lines (A_0-A_7) to select one of 256 storage locations. Additional connections are provided for a READ/WRITE command CHIP SELECT DATA IN, and DATA OUT and DATA OUT lines.

To perform READ and WRITE operations the CHIP-SELECT signal must be low. When the CHIP-SELECT signal is high, read and write operations are inhibited and the output is a high impedance. To change addresses, the CHIP-SELECT signal must be returned to a high level, regardless of the logic level of the READ/WRITE input. In a multiple package application, the CHIP-SELECT signal may be used to permit the selection of individual packages.

Output-voltage levels appear on the outputs only when the CHIP SELECT and READ/WRITE signals are both low. Separate data inputs and outputs are provided; they may be tied together, or, to eliminate interaction between READ and WRITE functions, may be used separately. The circuit arrangement permits the outputs from many arrays to be tied to a common bus.

All input and output lines are buffered. The CD4061A output buffers are capable of direct interfacing with TTL devices.

The CD4061A is available in a hermetically sealed 16-lead dual-in-line ceramic package (CD4061AD) or in chip form (CD4061AH).

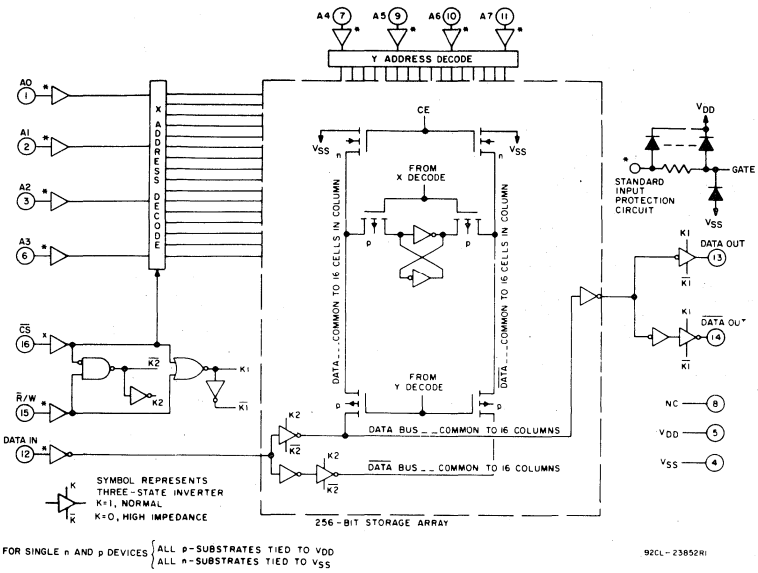


Fig. 1 – CD4061A logic diagram.

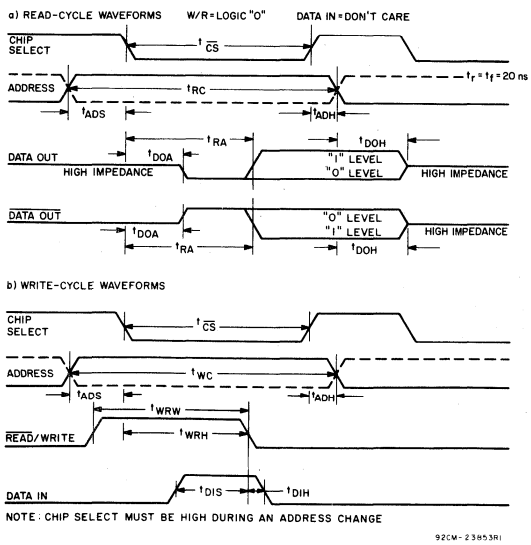


Fig. 2 – Typical write-read waveforms.

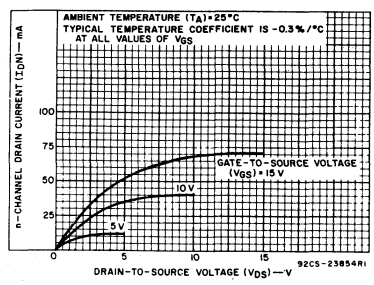


Fig. 3 – Typical n-channel drain characteristics.

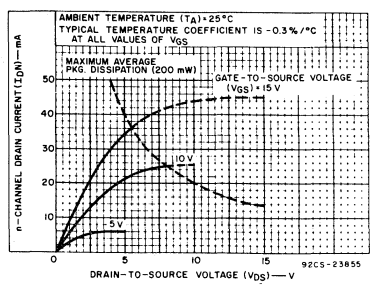


Fig. 4 – Minimum n-channel drain characteristics.

MAXIMUM RATINGS,
Absolute-Maximum Values:

STORAGE-TEMPERATURE RANGE . . . . . −65 to +150°C

OPERATING-TEMPERATURE RANGE . . . . . −55 to +125°C

DC SUPPLY-VOLTAGE RANGE:
V_{DD} . . . . . −0.5 to +15 V

DEVICE DISSIPATION (PER PACKAGE) . . . . . 200 mW

ALL INPUTS . . . . . $V_{SS} \leqslant V_I \leqslant V_{DD}$

RECOMMENDED DC SUPPLY VOLTAGE (V_{DD}-V_{SS}) . . . . . 3 to 15 V

LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

Features:

- **Low standby power: 10 nW/bit (typ.) @ V_{DD} = 10 V**
- **Access time: 380 ns (max.) @ V_{DD} = 10 V**
- **Single 3-to-15 V power supply**
- **COS/MOS input/output logic compatibility**
- **TTL output drive capability**
- **Three-state data outputs for bus-oriented systems**
- **1101-type pin designations**
- **Separate data output and data input lines**
- **Noise immunity: 45% of V_{DD} (typ.)**
- **Fully decoded addressing**
- **Single write/read control line**

CD4061A OPERATIONAL MODES

OPERATION	ADDRESS LINES	$\overline{\text{CHIP-SELECT}}$	READ/WRITE	DATA IN	DATA OUTPUTS
Write "0"	Stable	0	1	0	High-Impedance
Write "1"	Stable	0	1	1	High-Impedance
Read	Stable	0	0	X	Valid 1 or 0
*Read Modify Write	Stable	0	0/1	X	Valid 1 or 0/High-Impedance
Address Change	Changing	1	X	X	High-Impedance

X = Don't Care

*For a READ MODIFY WRITE operation, $\overline{\text{CHIP SELECT}}$ may be held to logic 0 for the whole operation.

DYNAMIC ELECTRICAL CHARACTERISTICS

at $T_A = 25°C$, $V_{SS} = 0$ V, $C_L = 50$ pF, and t_r, $t_f = 20$ ns

CHARACTERISTIC		TEST CONDITIONS V_{DD} (V)	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
READ CYCLE TIME						
Read Cycle	t_{RC}	5	1200	1000	–	ns
		10	550	450	–	
Address Setup	t_{ADS}	5	40	0	–	ns
		10	0	–	–	
$\overline{\text{Chip Select}}$	$t_{\overline{CS}}$	5	700	500	–	ns
		10	350	250	–	
Address Hold	t_{ADH}	5	460	–	–	ns
		10	200	–	–	
Read Access	t_{RA}	5	–	450	750	ns
		10	–	250	380	
Data Out Hold	t_{DOH}	5	110	170	230	ns
		10	130	160	190	
Data Out Active	t_{DOA}	5	80	120	160	ns
		10	40	70	100	
Output Transition	t_{TLH}	5	–	60	100	ns
		10	–	50	75	
	t_{THL}	5	–	35	60	
		10	–	25	40	
Chip-Select Input Rise and Fall Time,	t_{rCE}	5	–	–	15	μs
	t_{fCE}	10	–	–	5	
		15	–	–	1	
WRITE CYCLE TIME						
Write Cycle	t_{WC}	5	1200	1000	–	ns
		10	550	450	–	
Address Setup	t_{ADS}	5	40	0	–	
		10	0	–	–	
$\overline{\text{Chip Select}}$	$t_{\overline{CS}}$	5	700	500	–	
		10	350	250	–	
Address Hold	t_{ADH}	5	460	–	–	
		10	200	–	–	
Write Hold	t_{WRH}	5	150	100	–	
		10	100	70	–	
Write	t_{WRW}	5	150	100	–	
		10	100	70	–	
Data-In Setup	t_{DIS}	5	140	80	–	
		10	80	35	–	
Data-In Hold	t_{DIH}	5	25	10	–	
		10	20	10	–	

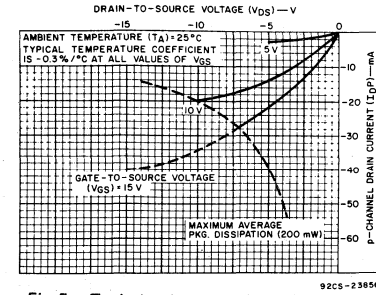


Fig. 5 – Typical p-channel drain characteristics.

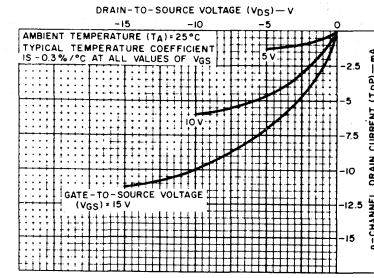


Fig. 6 – Minimum p-channel drain characteristics.

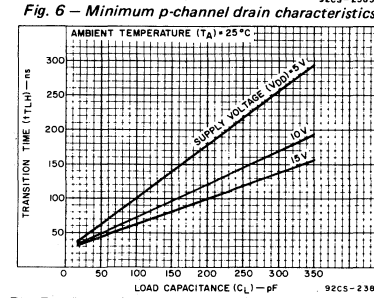


Fig. 7 – Typical low-to-high transition time (t_{TLH}) vs. C_L.

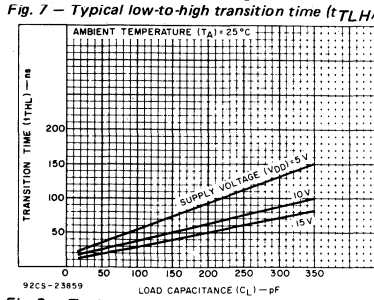


Fig. 8 – Typical high-to-low transition time (t_{THL}) vs. C_L.

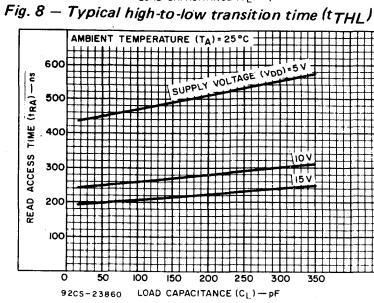


Fig. 9 – Typical read access time (t_{RA}) vs. C_L.

CD4061A Types

STATIC ELECTRICAL CHARACTERISTICS

(All inputs . . . $V_{SS} \leq V_I \leq V_{DD}$)

(Recommended DC Supply Voltage ($V_{DD}-V_{SS}$) . . . 3 to 15 V)

CHARACTERISTIC	TEST CONDITIONS V_O (V)	TEST CONDITIONS V_{DD} (V)	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 125°C MIN.	LIMITS 125°C MAX.	UNIT
Quiescent Device Current, I_L *See Fig. 14*		5	–	5	–	0.12	5	–	150	μA
		10	–	10	–	0.25	10	–	300	
Quiescent Device Dissipation/Package, P_D		5	–	–	–	0.6	25	–	750	μW
		10	–	–	–	2.5	100	–	3000	
Output Voltage Low-Level, V_{OL}		5	–	0.01	–	0	0.01	–	0.05	V
		10	–	0.01	–	0	0.01	–	0.05	
High-Level, V_{OH}		5	4.99	–	4.99	5	–	4.95	–	
		10	9.99	–	9.99	10	–	9.95	–	
Noise Immunity, (All Inputs) *See Fig. 17* V_{NL}	0.8	5	1.5	–	1.5	2.25	–	1.4	–	V
	1	10	3	–	3	4.5	–	2.9	–	
V_{NH}	4.2	5	1.4	–	1.5	2.25	–	1.5	–	
	9	10	2.9	–	3	4.5	–	3	–	
Output Drive Current: (Data Out, $\overline{\text{Data Out}}$) N-Channel (Sink), I_DN *See Figs. 3, 4, 12*	0.4	4.5	2	–	1.6	2.5	–	1.1	–	mA
	0.5	10	4.3	–	3.5	5	–	2.4	–	
P-Channel (Source), I_DP *See Figs. 5, 6, 13*	2.5	5	−1.1	–	−0.9	−1.8	–	−0.65	–	
	4.6	5	−0.5	–	−0.4	−0.8	–	−0.3	–	
	9.5	10	−1.1	–	−0.9	−1.8	–	−0.65	–	
Output Off Resistance (High-Impedance State), R_O (Off)		5	10	–	10	–	–	10	–	MΩ
		10	10	–	10	–	–	10	–	

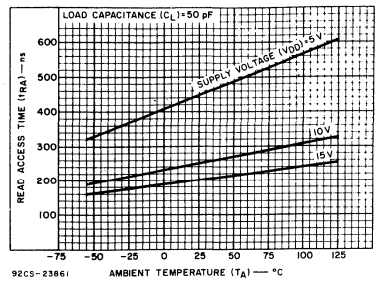


Fig. 10 – Typical read access time (t_{RA}) vs. temperature.

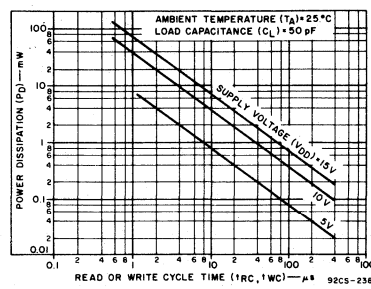
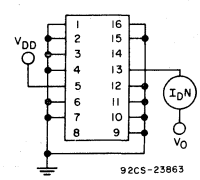


Fig. 11 – Typical power dissipation vs. cycle time.



Note: At address "0", "0" stored in memory.

Fig. 12 – N-channel drive current.

Note: At address 0, "1" stored in memory.

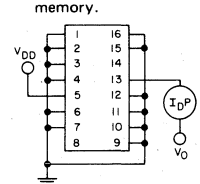


Fig. 13 – P-channel drive current.

Note for Fig. 12 and Fig. 13:
Power dissipation measured using random data pattern. Input pulse delays and widths set to minimum values specified on data sheet with the exception of cycle time, 15 V setups identical to 10 V data sheet values, with the exception of t_{CE} = 400 ns.

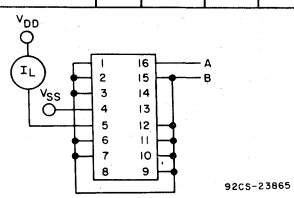


Fig. 14 – Quiescent device current.

Quiescent Device Current Test Conditions

Test	A	B	Memory Cells
1	0	0	All 0
2	1	1	All 0
3	0	1	All 0
4	0	0	All 1
5	1	1	All 1
6	0	1	All 1

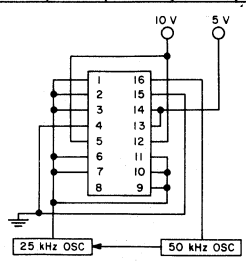
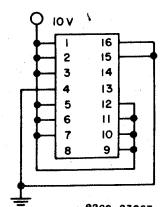


Fig. 15 – Operating life.



Description of Test:

Functional test run with random data input. All inputs toggle between 30% and 70% of V_{DD}.

Fig. 16 – Bias life.

Note: Connection to all terminals in Figs. 15 & 16 (except 4 and 5) are made through 47 kΩ resistors.

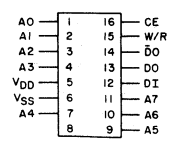


Fig. 17 – Noise immunity.

COS/MOS 200-Stage Dynamic Shift Register

MAXIMUM RATINGS, Absolute-Maximum Values:

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . -65 to +150° C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES K, T, H . . . . . -55 to +125° C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal): . . . . . -0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D)

FOR T_A = -55 to +100° C (PACKAGE TYPES K, T) . . . . . 500 mW

FOR T_A = +100 to +125° C (PACKAGE TYPES K, T) . . Derate Linearly at 12 mW/° C to 200 mW

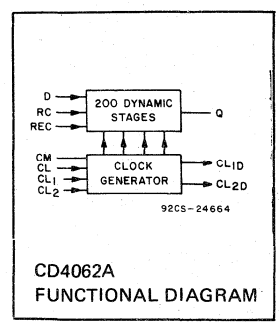
DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . -0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265° C



CD4062A
FUNCTIONAL DIAGRAM

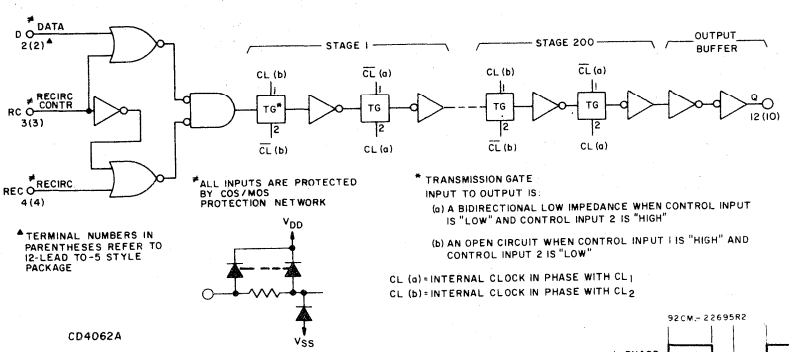


Fig. 1 – CD4062A logic block diagram.

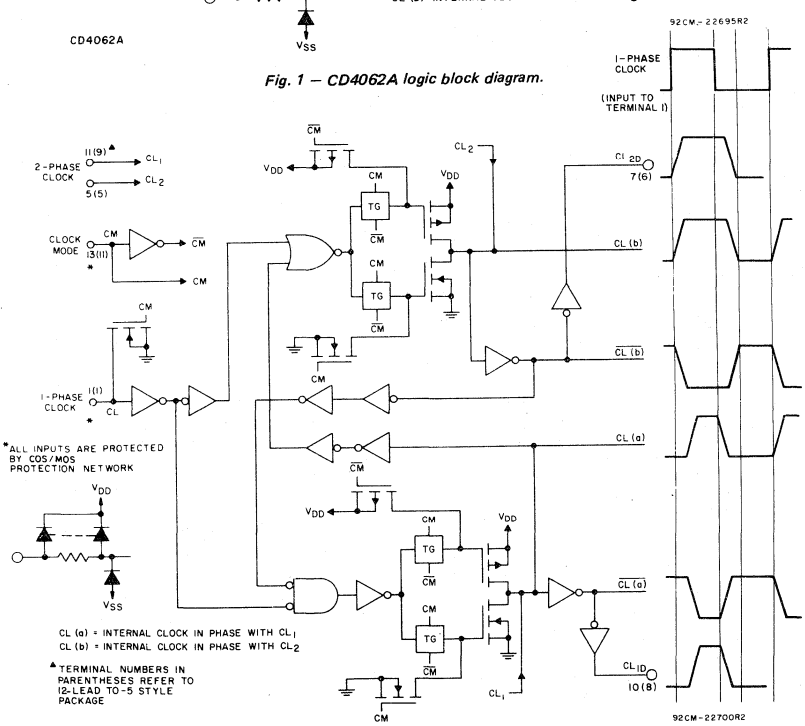


Fig. 2 – Clock circuit logic diagram.

The RCA-CD4062A is a 200-stage dynamic shift register with provision for either single- or two-phase clock input signals. Single-phase-clocked operation is intended for low-power, low clock-line capacitance requirements. Single-phase clocking is specified for medium-speed operation (< 1 MHz) at supply voltages up to 10 volts. Clock input capacitance is extremely low (< 5 pF), and clock rise and fall times are non-critical. The clock-mode signal (CM) must be low for single-phase operation.

Two-phase clock-input signals may be used for high-speed operation (up to 5 MHz) or to further reduce clock rise and fall time requirements at low speeds. Two-phase operation is specified for supply voltages up to 15 volts. Clock input capacitance is only 50 pF/phase. The clock-mode signal (CM) must be high for two-phase operation. The single-phase-clock input has an internal pull-down device which is activated when CM is high and may be left unconnected in two-phase operation.

The logic level present at the data input is transferred into the first stage and shifted one stage at each positive-going clock transition for single-phase operation, and at the positive-going transition of CL_1 for two-phase operation.

The CD4062A-Series types are supplied in 16-lead flat packages (K suffix), 12-lead hermetic TO-5 packages (T suffix), and in chip form (H suffix).

Features:

- **Minimum shift rates over full temperature range—**

  Single-phase clock: 3 V ≤ V_{DD} ≤ 10 V; f_{min} = 10 kHz; -55° C ≤ T_A ≤ +125° C (f_{min} = 1 kHz up to T_A ≤ 75° C)

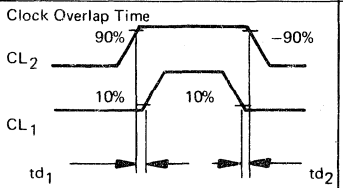
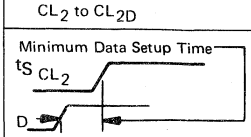
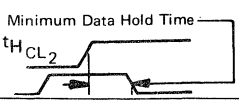
  Two-phase clock: 3 V ≤ V_{DD} ≤ 15 V; f_{min} = 10 kHz; -55° C ≤ T_A ≤ +125° C (f_{min} = 1 kHz up to T_A ≤ 75° C)

RECOMMENDED OPERATING CONDITIONS at T_A = 25° C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range):				
Single-Phase Clock		3	10	V
Two-Phase Clock		3	12	
Clock Input Frequency, f_{CL}*	5	0.15	500	kHz
	10	0.15	1000	
Clock Pulse Width, t_W*	5	250	66.7 X 10^6	ns
	10	500	66.7 X 10^6	
Clock Rise or Fall Times, t_rCL or t_fCL*	5	–	10	μs
	10	–	1	
Data Hold Time, t_H*	5	150	–	ns
	10	50	–	

* For single-phase clock, 50% duty cycle

Two-Phase Clock Operation (CL_1, CL_2); Clock Mode (CM) = High; 3 V ≤ V_{DD} ≤ 15 V. See Figure 4.

CHARACTERISTIC	TEST CONDITIONS V_{DD} V	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Maximum Clock Input Frequency, f_{CL}	5	1.25	2.5	–	MHz
	10	2.5	5	–	
Minimum Clock Input Frequency, f_{CL}	5	150	10	–	Hz
	10	150	10	–	
Clock Overlap Time 		40	–	–	ns
Average Input Capacitance, C_I CL_1, CL_2		–	50	–	pF
Propagation Delays; t_{PHL}, t_{PLH} CL_1 to Q	5	–	250	500	ns
	10	–	100	200	
CL_1 to CL_{1D} CL_2 to CL_{2D}	5	–	250	500	
	10	–	100	200	
Minimum Data Setup Time 	5	–	150	300	ns
	10	–	50	100	
Minimum Data Hold Time 	5	–	–	0	ns
	10	–	–	0	
Clock Rise and Fall Times t_rCL_1, CL_2 t_fCL_1, CL_2		No Restrictions If Clock Overlap Requirement Is Met			

Features (Cont'd):

- **Low power dissipation 0.3 mW/bit at 1 MHz and 10 V 0.04 mW/bit at 0.5 MHz and 5V (alternating 1-0 data pattern)**
- **Data output TTL-DTL compatible**
- **Recirculating capability**
- **Delayed two-phase clock outputs available for cascading registers**
- **Asynchronous ripple-type presettable to all 1's or 0's**
- **Ultra-low-power-dissipation standby operation**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Serial shift registers**
- **Time-delay circuits**
- **CRT refresh memory**
- **Long serial memory**

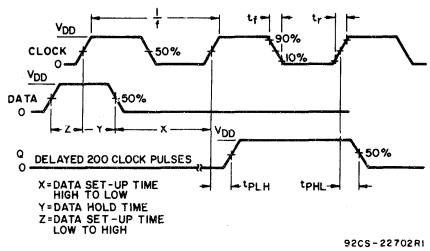


Fig. 3 – Timing diagram–single-phase clock.

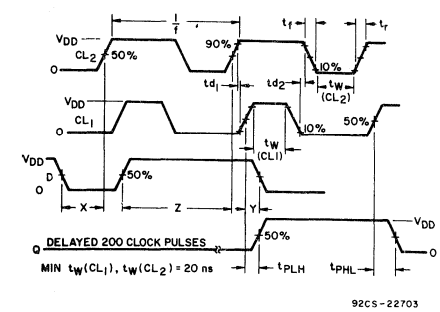


Fig. 4 – Timing diagram–two-phase clock.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS		CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) -55	+25 TYP.	+25 LIMIT	+125	UNITS
Quiescent Device Current, I_L Max.		–	–	5	12	0.5	12	720	μA
		–	–	10	25	1	25	1500	
CM=High, CL_1=High, CL_2=Low		–	–	15	50	1	50	2000	
Output Voltage: Low Level, V_{OL}		–	5	5	0 Typ.; 0.05 Max				V
		–	10	10	0 Typ.; 0.05 Max				
High Level V_{OH}		–	0	5	4.95 Min.; 5 Typ.				
		–	0	10	9.95 Min.; 10 Typ.				
Noise Immunity: Inputs Low, V_{NL}		4.2	–	5	1.5 Min.; 2.25 Typ.				V
		9	–	10	3 Min.; 4.5 Typ.				
Inputs High V_{NH}		0.8	–	5	1.5 Min.; 2.25 Typ.				
		1	–	10	3 Min.; 4.5 Typ.				
Noise Margin: Inputs Low, V_{NML}		4.5	–	5	1 Min.				V
		9	–	10	1 Min.				
Inputs High, V_{NMH}		0.5	–	5	1 Min.				
		1	–	10	1 Min.				
Output Drive Current: N-Channel (Sink), I_DN Min.	Q	0.4	–	4.5	1.6	2.6	1.3	0.91	mA
	Output	0.5	–	10	5	8*	4	3.2	
	CL_{1D},	0.5	–	5	0.87	1.4	0.7	0.49	
	CL_{2D}	0.5	–	10	2.2	3.6	1.8	1.26	
P-Channel (Source):		4.5	–	5	-0.31	-0.5	-0.25	-0.17	mA
I_DP Min.	Q	2.5	–	5	-0.93	-1.5	-0.75	-0.52	
	Output	9.5	–	10	-0.87	-1.4	-0.7	-0.49	
	CL_{1D},	4.5	–	5	-0.43	-0.7	-0.35	-0.24	
	CL_{2D}	9.5	–	10	-1.1	-1.8	-0.9	-0.63	
Input Leakage Current,		Any Input							μA
I_{IL}, I_{IH}		–	–	15	$\pm 10^{-5}$ Typ., ±1 Max.				

* Maximum power dissipation rating ⩽ 200 mW.

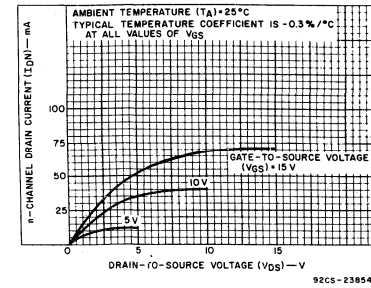


Fig. 5— Typical n-channel drain characterstics for Q output.

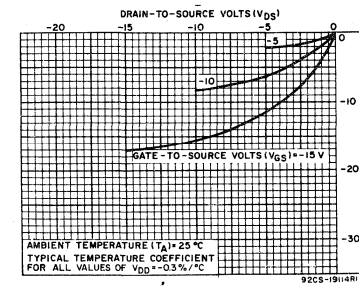


Fig. 6— Typical p-channel drain characteristics for Q output.

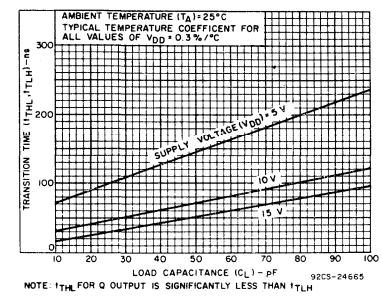


Fig. 7— Typical transition time vs. C_L for data outputs.

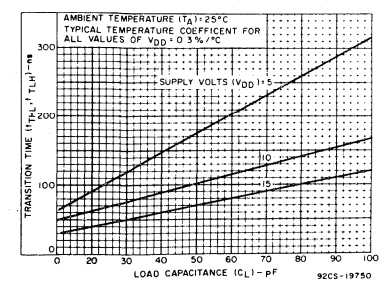
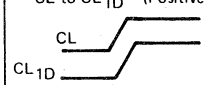
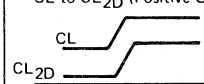
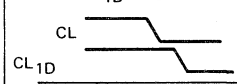
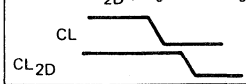
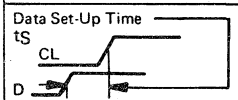
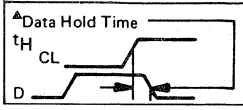


Fig. 8— Typical transition time vs. C_L for delayed clock output.

CD4062A Types

DYNAMIC CHARACTERISTICS AT T_A = 25° C, V_{SS} = 0 V, C_L = 50 pF, Input t_r, t_f = 20 ns, except t_rCL and t_fCL

Single-Phase-Clock Operation; Clock Mode (CM) = Low; 3 V ≤ V_{DD} ≤ 10 V (See Figure 3)

CHARACTERISTIC	TEST CONDITIONS	V_{DD} V	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Maximum Clock Input Frequency, f_{CL} (50% Duty Cycle)	t_r, t_f=20 ns	5	0.5	1	–	MHz
		10	1	2	–	
Minimum Clock Input Frequency, f_{CL} (50% Duty Cycle)		5	150	10	–	Hz
		10	150	10	–	
Clock Rise and Fall Times** t_rCL, t_fCL		5	–	–	10	μs
		10	–	–	1	
Average Input Capacitance, C_I	All Inputs Except CL_1 and CL_2		–	5	–	pF
Propagation Delays: CL to Q		5	–	1000	2000	ns
		10	–	400	800	
CL to CL_{1D} (Positive Going) 	(50% Points)	5	–	750	1500	ns
		10	–	300	600	
CL to CL_{2D} (Positive Going) 	(50% Points)	5	–	500	1000	
		10	–	200	400	
CL to CL_{1D} (Negative Going) 	(50% Points)	5	–	450	900	
		10	–	175	350	
CL to CL_{2D} (Negative Going) 	(50% Points)	5	–	750	1500	
		10	–	300	600	
Transition Time: t_{TLH}, t_{THL} Q Output		5	–	100	200	ns
		10	–	50	100	
CL_{1D}, CL_{2D}		5	–	200	400	
		10	–	100	200	
Data Set-Up Time t_S 		5	–	–	0	ns
		10	–	–	0	
▲Data Hold Time t_H 		5	–	–	150	ns
		10	–	–	150	

** If more than one unit is cascaded in single-phase parallel clocked application, t_rCL should be made less than or equal to the sum of the propagation delay at 15 pf, and the transition time of the output driving stage. (See Figs. 5 and 7 for cascading options.)

▲ Use of delayed clock permits high-speed logic to precede CD4062A register (see cascade register operation).

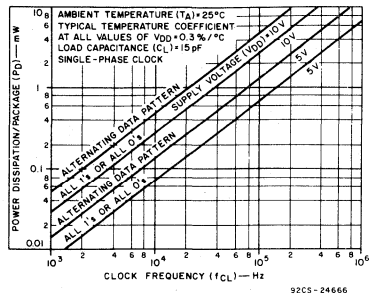


Fig. 9— Typical power dissipation vs. frequency.

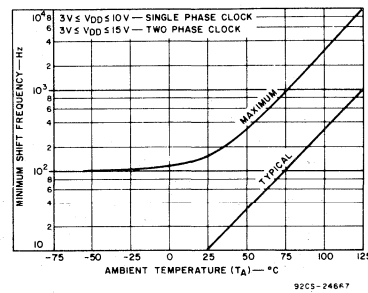


Fig. 10— Minimum shift frequency vs. ambient temperature.

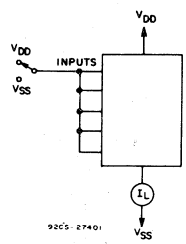


Fig. 11— Quiescent-device-current test circuit.

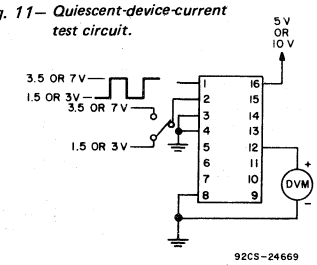


Fig. 12— Noise-immunity test circuit.

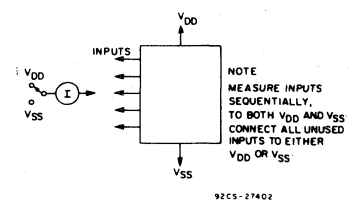


Fig. 13—Input-leakage-current test circuit.

COS/MOS Quad Bilateral Switch

For Transmission or Multiplexing of Analog or Digital Signals

RCA CD4066A is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with RCA-CD4016, but exhibits a much lower ON resistance. In addition, the ON resistance is relatively constant over the full input-signal range.

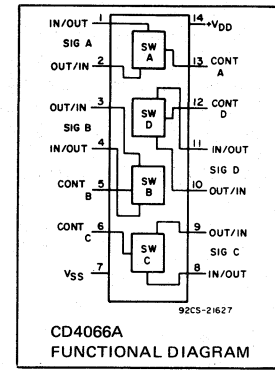
The CD4066A consists of four independent bilateral switches. A single control signal is required per switch. Both the p and the n device in a given switch are biased ON or OFF simultaneously by the control signal. As shown in Fig. 1, the well of the n-channel device on each switch is either tied to the input when the switch is ON or to V_{SS} when the switch is OFF. This configuration eliminates the variation of the switch-transistor threshold voltage with input signal, and thus keeps the ON resistance low over the full operating-signal range.

The advantages over single-channel switches include peak input-signal voltage swings equal to the full supply voltage, and more constant ON impedance over the input-signal range. For sample-and-hold applications, however, the CD4016 is recommended.

These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- **15-V digital or ± 7.5-V peak-to-peak switching**
- **80Ω typical ON resistance for 15-V operation**
- **Switch ON resistance matched to within 5 Ω over 15-V signal-input range**
- **ON resistance flat over full peak-to-peak signal range**
- **High ON/OFF output-voltage ratio: 65 dB typ. @ f_{is} = 10 kHz, R_L = 10 kΩ**
- **High degree of linearity: < 0.5% distortion typ. @ f_{is} = 1 kHz, V_{is} = 5 V_{p-p}, $V_{DD}-V_{SS} \geq$ 10 V, R_L = 10 kΩ**
- **Extremely low OFF switch leakage resulting in very low offset current and high effective OFF resistance: 10 pA typ. @ $V_{DD}-V_{SS}$ = 10 V, T_A = 25°C**
- **Extremely high control input impedance (control circuit isolated from signal circuit): 10^{12} Ω typ.**
- **Low crosstalk between switches: -50 dB typ. @ f_{is} = 0.9 MHz, R_L = 1 kΩ**
- **Matched control-input to signal-output capacitance: Reduces output signal transients**
- **Frequency response, switch ON = 40 MHz (typ.)**
- **Quiescent current specified to 15-V**
- **Maximum control input leakage current of 1-μA at 15-V (Full package-temperature range)**



CD4066A
FUNCTIONAL DIAGRAM

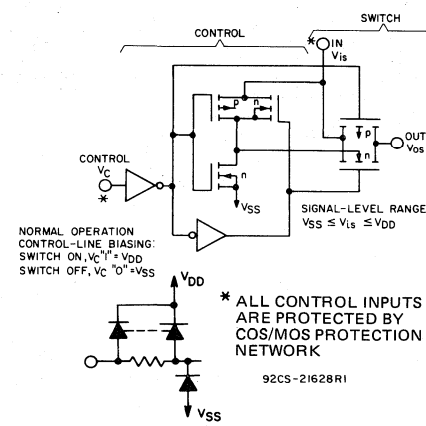


Fig. 1 – Schematic diagram of 1 of 4 identical switches and its associated control circuitry.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . -65 to +125°C

OPERATING TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H. . . . . -55 to +125°C

PACKAGE TYPE E . . . . . -40 to +85°C

DC SUPPLY VOLTAGE RANGE, V_{DD}

(Voltages referenced to V_{SS}) . . . . . -0.5 to +15 V

POWER DISSIPATION PER PACKAGE:

FOR T_A = -40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPE E) Derate Linearly at 12 mW/°C . . . . . 200 mW

FOR T_A = -55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) Derate Linearly at 12 mW/°C . . . 200 mW

DEVICE DISSIPATION PER SECTION:

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW

ALL SIGNAL AND DIGITAL CONTROL INPUTS . . . . . $V_{SS} \leq V_I \leq V_{DD}$

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

SPECIAL CONSIDERATIONS – CD4066A

1. In applications where separate power sources are used to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load of the 4 CD4066A bilateral switches). This provision avoids any permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from CD4066A.
2. In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 4, 8, or 11, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R_{ON} values shown).

   No V_{DD} current will flow through R_L if the switch current flows into terminals 2, 3, 9, or 10.
3. Minimum bilateral switch output load resistance is 100 Ω.

OPERATING CONDITIONS AT T_A = 25°C

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	V_{DD}	MIN.	MAX.	UNITS
Supply Voltage Range (T_A = Full Package Temperature Range)	–	3	12	V

CD4066A Types

Applications:

- **Analog signal switching/multiplexing**
  - **Signal gating** — **Modulator**
  - **Squelch control** — **Demodulator**
  - **Chopper** — **Commutating switch**
- **Digital signal switching/Multiplexing**
- **Transmission-gate logic implementation**
- **Analog-to-digital & digital-to-analog conversion**
- **Digital control of frequency, impedance, phase, and analog-signal gain**

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS *All Voltage Values Are in Volts*			LIMITS Values at −55°C, +25°C, +125°C Apply to D, F, K, H Packages Values at −40°C, +25°C, +85°C Apply to E Package						UNITS
			V_{DD} (V)	−55°	−40°	+85°	+125°	+25° TYP.	+25° MAX.	
Quiescent Device Current, I_L max. D, F, K, H Pkgs.			5	0.25	–	–	7.5	0.01	0.25	μA
			10	0.5	–	–	15	0.01	0.5	
			15	2	–	–	40	0.02	2	
E Pkg.			5	–	2.5	15	–	0.25	2.5	μA
			10	–	5	30	–	0.25	5	
			15	–	50	500	–	0.5	50	
SIGNAL INPUTS (V_{is}) AND OUTPUTS (V_{os})										
ON Resistance, R_{ON} Max.	$V_C = V_{DD}$	V_{SS}	V_{is}							Ω
	$R_L = 10k\Omega$*									
	+7.5	−7.5	−7.5 to +7.5	220	250	300	320	80	280	
	+15	0	0 to +15							
	+5	−5	−5 to +5	400	450	520	550	120	500	
	+10	0	0 to +10							
	+2.5	−2.5	−2.5 to +2.5	3000	3500	5200	5500	270	5000	
	−5	0	0 to +5							
Δ ON Resistance Between Any 2 of 4 Switches, ΔR_{ON}	$R_L = 10k\Omega$*									Ω
	+7.5 or +15	−7.5 or 0	+7.5 to −7.5 / +15 to 0	–	–	–	–	5	–	
	+5 or +10	−5 or 0	+5 to −5 / +10 to 0	–	–	–	–	10	–	
Sine Wave Response (Distortion)	+5	−5	5V p-p▲	–	–	–	–	0.4	–	%
	$R_L = 10k\Omega$, $f_{is} = 1kHz$									
Frequency Response Switch ON (Sine-Wave Input)	+5	−5	−5 p-p	–	–	–	–	40	–	MHz
	$R_L = 1k\Omega$, $20 \log_{10} \frac{V_{os}}{V_{is}} = -3dB$									
Feedthrough-Switch OFF	+5	−5	−5 p-p	–	–	–	–	1.25	–	MHz
	$R_L = 1k\Omega$, $20 \log_{10} \frac{V_{os}}{V_{is}} = -50dB$									
Input or Output Leakage — Switch OFF (Effective OFF Resistance)	V_{DD}	$V_C = V_{SS}$								nA
	+7.5	−7.5	±7.5	–	–	–	–	±0.1	±100*	
	+5	−5	±5	–	–	–	–	±0.1	±100*	
Crosstalk Between Any 2 of the 4 Switches (f at −50 dB)	$V_C(A) = V_{DD} = +5$, $V_C(B) = V_{SS} = -5$, $R_L = 1k\Omega$		(A) 5V p-p	–	–	–	–	0.9	–	MHz
	$20 \log_{10} \frac{V_{os}(B)}{V_{is}(A)} = -50dB$									

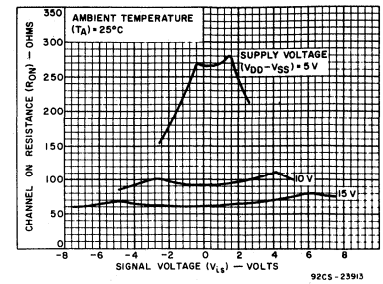


Fig. 2 (a) — Typical channel ON resistance vs. signal voltage for three values of supply voltage ($V_{DD}-V_{SS}$).

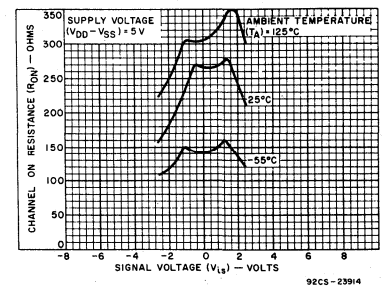


Fig. 2 (b) — Typical channel ON resistance vs. signal voltage with supply voltage ($V_{DD}-V_{SS}$) = 5 V.

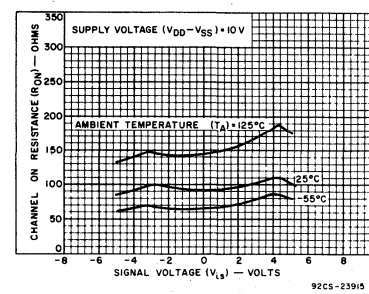


Fig. 2 (c) — Typical channel ON resistance vs. signal voltage with supply voltage ($V_{DD}-V_{SS}$) = 10 V.

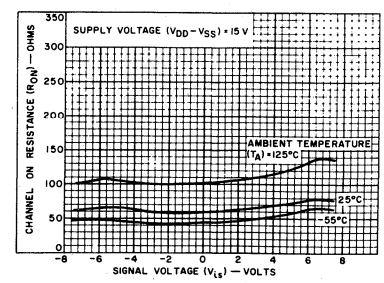


Fig. 2 (d) — Typical channel ON resistance vs. signal voltage with supply voltage ($V_{DD}-V_{SS}$) = 15 V.

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	TEST CONDITIONS *All Voltage Values Are in Volts*		LIMITS Values at -55°C, +25°C, +125°C Apply to D, F, K, H Packages; Values at -40°C, +25°C, +85°C Apply to E Package						UNITS
		V_{DD} (V)	-55°	-40°	+85°	+125°	+25° TYP.	+25° MAX.	
Propagation Delay (Signal Input to Signal Output) t_{pd}	V_{DD} = 5	$V_C = V_{DD}$, V_{SS} = GND, C_L = 15pF, V_{is} = sq. wave, t_r, t_f = 20 ns (Input Signal)	–	–	–	–	20	50	ns
	V_{DD} = 10		–	–	–	–	10	25	
Capacitance: Input, C_{is}	V_{DD} = +5, $V_{CC} = V_{SS}$ = -5		–	–	–	–	8	–	pF
Output, C_{os}			–	–	–	–	8	–	
Feedthrough, C_{ios}			–	–	–	–	0.5	–	
CONTROL (V_C)									
Noise Immunity, V_{NL} Min.	$V_{is} \leq V_{DD}$, I_{is} = 10μA, $V_{DD} - V_{SS}$ = 10		2	2	2	2	2 min 4.5	–	V
Input Leakage Current, I_{IL} Max.	$V_{is} \leq V_{DD}$, $V_{DD} - V_{SS}$ = 15, $V_C \leq V_{DD} - V_{SS}$		±1				$\pm 10^{-6}$	±1	μA
Crosstalk Control Input to Signal Output	$V_{DD}-V_{SS}$ = 10, V_C = 10 (sq. wave), $t_{rc} = t_{fc}$ = 20 ns	R_L = 10kΩ	–	–	–	–	50	–	mV
Propagation Delay, t_{pdC}		R_L=300kΩ, $V_{is} \leq 10$, C_L = 15pF	–	–	–	–	35	–	ns
Maximum Allowable Control Input Repetition Rate	V_{DD}=10, V_{SS}=GND, R_L=1kΩ, C_L=15pF, V_C = 10 (sq. wave), t_r, t_f = 20 ns		–	–	–	–	10	–	MHz
Av. Input Capacitance, C_I			–	–	–	–	5	–	pF

* Limit determined by minimum feasible leakage measurement for automatic testing.

Δ Symmetrical about 0 volts. • For all test conditions.

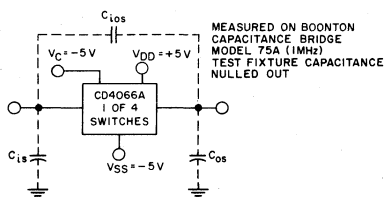


Fig. 6 – Capacitance test circuit.

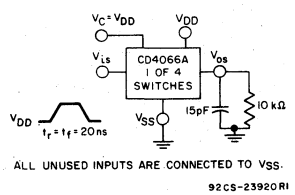


Fig. 8 – Propagation delay time signal input (V_{is}) to signal output (V_{os}).

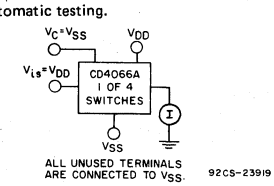


Fig. 7 – OFF switch input or output leakage.

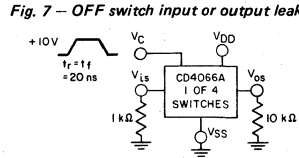


Fig. 9 – Crosstalk-control input to signal output.

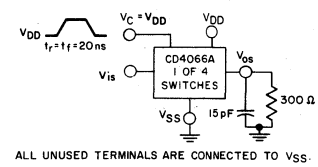


Fig. 11 – Propagation delay t_{PLH}, t_{PHL} control-signal output.

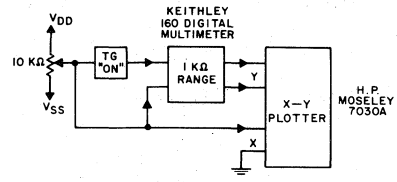


Fig. 3 – Channel ON resistance measurement circuit.

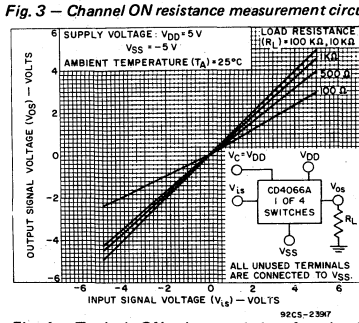


Fig. 4 – Typical ON characteristics for 1 of 4 channels.

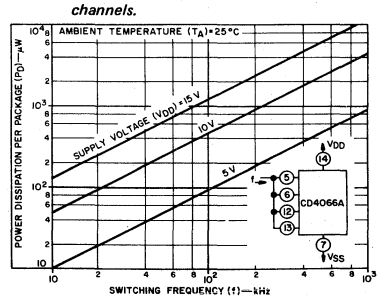


Fig. 5 – Power dissipation per package vs. switching frequency.

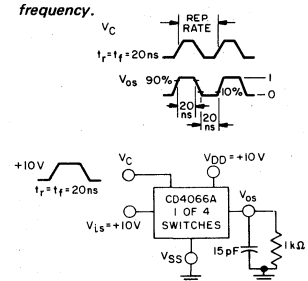


Fig. 10 – Maximum allowable control input repetition rate.

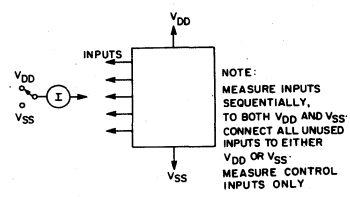


Fig. 12 – Input leakage current test circuit.

CD40061, CD40061A Types

Preliminary Data

COS/MOS 256-Word by 1-Bit Static Random-Access Memory

The RCA-CD40061 and CD40061A are 256-word by 1-bit COS/MOS fully static random access memories. They are similar in terminal arrangement and function to the CD4061A, except that the requirement for the Chip-Select input to return to a high level between address changes in eliminated.

The CD40061AD and CD40061AE have maximum supply voltage ratings of 15 V; the CD40061E maximum rating is 7 V. These devices are fully decoded and utilize eight Address inputs (A_0-A_7) to select one of the 256 storage locations. Additional connections are provided for an active Low Chip-Select ($\overline{CS}$), a $\overline{Read}$/Write command ($\overline{R}/W$), a Data input (DATA IN), an active High 3-State Output (DATA OUT), and an active Low 3-State Output ($\overline{DATA}$ OUT). DATA OUT is the same voltage state as DATA IN.

The Chip-Select input must be low to enable the Read or Write operations. A high level both inhibits these functions and causes the outputs to exhibit a high impedance. Output voltage levels appear at the output only when both CS and $\overline{R}/W$ inputs are at low levels. These outputs interface directly with TTL devices.

Both the CD40061 and CD40061A are supplied in 16-lead dual-in-line plastic packages (E suffix) or in chip form (H suffix). The CD40061A is also supplied in a hermetically sealed 16-lead dual-in-line ceramic side-brazed package (D suffix).

Features:

- **Organization — 256-words by 1-bit**
- **COS/MOS compatible inputs and outputs**
- **Low power dissipation (typ.) @ 300 nS cycle time:**
  10 nW/Bit standby @ V_{DD} = 5 V
  0.1 mW/Bit operating @ V_{DD} = 5 V
  40 nW/Bit standby @ V_{DD} = 10 V
  0.4 mW/Bit operating @ V_{DD} = 10 V
- **Access time (typ.):**
  150 nS @ V_{DD} = 10 V; 300 nS @ V_{DD} = 5 V
- **Noise immunity (typ.): 45% of V_{DD}**
- **TTL output drive capability**
- **3-State complementary data outputs**
- **Separate data-in and data-out lines**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE ..... −65 to +150°C
OPERATING-TEMPERATURE RANGE:
  CERAMIC-PACKAGE TYPES ..... −55 to +125°C
  PLASTIC-PACKAGE TYPES ..... −40 to +85°C
SUPPLY VOLTAGE RANGE (V_{DD}−V_{SS}):
  CD40061E ..... 7 to −0.5 V
  CD40061AD, CD40061AE ..... 15 to −0.5 V
INPUT VOLTAGE RANGE (V_I−V_{SS}) ..... V_{DD} to −0.5 V
DEVICE DISSIPATION (per package) ..... 200 mW
RECOMMENDED DC SUPPLY VOLTAGE RANGE (V_{DD}−V_{SS}):
  CD40061E ..... 3 to 6 V
  CD40061AD, CD40061AE ..... 3 to 12 V
RECOMMENDED INPUT VOLTAGE SWING ..... V_{DD} to V_{SS}
LEAD TEMPERATURE (During soldering):
  At distance 1/16 ±1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... 265°C

CD40061 and CD40061A OPERATIONAL MODES

MODE	$\overline{CHIP\text{-}SELECT}$	$\overline{READ/WRITE}$	DATA OUT	$\overline{DATA}$ OUT
Write	0	1	High Impedance	High Impedance
Read	0	0	Storage State	Complement of Storage State
Unselected	1	X	High Impedance	High Impedance

1 = High Level 0 = Low Level X = Don't Care

CAPACITANCES (V_I = 0, f = 1 MHz)

CHARACTERISTICS	Min.	Typ.	Max.	UNITS
Address Input, C_A	–	9	–	pF
Chip-Select, C_{CS}	–	9	–	pF
Read/Write Input, C_{WE}	–	5	–	pF
Data Input, C_{DI}	–	5	–	pF
Data Output, C_{DO}	–	10	–	pF

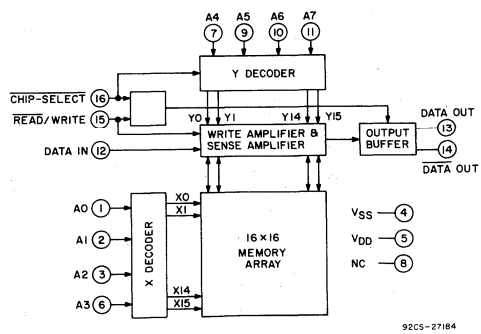


Fig. 1 — Functional block diagram for CD40061, and CD40061A.

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C

Values shown for V_{DD} = 5 V apply to all types; values shown for V_{DD} = 10 V apply to the CD40061AD and CD40061AE only.

CHARACTERISTIC	TEST CONDITIONS V_O(V)	TEST CONDITIONS V_{DD}(V)	TYPICAL VALUES	UNITS
Quiescent Device Current, I_L		5 10	0.5 1	μA
Output Voltage, Low Level, V_{OL}		5 10	0 0	V
Output Voltage, High Level, V_{OH}		5 10	5 10	V
Output Current, Low Level, I_{OL}	0.4 0.5	5 10	1.6 3.5	mA
Output Current, High Level, I_{OH}	2.5 4.5 9	5 5 10	−0.9 −0.4 −0.9	mA
Noise Immunity, All Inputs Low, V_{NL}	0.8 1	5 10	2.25 4.5	V
Noise Immunity, All Inputs High, V_{NH}	4.2 9	5 10	2.25 4.5	V
Output Resistance, Off State, R_O(off)		5 10	10 10	MΩ

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{DD} ±5%, Input t_r, t_f = 10 ns, and C_L = 50 pF, see Note 3.

READ CYCLE TIMES (For waveforms, see Figs. 2, 3 and 4)

CHARACTERISTIC		TEST CONDITIONS V_{DD} (V)	TYPICAL VALUES	UNITS
Chip-Select, (Note 1)	$t_{\overline{CS}}$	5 10	310 180	ns
Address Setup,	t_{ADS}	5 10	20 10	ns
Address Hold,	t_{ADH}	5 10	0 0	ns
Read Setup,	t_{RDS}	5 10	0 0	ns
Read Hold,	t_{RDH}	5 10	0 0	ns
Data Out Hold,	t_{DOH}	5 10	40 20	ns
Data Out Active,	t_{DOA}	5 10	20 15	ns
Read Cycle, (Note 2)	t_{RC}	5 10	350 200	ns
Access,	t_{ACC}	5 10	300 150	ns

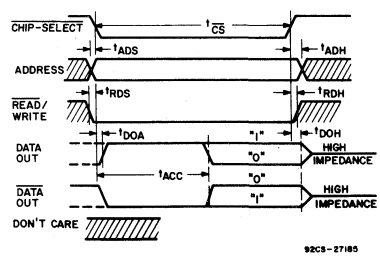


Fig. 2 – Read cycle waveforms for CD40061, CD40061A.

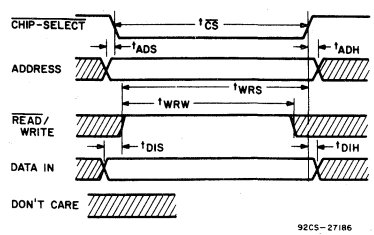


Fig. 3 – Write cycle waveforms for CD40061, CD40061A.

DYNAMIC ELECTRICAL CHARACTERISTICS (Cont'd)

WRITE CYCLE TIMES (For waveforms, see Figs. 2, 3 and 4)

CHARACTERISTIC		TEST CONDITIONS V_{DD} (V)	TYPICAL VALUES	UNITS
Chip-Select,	$t_{\overline{CS}}$	5 10	170 90	ns
Address Setup,	t_{ADS}	5 10	20 10	ns
Address Hold,	t_{ADH}	5 10	0 0	ns
Write Setup,	t_{WRS}	5 10	170 90	ns
Write Width,	t_{WRW}	5 10	170 90	ns
Data In Setup,	t_{DIS}	5 10	0 0	ns
Data In Hold,	t_{DIH}	5 10	20 10	ns
Write Cycle, (Note 2)	t_{WC}	5 10	200 110	ns

READ/MODIFY/WRITE TIMES (For waveforms, see Figs. 2, 3 and 4)

CHARACTERISTIC		TEST CONDITIONS V_{DD} (V)	TYPICAL VALUES	UNITS
Chip-Select, (Note 1)	$t_{\overline{CS}}$	5 10	480 270	ns
Address Setup,	t_{ADS}	5 10	20 10	ns
Address Hold,	t_{ADH}	5 10	0 0	ns
Read Setup,	t_{RDS}	5 10	0 0	ns
Data Out Active,	t_{DOA}	5 10	20 15	ns
Previous Data Hold,	t_{PDH}	5 10	40 20	ns
Access,	t_{ACC}	5 10	300 150	ns
Read Width Effective,	t_{RDW}	5 10	310 180	ns
Write Setup,	t_{WRS}	5 10	170 90	ns
Write Width	t_{WRW}	5 10	170 90	ns
Data In Setup,	t_{DIS}	5 10	0 0	ns
Data In Hold,	t_{DIH}	5 10	20 10	ns
Read/Modity/Write Cycle, (Note 2)	t_{RWC}	5 10	500 280	ns

Note 1 – The chip-select times specified provide an active output data time of 50 ns minimum.

Note 2 – Cycle time defines the shortest time in which this memory will correctly perform its desired function.

Note 3 – Address rise and fall times must be equal to or less than 1 μs under all conditions and for all modes.

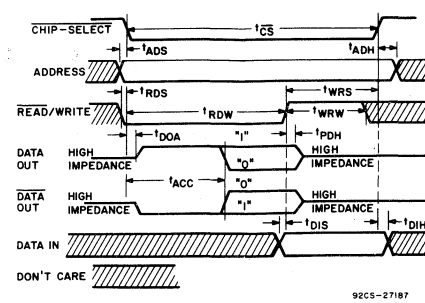


Fig. 4 – Read/modify/write cycle waveforms for CD40061, CD40061A.

COS/MOS Timekeeping and Special Products

Technical Data

CD22001H, CD22002H

COS/MOS 5-Function Liquid-Crystal Digital-Watch Circuit

The RCA-CD22001H* and CD22002H* are complementary MOS circuits containing all logic necessary for a digital-readout wristwatch that will display either hours and minutes, month and date, or seconds on a single 3-1/2-digit field-effect liquid-crystal display.

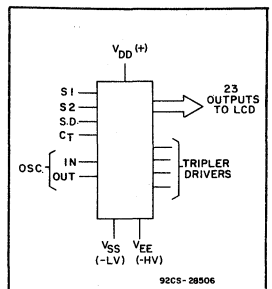
These devices contain an inverter-amplifier for a 32-kHz quartz crystal oscillator, a countdown chain, and counters for seconds, minutes, hours, date, and months. The display section contains seven-segment decoders plus level translators and drivers to provide high-voltage ac drive to each of the 23 segments. Access to the control section is provided by two inputs, S1 and S2. These inputs are normally activated by a push-button contact to the watch case (V_{DD}). Debounce circuitry for these inputs is provided on the chip.

The CD22001H and CD22022H are similar except that the CD22022H may be placed in the reset condition by activating S1 and S2 simultaneously.

* Formerly Developmental type Nos. TA6979AH and TA10179H, respectively.

Special Features:

- **3-1/2 digit display, 5-function watch: month, date, hours, minutes, and seconds**
- **Two timekeeping display modes**
- **Simple two-button operation**
- **Simple high-voltage converter on chip**
- **Single-cell operation**
- **Counter test input for high-speed testing**
- **Smart calendar**
- **Shutdown input for power conservation**
- **Automatic and manual reset (CD22002H)**



CD22001H, CD22002H Functional Diagram

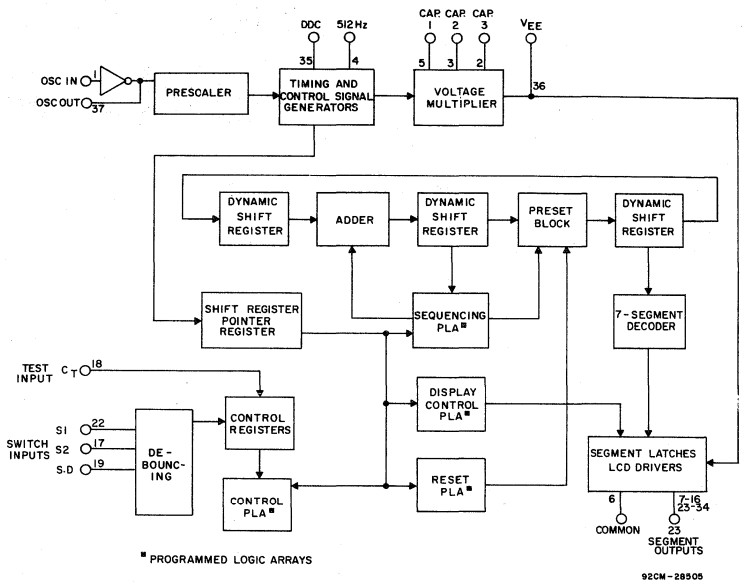
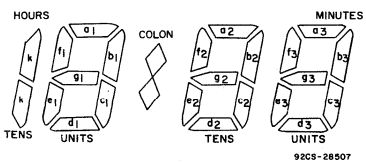


Fig.1 – Block diagram of the CD22001H or CD22002H.



	a	b	c	d	e	f	g
1		X	X				
2	X	X		X	X		X
3	X	X	X	X			X
4		X	X			X	X
5	X		X	X		X	X
6	X		X	X	X	X	X
7	X	X	X				
8	X	X	X	X	X	X	X
9	X	X	X	X		X	X
0	X	X	X	X	X	X	

X = Segment activated

Fig.2 – Segment designations and number to segment definition.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE RANGE (V_{DD}-V_{SS}), (V_{DD}-V_{EE})	−0.5 to +6 V
INPUT VOLTAGE RANGE, ALL INPUTS	$V_{SS} \leq V_I \leq V_{DD}$
DEVICE DISSIPATION	200 mW
OPERATING-TEMPERATURE RANGE	−10°C to +60°C
STORAGE-TEMPERATURE RANGE	−20°C to +70°C

Architecture

The operation and timekeeping of the CD22001H and CD22002H are controlled by an innovative dynamic circuit, as shown in Fig.1. The architecture of both chips is designed around a recirculating dynamic shift register. Timing information is circulated through the register at a very precise rate, as determined by the crystal oscillator. This information is read from the dynamic shift register and altered by a series of programmed logic arrays (PLA). At certain intervals during the dynamic shift register cycle, information is latched from the shift register and decoded into seven-segment information to be displayed on the LCD.

Watch Operation

The display and set functions are controlled by two switches, S1 and S2. The seven items which can be displayed are:

Functions	Example
1. time (hours and minutes)	12:00
2. date (month and day)	12 1
3. seconds	:01
4. set month	12
5. set day	1
6. set hour	12: A
7. set minute	:00

In general, the colon is used to distinguish time from date, and position (right or left of colon) is used to distinguish hours from

minutes and the month from the day. Seconds can be recognized because they change once per second and the colon remains on.

The first three items (time, date, and seconds) can be called up in either of two "RUN" modes. During operation in these modes, S1 is used to select either time, date, or seconds to appear on the display. The remaining items (4 through 7) are set modes. In these modes, S1 is used to advance the item being displayed. S2 is used to advance the watch to the desired RUN or SET mode as follows:

1. RUN I
2. RUN II
3. set month
4. set day
5. set hour
6. set minutes

Each momentary depression of S2 advances the watch to the next mode.

RUN I Mode

In RUN I mode, the watch normally displays hours and minutes with the colon flashing at 1 Hz. Depressing S1 will cause month and day to be displayed as long as the button is held. The display will return to hours-minutes 1-1/2 seconds after S1 is released. Seconds can be called up by depressing S1 once if date is displayed or twice if hours-minutes are displayed. Seconds will then continue to be displayed until S1 is again depressed and the display returns to hours-minutes.

RUN II Mode

In RUN II mode, the watch alternately displays hours-minutes, then month-day for 1-1/2 seconds each. Depressing S1 once calls up seconds. Depressing S1 again restores the alternating condition. Note that when seconds are displayed, RUN I and RUN II are indistinguishable. In either case, however, depressing S1 returns the watch to a distinguishable condition.

Additional Features

The day counter will count 28, 30, or 31 days depending on the month. February is considered a 28-day month, and therefore, the day must be set every four years on leap year. This is done by waiting until March 1 (the watch will read March 2), and then setting the correct day.

A leading zero in digit two is blanked when day is displayed but appears for minutes and seconds.

Setting the Watch

To set the watch, depress and release S2 until only the month appears on the display. The month appears on the left, the colon is off and the right side is blank. The month can be advanced at a 1-Hz rate by depressing and holding S1, or stepped one month at a time by momentarily depressing and releasing S1.

From this condition, one momentary depression of S2 causes the day to appear. The day is displayed on the right, the colon is off and the left side is blank. The day can be advanced in the same manner as for the month update.

The next momentary depression of S2 calls up the hour. The hour appears on the left, the colon is on and an A or P (AM or PM) will appear on the far right. The A or P changes when the hour is advanced through 12:, the total cycle being twenty-four (24) hours.

The next depression of S2 calls up minutes. If minutes are advanced using S1, the seconds are reset to zero and placed on hold. The minutes should be set ahead by approximately one minute, compared to standard time. After advancing to either RUN mode by depressing S2 once for RUN I or twice for RUN II, the hold is then released by depressing S1 to resume normal timekeeping. Using this method, the watch can be accurately set to within 1/4 second of the desired time.

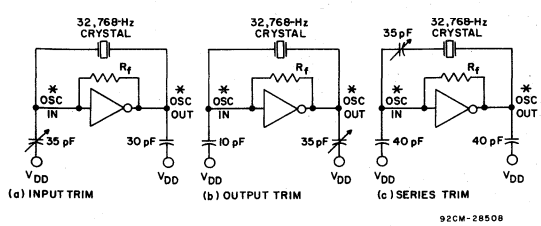
Display Drive

The ac drive for the liquid-crystal display is generated from the 32-Hz square wave in the countdown chain. The 32-Hz waveform, like all other logic signals on the chip, has an amplitude of 1.5 V. In order to drive a liquid-crystal display, the amplitude must be changed to higher voltages. Therefore, the 32-Hz square wave is passed through a level translator and driver circuit before it becomes the Common Output to the backplane of a display. The Common Output and its complement are routed to the other 22 output drivers. In response to low-level logic signals from the timekeeping section of the chip, the output drivers apply either the true Common Output or its complement to the segments of the display. Applying the true waveform maintains the segment in an off (unactivated) state, because the differential voltage between segment and backplane of the display is zero. Applying the complement waveform maintains the segment in an on (activated) state because the differential voltage between segment and backplane is twice the magnitude of V_{EE}. The nomenclature of the display segments is given in Figure 2. In order to prevent any potentially damaging dc voltage from appearing across the LCD, which might occur if the oscillator stops because of low battery voltage or if the watch is in the shutdown mode, a capacitor should be placed in series with the common backplane output. The capacitor value may typically be 0.02 μF. (See Figs. 4, 5, and 6).

Test Inputs

The CT "test" input may be used to speed up operation of the watch circuit to facilitate rapid testing. The actual function of the CT input is dependent upon the different states of the device.

1. During shutdown, the CT input becomes the input to the dynamic shift register which, in a static mode, allows testing of leakage current in two major states, all "1" or all "0".
2. In normal operation, if CT is held high, the first three stages of the prescaler are bypassed, speeding up the device by 2^3 or 8 times.
3. In normal operation, a 3-bit mode register controlled by S2 determines the mode the watch will enter, i.e., (RUN I, RUN II, up-date). Six modes (0-5) are normally used. When the CT input is high, this allows the 3-bit register to count past 5 to modes 6 and 7. Mode 6 is basically a vacant mode in both devices. Once in mode 7, the CT input can be reduced to zero and times 8 operation will continue. At this time the CT input couples directly into the adder circuit of the dynamic shift register to allow for direct manipulation of the information in the dynamic shift register.
4. Any time the CT input is activated, the switch debounce circuitry on the chip is bypassed.



Typical value of feedback resistance (R_f) = 10 to 20 megohms

Typical crystal load capacitance (C_L)=15 pF

See ICAN 6086 for more detailed oscillator discussion

* **In watch layouts, avoid layout geometrics that can cause coupling of segment signals to oscillator input or output terminals. Excessive capacitive coupling can cause oscillator frequency variation that can affect watch accuracy.**

Fig.3 – Oscillator configurations.

High-Voltage Supplies

Both devices have internal circuitry which, when connected with three external low-value capacitors, operates as a voltage tripler to convert the nominal 1.5 volt battery voltage to greater than 4 volts to drive the liquid-crystal display and the display-driver section of the chip. (See Fig.4). Alternately, two capacitors may be used in a voltage-doubler configuration to convert the 1.5-volt supply to a V_{EE} of greater than 2.7 volts (See Fig.5). The devices also have a 256 Hz, 15 μs pulse output (DDC) which can be used to drive an external flyback type high-voltage supply circuit if a display voltage greater than 4.5 volts is required (See Fig.6).

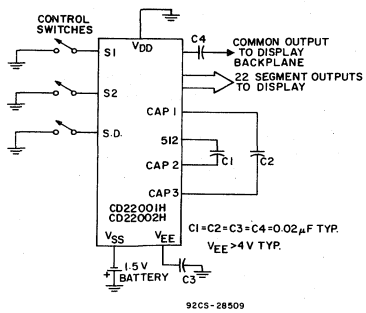


Fig.4 — Typical application using voltage-tripler high-voltage converter configuration (oscillator not shown).

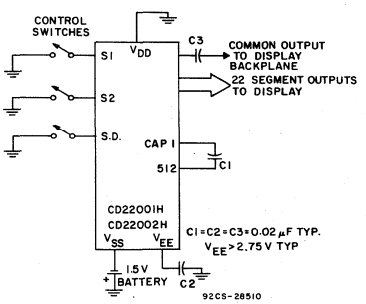


Fig.5 — Typical application using voltage-doubler high-voltage converter configuration (oscillator not shown)

Shutdown Input

The shutdown input is normally pulled down to V_{SS} by an on-chip resistor. When held at V_{DD}, the shutdown input causes the oscillator to stop, resets the watch, and disables the high-voltage supply, thereby reducing total watch current to a minimum value and imposes negligible loading on the battery. This condition allows storage of the watch with the battery connected. Releasing shutdown restores the oscillator and high-voltage supply operation, and the watch is held in the reset mode.

Reset Mode

When the shutdown input is activated and released, the watch is put in the reset mode. The mode is RUN I displaying hours-minutes with the colon frozen on and the counters reset to December 1 at 12:00 AM with seconds frozen at 00. Depressing S1 releases the hold on seconds, the colon begins flashing, and normal time-keeping operation is resumed.

The CD22002H may also be placed in the reset condition by activating S1 and S2 simultaneously.

Mounting Considerations

All COS/MOS chips are non-gold backed and require the use of epoxy mounting. DuPont No.5504A conductive silver paste or equivalent is recommended. In any case, the manufacturer's recommendations for storage and use should be followed. If DuPont No. 5504A paste is used, the bond should be cured at temperatures between 185°C and 200° for 75 minutes.

In COS/MOS circuits, p-channel substrates are connected to V_{DD}; therefore, when chips are mounted and a conductive paste is used, care must be taken to keep the active substrate isolated from ground or other circuit elements.

Packing, Shipping, and Storage Criteria

Solid state chips, unlike packaged devices, are non-hermetic devices, normally fragile and small in physical size, and therefore, require special handling considerations as follows:

1. Chips must be stored under proper conditions to insure that they are not subjected to a moist and/or contaminated atmosphere that could alter their electrical physical, or mechanical characteristics. After the shipping container is opened, the chip must be stored under the following conditions:
   A. Storage temperature, 40°C max. recommended
   B. Relative humidity, 50% max.
   C. Clean, dust-free environment
2. The user must exercise proper care when handling chips to prevent even the slightest physical damage to the chip.
3. During mounting and lead bonding of chips the user must use proper assembly techniques to obtain proper electrical, thermal, and mechanical performance.
4. After the chip has been mounted and bonded, any necessary procedure must be followed by the user to insure that these non-hermetic chips are not subjected to moist or contaminated atmosphere which might cause the development of electrical conductive paths across the relatively small insulating surfaces. In addition, proper consideration must be given to the protection of these devices from other harmful environments which could conceivably adversely affect their proper performance.

Handling Criteria

The user should find the following suggested precautions helpful in handling COS/MOS chips.

1. **Grounding**
   a. Bonders, pellet pick-up tools, table tops, trim and form tools, sealing equipment, and other equipment used in chip handling should be properly grounded.
   b. The operator should be properly grounded.
2. **In-Process Handling**
   a. Assemblies or subassemblies of chips should be transported and stored in conductive carriers.
   b. All external leads of the assemblies or subassemblies should be shorted together.
3. **Bonding Sequence**
   a. Connect V_{DD} first to external connections, for example, terminal 21 of these types.
   b. Remaining functions may be connected to their external connections in any sequence.
4. **Testing**
   a. Transport all assemblies of chips in conductive carriers.
   b. In testing chip assemblies or subassemblies, the operator should be properly grounded.

For additional handling considerations for COS/MOS devices, refer to ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits", available on request from RCA Solid State Division, Box 3200, Somerville, N.J. 08876.

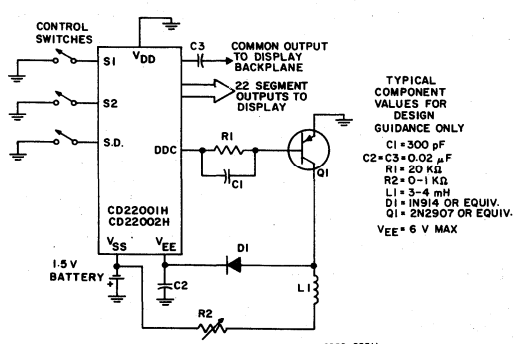


Fig.6 — Typical application using flyback-type high-voltage converter configuration (oscillator not shown).

STATIC ELECTRICAL CHARACTERISTICS AT $T_A = 25^oC$, $V_{DD} = 0$ V

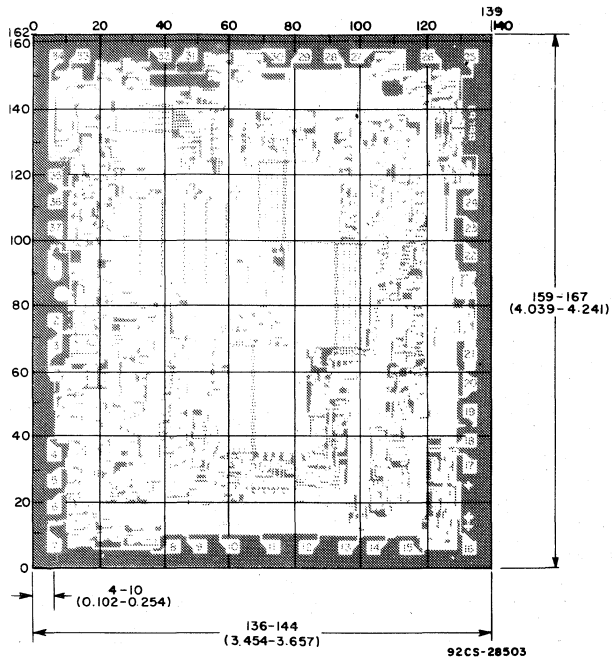
CHARACTERISTIC	TEST CONDITIONS V_O V	V_{SS} V	V_{EE} V	LIMITS Min.	Typ.	Max.	UNITS
LOW VOLTAGE (V_{SS}) SECTION							
Quiescent Device Current I_{DD}	▲	−1.5	–	–	0.1	1	μA
Output Voltage (512 Hz and DDC Outputs):							
Low Level V_{OL}	–	−1.5	–	−1.45	−1.5	–	V
High Level V_{OH}	–	−1.5	–	–	0	−0.05	
Output Drive Current (512 Hz and DDC Outputs):							
N-Channel (Sink) I_{OL}	−1	−1.5	–	100	200	–	μA
P-Channel (Source) I_{OH}	−0.5	−1.5	–	−30	−100	–	
HIGH VOLTAGE (V_{EE}) SECTION							
Quiescent Device Current I_{DD}	▲	–	−4	–	0.1	–	μA
Output Voltage (Segment and Common Outputs):							
Low Level V_{OL}	–	–	−4	−3.95	−4	–	V
High Level V_{OH}	–	–	−4	–	0	−0.05	
Output Drive Current (Segment and Common Outputs):							
N-Channel (Sink) I_{OL}	−3.5	–	−4	60	200	–	μA
P-Channel (Source) I_{OH}	−0.5	–	−4	−60	−200	–	
INPUTS							
	V_{IN}	V_{SS}	V_{EE}				
Input Current I_{IN}:							
Oscillator	0, −1.5	−1.5	–	–	±150	–	nA
Setting and C_T	0	−1.5	–	–	10*	–	μA
Shutdown	0	−1.5	–	–	0.1	–	

* Input current due to internal pull-down. ▲ Shutdown mode.

DYNAMIC ELECTRICAL CHARACTERISTICS AT $T_A = 25^oC$, $V_{DD} = 0$ V

CHARACTERISTICS	TEST CONDITIONS	V_{SS} V	LIMITS Min.	Typ.	Max.	UNITS
Crystal Oscillator Starting Voltage V_S	f_{IN} = 32768 Hz	–	–	−1.2	−1.4	V
Operating Current:						
V_{SS} Section I_{SS}□	f_{IN} = 32768 Hz	−1.5	–	3	5	μA
V_{EE} Section I_{EE}□		−1.5	–	0.2	1	
Converter Frequency (DDC Output) f_{DDC}	f_{IN} = 32768 Hz	−1.5	–	256	–	Hz
Tripler Frequency (512 Output) f_{TR}		−1.5	–	512	–	
Display Segment Frequency Output f_{SEG}		−1.5	–	32	–	
Oscillator Input Capacitance C_{IN}	V_{IN} = −0.8 V	−1.5	–	5	–	pF
Oscillator Output Capacitance C_O		−1.5	–	5	–	
Tripler Output Voltage V_{EE}	f_{IN} = 32768 Hz, I_{EE} = 1 μA	−1.5	−3.5	−4	–	V

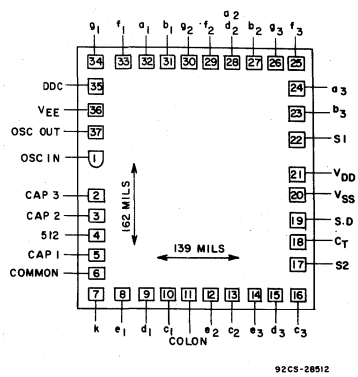
□ With crystal oscillator operating, no display or high-voltage converter connected, and no control inputs activated.



Dimensions and Pad Layout for CD22001H and CD22002H.

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).



Pad designation and location diagram for the CD22001H and CD22002H.

COS/MOS 6-Function Liquid-Crystal Digital-Watch Circuit with Stopwatch

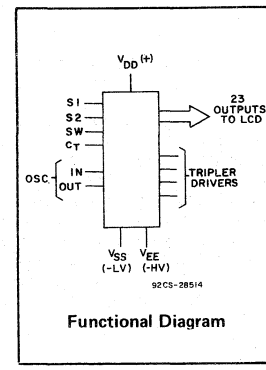
The RCA-CD22003H* is a complementary MOS circuit containing all logic necessary for a digital readout wristwatch that will display either hours and minutes, month and date, or seconds, plus a 15-minute, 1 second resolution stopwatch on a single 3-1/2 digit field-effect liquid crystal display.

The chip contains an inverter-amplifier for a 32-kHz quartz crystal oscillator, a countdown chain, and counters for seconds, minutes, hours, date and months. The display section contains seven-segment decoders plus level translators and drivers to provide high-voltage ac drive to each of the 23 segments. Access to the control section is provided by two chip inputs, S1 and S2.

These inputs are activated by a pushbutton contact to the watch case (V_{DD}).

Debounce circuitry is provided on the chip.

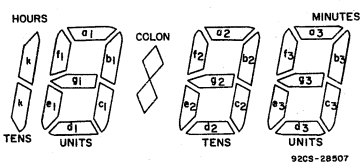
* Formerly Developmental type No. TA10039A.



Functional Diagram

Special Features:

- **3-1/2 digit display, 6-function watch: month, date, hours, minutes, seconds, and stopwatch**
- **Two timekeeping display modes**
- **Simple two-button operation**
- **Simple high-voltage converter on chip**
- **Single-cell operation**
- **Counter test input for high-speed testing**
- **15-minute, 1 second resolution stopwatch**
- **Smart calendar**
- **Automatic and manual reset**
- **Automatic shutdown for power conservation**



	a	b	c	d	e	f	g
1		X	X				
2	X	X		X	X		X
3	X	X	X	X			X
4		X	X			X	X
5	X		X	X		X	X
6	X		X	X	X	X	X
7	X	X	X				
8	X	X	X	X	X	X	X
9	X	X	X	X		X	X
0	X	X	X	X	X	X	

X = Segment activated

Fig.2 – Segment designations and number to segment definition.

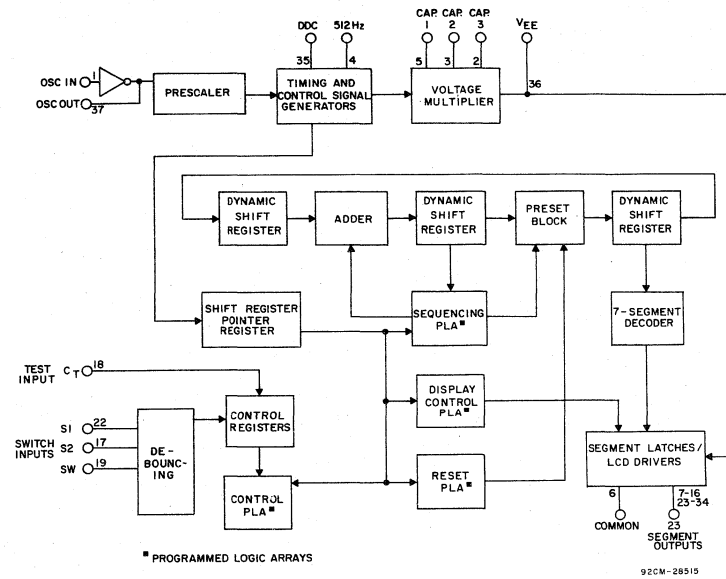


Fig.1 – Block diagram of the CD22003H.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE: (V_{DD}–V_{SS}), (V_{DD}–V_{EE})	–0.5 to +6 V
INPUT VOLTAGE RANGE: OSC. IN, OSC. OUT, S1, S2, C_T Test, and Shutdown	$V_{SS} \leqslant V_{IN} \leqslant V_{DD}$
DEVICE DISSIPATION	200 mW
OPERATING-TEMPERATURE RANGE (T_A)	–10 to +60°C
STORAGE-TEMPERATURE RANGE (T_{stg})	–20 to +70°C

CD22003H

Architecture

The operation and timekeeping of the CD22003H is controlled by an innovative dynamic circuit as shown in Fig. 1. The architecture of the CD22003H is designed around a recirculating dynamic shift register. Timing information is circulated through the register at a very precise rate as determined by the crystal oscillator. This information is read from the dynamic shift register and altered by a series of programmed logic arrays (PLA). At certain intervals during the dynamic shift register cycle, information is latched from the shift register and decoded into seven segment information to be displayed on the LCD.

Watch Operation

The display and set functions are controlled by two switches, S1 and S2. The seven items which can be displayed are:

Functions	Example
1. time (hours and minutes)	12:00
2. date (month and day)	12 1
3. seconds	:01
4. set month	12
5. set day	1
6. set hour	12: A
7. set minute	:00

In general, the colon is used to distinguish time from date, and position (right or left of colon) is used to distinguish hours from minutes and the month from the day. Seconds can be recognized because they change once per second and the colon remains on.

The first three items (time, date, and seconds) can be called up in either of two "RUN" modes. During operation in these modes, S1 is used to select either time, date, or seconds to appear on the display. The remaining items (4 through 7) are set modes. In these modes, S1 is used to advance the item being displayed. S2 is used to advance the watch to the desired RUN or SET mode as follows:

1. RUN I
2. RUN II
3. set month
4. set day
5. set hour
6. set minutes

Each momentary depression of S2 advances the watch to the next mode.

RUN I Mode

In RUN I mode, the watch normally displays hours and minutes with the colon flashing at 1 Hz. Depressing S1 will cause month and day to be displayed as long as the button is held. The display will return to hours-minutes 1-1/2 seconds after S1 is released. Seconds can be called up by depressing S1 once if date is displayed or twice if hours-minutes are displayed. Seconds will then continue to be displayed until S1 is again depressed and the display returns to hours-minutes.

RUN II Mode

In RUN II mode, the watch alternately displays hours-minutes, then month-day for 1-second each. Depressing S1 once calls up seconds. Depressing S1 again restores the alternating condition. Note that when seconds are displayed, RUN I and RUN II are indistinguishable. In either case, however, depressing S1 returns the watch to a distinguishable condition.

Additional Features

The day counter will count 28, 30, or 31 days depending on the month. February is considered a 28-day month, and therefore, the day must be set every four years on leap year. This is done by waiting until March 1 (the watch will read March 2), and then setting the correct day.

A leading zero in digit two is blanked when day is displayed but appears for minutes and seconds.

Setting the Watch

To set the watch, depress and release S2 until only the month appears on the display. The month appears on the left, the colon is off and the right side is blank. The month can be advanced at a 1-Hz rate by depressing and holding S1, or stepped one month at a time by momentarily depressing and releasing S1.

From this condition, one momentary depression of S2 causes the day to appear. The day is displayed on the right, the colon is off and the left side is blank. The day can be advanced in the same manner as for the month update.

The next momentary depression of S2 calls up the hour. The hour appears on the left, the colon is on and an A or P (AM or PM) will appear on the far right. The A or P changes when the hour is advanced through 12:, the total cycle being twenty-four (24) hours.

The next depression of S2 calls up minutes. If minutes are advanced using S1, the seconds are reset to zero and placed on hold. The minutes should be set ahead by approximately one minute, compared to standard time. After advancing to either RUN mode by depressing S2 once for RUN I or twice for RUN II, the hold is then released by depressing S1 to resume normal timekeeping. Using this method, the watch can be accurately set to within 1/4 second of the desired time.

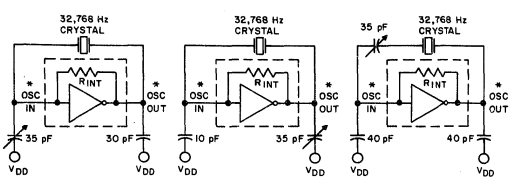
Display Drive

The ac drive for the liquid-crystal display is generated from the 32-Hz square wave in the countdown chain. The 32-Hz waveform, like all other logic signals on the chip, has an amplitude of 1.5 V. In order to drive a liquid-crystal display, the amplitude must be changed to higher voltages. Therefore, the 32-Hz square wave is passed through a level translator and driver circuit before it becomes the Common Output to the backplane of a display. The Common Output and its complement are routed to the other 22 output drivers. In response to low-level logic signals from the timekeeping section of the chip, the output drivers apply either the true Common Output or its complement to the segments of the display. Applying the true waveform maintains the segment in an off (unactivated) state, because the differential voltage between segment and backplane of the display is zero. Applying the complement waveform maintains the segment in an on (activated) state because the differential voltage between segment and backplane is twice the magnitude of V_{EE}. The nomenclature of the display segments is given in Figure 2. In order to prevent any potentially damaging dc voltage from appearing across the LCD, which might occur if the oscillator stops because of low battery voltage or if the watch is in the shutdown mode, a capacitor should be placed in series with the common backplane output. The capacitor value may typically be 0.02 μF. (See Figs. 4, 5, and 6).

Test Inputs

The CT "test" input may be used to speed up operation of the watch circuit to facilitate rapid testing. The actual function of the CT input is dependent upon the different states of the device.

1. During shutdown, the CT input becomes the input to the dynamic shift register which, in a static mode, allows testing of leakage current in two major states, all "1" or all "0".



a) INPUT TRIM b) OUTPUT TRIM c) SERIES TRIM

NOTE: THE CD22003H HAS AN INTERNAL OSCILLATOR FEEDBACK RESISTOR INCORPORATED ON CHIP, $R_{INT} \approx 15$ MΩ

Typical crystal load capacitance (C_L)=15 pF
See ICAN 6086 for more detailed oscillator discussion

*** In watch layouts, avoid layout geometrics that can cause coupling of segment signals to oscillator input or output terminals. Excessive capacitive coupling can cause oscillator frequency variation that can affect watch accuracy.**

Fig. 3 — Oscillator configurations.

92CM-28515

2. In normal operation, if CT is held high, the first three stages of the prescaler are bypassed, speeding up the device by 2^3 or 8 times.
3. In normal operation, a 3-bit mode register controlled by S2 determines the mode the watch will enter, i.e., (RUN I, RUN II, up-date). Six modes (0-5) are normally used. When the CT input is high, this allows the 3-bit register to count past 5 to modes 6 and 7. Mode 6 is basically a vacant mode in both devices. Once in mode 7, the CT input can be reduced to zero and times 8 operation will continue. At this time the CT input couples directly into the adder circuit of the dynamic shift register to allow for direct manipulation of the information in the dynamic shift register.
4. Any time the CT input is activated, the switch debounce circuitry on the chip is bypassed.

High-Voltage Supplies

The CD22003H has internal circuitry which, when connected with 3 external low-value capacitors, operates as a voltage tripler to convert the nominal 1.5 volt battery voltage to greater than 4 volts to drive the liquid-crystal display and the display-driver section of the chip. (See Fig.4). Alternately, two capacitors may be used in a voltage-doubler configuration to convert the 1.5-volt supply to a V_{EE} of greater than 2.7 volts (See Fig.5). The CD22003H has a 256-Hz 15 μs pulse output (DDC) which can be used to drive an external flyback type high-voltage supply circuit if a display voltage greater than 4.5 volts is required (See Fig.6).

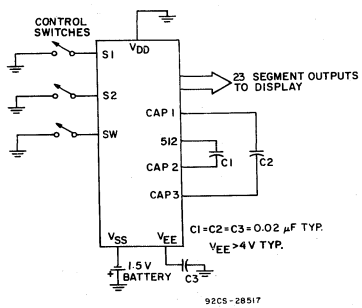


Fig.4 – Typical application using voltage tripler high-voltage converter configuration (oscillator not shown).

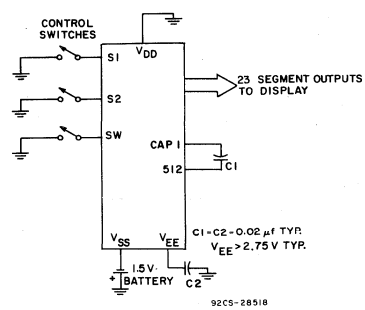


Fig.5 – Typical application using voltage doubler high-voltage converter configuration (oscillator not shown).

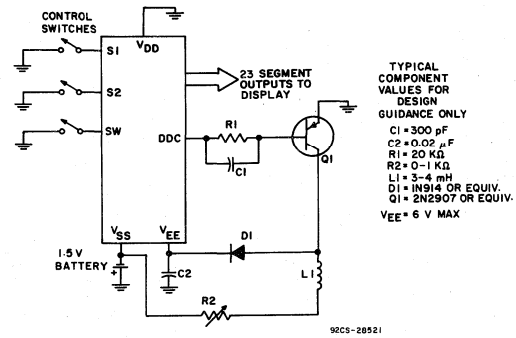


Fig.6 – Typical application using flyback-type high-voltage converter configuration (oscillator not shown).

Stopwatch

The 15 minute, 1-second resolution stopwatch is accessed by momentarily connecting the stopwatch (SW) input to V_{DD}. The stopwatch comes up reset displaying 0 minutes and 00 seconds with the colon on. Another closure of SW starts the display counting at a 1 Hz rate, a second closure of SW stops the counting with the elapsed time frozen on the display, and a third closure of SW resets the stopwatch to zero. The start-stop-reset cycle continues until the watch is brought out of the stopwatch mode by momentarily closing the S1 switch to V_{DD}. The stopwatch recycles and begins to count from 0:00 after 15 minutes. Because stopwatch is independent of the rest of the watch, normal timekeeping is unaffected by the stopwatch operation.

Shutdown Input

The shutdown function occurs automatically. The watch is placed in the months update mode and, if no switches are depressed for 30 seconds, the watch enters shutdown and the display goes off. In shutdown mode, the oscillator is stopped, the watch is reset, and the high-voltage supply is disabled, thereby reducing total watch current to a minimum value. This condition allows storage of the watch with the battery connected. Closing the S2 input to V_{DD} restarts the watch in the reset condition. If the watch is in any mode other than months update mode, or any switch input is closed to V_{DD}, the shutdown timer is reset.

Reset Mode

When the shutdown input is activated and released, the watch is put in the reset mode. The mode is RUN I displaying hours-minutes with the colon frozen on and the counters reset to December 1 at 12:00 AM with seconds frozen at 00. Depressing S1 releases the hold on seconds, the colon begins flashing, and normal time-keeping operation is resumed.

The CD22003H may also be placed in the reset condition by activating S1 and S2 simultaneously.

Mounting Considerations

All COS/MOS chips are non-gold backed and require the use of epoxy mounting. DuPont No.5504A conductive silver paste or equivalent is recommended. In any case, the manufacturer's recommendations for storage and use should be followed. If DuPont No. 5504A paste is used, the bond should be cured at temperatures between 185°C and 200° for 75 minutes.

In COS/MOS circuits, p-channel substrates are connected to V_{DD}; therefore, when chips are mounted and a conductive paste is used, care must be taken to keep the active substrate isolated from ground or other elements.

Packing, Shipping, and Storage Criteria

Solid state chips, unlike packaged devices, are non-hermetic devices, normally fragile and small in physical size, and therefore, require special handling considerations as follows:

1. Chips must be stored under proper conditions to insure that they are not subjected to a moist and/or contaminated atmosphere that could alter their electrical physical, or mechanical characteristics.

After the shipping container is opened, the chip must be stored under the following conditions:

A. Storage temperature, 40°C max. recommended
B. Relative humidity, 50% max.
C. Clean, dust-free environment

2. The user must exercise proper care when handling chips to prevent even the slightest physical damage to the chip.
3. During mounting and lead bonding of chips the user must use proper assembly techniques to obtain proper electrical, thermal, and mechanical performance.
4. After the chip has been mounted and bonded, any necessary procedure must be followed by the user to insure that these non-hermetic chips are not subjected to moist or contaminated atmosphere which might cause the development of electrical conductive paths across the relatively small insulating surfaces. In addition, proper consideration must be given to the protection of these devices from other harmful environments which could conceivably adversely affect their proper performance.

Handling Criteria

The user should find the following suggested precautions helpful in handling COS/MOS chips.

1. Grounding

a. Bonders, pellet pick-up tools, table tops, trim and form tools, sealing equipment, and other equipment used in chip handling should be properly grounded.
b. The operator should be properly grounded.

2. In-Process Handling

a. Assemblies or subassemblies of chips should be transported and stored in conductive carriers.
b. All external leads of the assemblies or subassemblies should be shorted together.

3. Bonding Sequence

a. Connect V_{DD} first to external connections, for example, terminal 21 of this type.
b. Remaining functions may be connected to their external connections in any sequence.

4. Testing

a. Transport all assemblies of chips in conductive carriers.
b. In testing chip assemblies or subassemblies, the operator should be properly grounded.

For additional handling considerations for COS/MOS devices, refer to ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits", available on request from RCA Solid State Division, Box 3200, Somerville, N.J. 08876.

STATIC ELECTRICAL CHARACTERISTICS AT T_A = 25°C, V_{DD} = 0 V

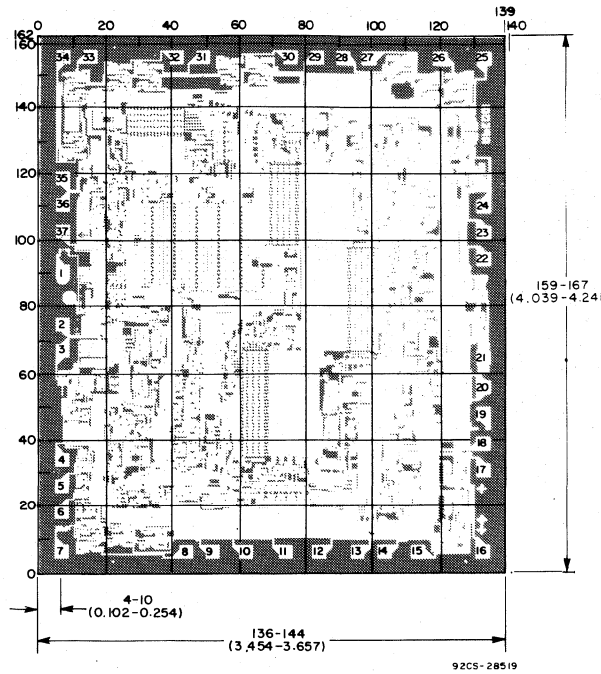
CHARACTERISTIC	TEST CONDITIONS V_O V	V_{SS} V	V_{EE} V	LIMITS Min.	Typ.	Max.	UNITS
LOW VOLTAGE (V_{SS}) SECTION							
Quiescent Device Current I_{DD}	▲	−1.5	–	–	0.1	1	μA
Output Voltage (512 Hz and DDC Outputs):							
Low Level V_{OL}	–	−1.5	–	−1.45	−1.5	–	V
High Level V_{OH}	–	−1.5	–	–	0	−0.05	V
Output Drive Current (512 Hz and DDC Outputs):							
N-Channel (Sink) I_{OL}	−1	−1.5	–	100	200	–	μA
P-Channel (Source) I_{OH}	−0.5	−1.5	–	−30	−100	–	μA
HIGH VOLTAGE (V_{EE}) SECTION							
Quiescent Device Current I_{DD}	▲	–	−4	–	0.1	–	μA
Output Voltage (Segment and Common Outputs):							
Low Level V_{OL}	–	–	−4	−3.95	−4	–	V
High Level V_{OH}	–	–	−4	–	0	−0.05	V
Output Drive Current (Segment and Common Outputs):							
N-Channel (Sink) I_{OL}	−3.5	–	−4	60	200	–	μA
P-Channel (Source) I_{OH}	−0.5	–	−4	−60	−200	–	μA
INPUTS							
	V_{IN}	V_{SS}	V_{EE}				
Input Current I_{IN}:							
Oscillator	0,−1.5	−1.5	–	–	±150	–	nA
Setting and C_T	0	−1.5	–	–	10*	–	μA
Stopwatch	0	−1.5	–	–	10*	–	μA

* Input current due to internal pull-down. ▲ Shutdown mode.

DYNAMIC ELECTRICAL CHARACTERISTICS AT T_A = 25°C, V_{DD} = 0 V

CHARACTERISTICS	TEST CONDITIONS	V_{SS} V	LIMITS Min.	Typ.	Max.	UNITS
Crystal Oscillator Starting Voltage V_S	f_{IN} = 32768 Hz	–	–	−1.2	−1.4	V
Operating Current:						
V_{SS} Section I_{SS}□	f_{IN} = 32768 Hz	−1.5	–	3	5	μA
V_{EE} Section I_{EE}□		−1.5	–	0.2	1	μA
Converter Frequency (DDC Output) f_{DDC}	f_{IN} = 32768 Hz	−1.5	–	256	–	Hz
Tripler Frequency (512 Output) f_{TR}		−1.5	–	512	–	Hz
Display Segment Frequency Output f_{SEG}		−1.5	–	32	–	Hz
Oscillator Input Capacitance C_{IN}	V_{IN} = −0.8 V	−1.5	–	5	–	pF
Oscillator Output Capacitance C_O		−1.5	–	5	–	pF
Tripler Output Voltage V_{EE}	f_{IN} = 32768 Hz, I_{EE} = 1 μA	−1.5	−3.5	−4	–	V

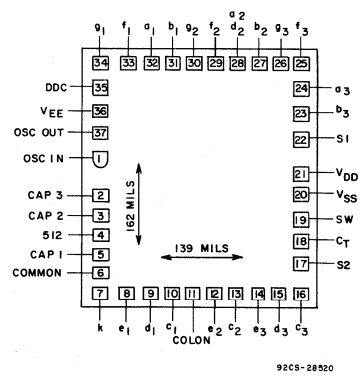
□ With crystal oscillator operating, no display or high-voltage converter connected, and no control inputs activated.



The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Dimensions and pad layout.



Pad designation and location diagram.

CD22006H

COS/MOS 6-Function Liquid-Crystal Digital-Watch Circuit

The CD22006H* is a single-chip timekeeping complementary MOS integrated circuit for use in six-function four-digit liquid-crystal-display watches. It is capable of displaying the month and date, the day of the week in alphabetic format, the hours and minutes, or seconds. The circuit contains an oscillator-amplifier for use with 32-kHz quartz crystals, and all countdown and timing logic necessary for the basic six functions, including four-year calendar logic. The display section contains a seven-segment decoder, level translators, and drivers to provide high-voltage ac drive for the segments of the liquid-crystal display. An on-chip voltage multiplier requiring a minimal number of external components provides the high voltage from a single 1.5 volt battery. Two switch inputs, S1 and S2, control the operation of the watch.

A single bond pad connection reverses the month and date positions on the display. All switch inputs have on-chip pull-down resistors, and are debounced by internal circuitry at a frequency of 16 Hz.

The CD22006H is supplied in chip form.

* Formerly RCA Dev. No. TA10178H.

Objective Data

Special Features:

- **4-digit display**
- **On-chip voltage multiplier circuitry**
- **Simple update procedure**
- **Single cell battery operation**
- **4-year calendar**
- **Power-up reset**

Special Features (Cont'd):

- **Automatic shutdown**
- **On-chip debounce circuitry**
- **Month-Date position reversal option**
- **On-chip oscillator feedback resistor and capacitors**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE:	
($V_{DD}-V_{SS}$), ($V_{DD}-V_{EE}$)	−0.5 to +6 V
INPUT VOLTAGE RANGE:	
OSC. IN, OSC. OUT, S1, S2, C_T and MDR	$V_{SS} \leqslant V_{IN} \leqslant V_{DD}$
DEVICE DISSIPATION	200 mW
OPERATING-TEMPERATURE RANGE (T_A)	−10 to +60°C
STORAGE-TEMPERATURE RANGE (T_{stg})	−65 to +150°C

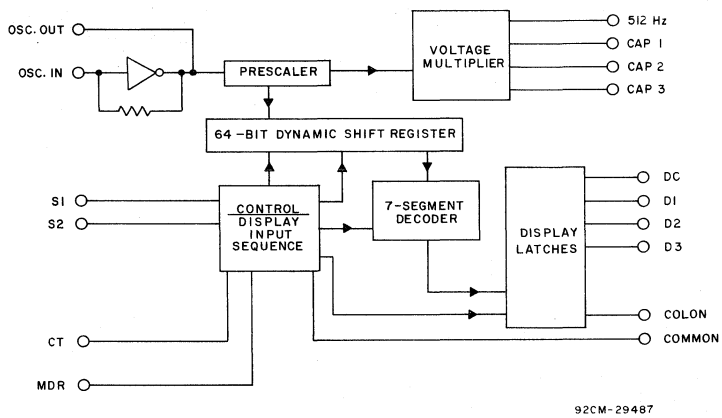


Fig. 1 — Functional block diagram.

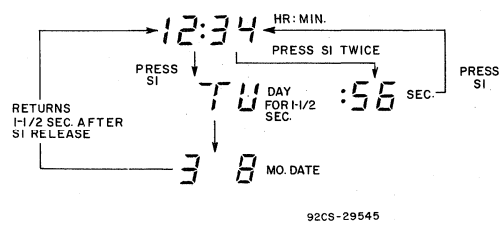


Fig. 2 — Digital display and operating sequence.

COS/MOS 6-Function Liquid-Crystal Digital-Watch Circuit

CD22007H: 6-Function (Month, Date, Day-of-Week, Hours, Minutes, and Seconds

CD22007V1H: 6-Function plus 60 Minute Stopwatch with Tenths of Seconds

CD22007V2H: 6-Function Plus 24 Hour Alarm

The CD22007H*, CD22007V1H*, and CD22007V2H* are single-chip timekeeping complementary MOS integrated circuits for use in multiple-function four-digit liquid-crystal-display watches. The basic six-function circuit, the CD22007H, is capable of displaying the month and date, the day of the week in alphabetic format, the hours and minutes, or seconds. The circuit contains an oscillator-amplifier for use with 32-kHz quartz crystals and all countdown and timing logic necessary for the basic six functions and added features. The display section contains a seven segment decoder, level translators, and drivers to provide high-voltage ac drive for the segments of the liquid-crystal display. An on-chip voltage multiplier requiring a minimal number of external components provides the high voltage from a single 1.5-volt battery. Two switch inputs, S1 and S2, control the operation of the basic six-function watch. A third input, S3, is used to control the added features of the CD22007V1H and CD22007V2H circuits.

The CD22007V1H includes the basic six-function circuit of the CD22007H with the addition of a stopwatch having a 0.1-second resolution and a range of 60 minutes.

The CD22007V2H includes the basic six-function circuit of the CD22007H plus an independent 24-hour alarm clock.

A single bond-pad connection reverses the month and date positions on the display. Another bond-pad connection causes the hours to be displayed in a 24-hour format used with an AM/PM indicator. All switch inputs have on-chip pull-down resistors, and are debounced by internal circuitry at a frequency of 16 Hz.

The CD22007H series types are supplied in chip form.

* Formerly RCA Dev. Nos. TA10282H, TA-10283H, and TA10284H, respectively.

Special Features:

- **4-digit display**
- **On-chip voltage multiplier circuitry**
- **Simple update procedure**
- **Single cell battery operation**
- **4-year calendar**
- **Power-up reset**

Special Features (Cont'd):

- **Automatic shutdown**
- **On-chip debounce circuitry**
- **Month-date position reversal option**
- **12/24-Hour time bond pad option**
- **On-chip oscillator feedback resistor and capacitors**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE:	
($V_{DD}-V_{SS}$), ($V_{DD}-V_{EE}$)	0.5 to +6 V
INPUT VOLTAGE RANGE:	
OSC. IN, OSC. OUT, S1, S2, S3, CT, 12/24 and MDR	$V_{SS} \leqslant V_{IN} \leqslant V_{DD}$
DEVICE DISSIPATION	200 mW
OPERATING -TEMPERATURE RANGE (T_A)	−10 to +60°C
STORAGE-TEMPERATURE RANGE (T_{stg})	−6.5 to +150°C

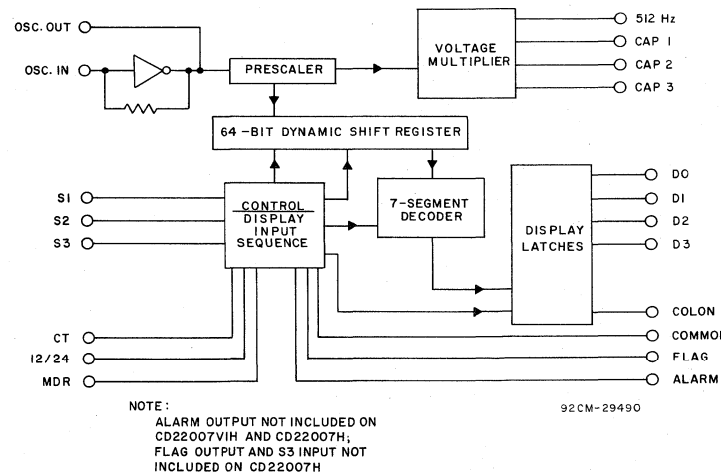


Fig.1 – Functional block diagram.

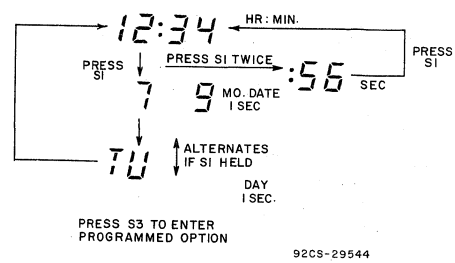


Fig.2 – Digital display and operating sequence.

CD22008H, CD22008VIH, CD22008V2H

Objective Data

COS/MOS 6-Function Liquid-Crystal Digital-Watch Circuit

CD2008H: 6-Function (Month, Date, Day-of-Week, Hours, Minutes, and Seconds

CD22008V1H: 6-Function plus 60 Minute Stopwatch with tenths of seconds

CD22008V2H: 6-Function plus 24-Hour Alarm

The CD22008H, CD22008V1H, and CD22008V2H are single-chip timekeeping complementary MOS integrated circuits for use in multiple-function 6-digit liquid-crystal display watches. The basic 6-function circuit, the CD22008H, is capable of displaying the month, date, day of the week in alphabetic format, hours, minutes, and seconds in three operating modes. The circuit contains an oscillator-amplifier with an internal feedback resistor for use with 32-kHz quartz crystals, and all countdown and timing logic necessary for the basic six functions and added features. The display section contains a 7-segment decoder, level translators, and drivers to provide high-voltage ac drive for the segments of the liquid-crystal display. An on-chip voltage multiplier requiring a minimal number of external components provides the high voltage from a single 1.5-volt battery. Two switch inputs, S1 and S2, control the operation of the basic 6-function watch. A third input, S3, is used to control the added features in the CD22008V1H and CD22008V2H circuits.

The CD22008V1H includes the basic six-function circuit of the CD22008H with the addition of a stopwatch having a 0.1-second resolution and a range of 60 minutes.

The CD22008V2H includes the basic 6-function circuit of the CD22008H plus an independent 24-hour alarm clock.

The CD22008H Series contains circuitry to allow for resetting the watch to the nearest hour (Fast-Sync mode).

A single bond-pad connection reverses the month and date positions on the display. Another bond-pad connection causes the hours to be displayed in 24-hour format. All switch inputs have on-chip pull-down resistors, and are debounced by internal circuitry.

The CD22008H Series is supplied in chip form.

Note: The CD22008H, CD22008V1H, and CD22008V2H were formerly RCA Developmental Nos. TA10327H, TA-10328H, and TA10329H, respectively.

Features:

- 6-Digit display with 2 flags
- Single-cell battery operation
- Fast-sync mode
- Power-up Reset
- Automatic Shutdown
- Simple Update procedure
- 4-Year calendar

Features (Cont'd)

- 12/24 Hour time option
- Month-Date position reversal option
- On-Chip circuitry for:
  - Voltage multiplier
  - Oscillator feedback
  - Switch debounce
- High-speed test capability

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE RANGE:	
(V_{DD}–V_{SS}), (V_{DD}–V_{EE})	–0.5 to +6 V
INPUT VOLTAGE RANGE:	
OSC. IN, OSC. OUT, S1, S2, S3, C_T, 12/24 and MDR	$V_{SS} \leqslant V_{IN} \leqslant V_{DD}$
DEVICE DISSIPATION	200 mW
OPERATING-TEMPERATURE RANGE (T_A)	10 to +60°C
STORAGE-TEMPERATURE RANGE (T_{stg})	–6.5 to +150°C

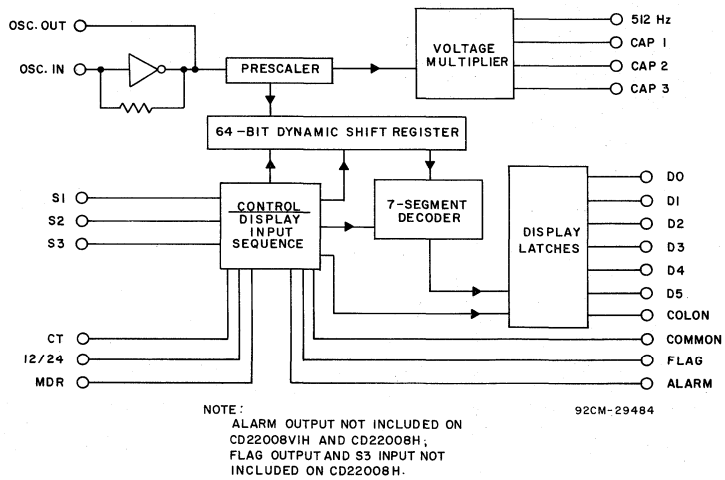


Fig.1 – Functional block diagram.

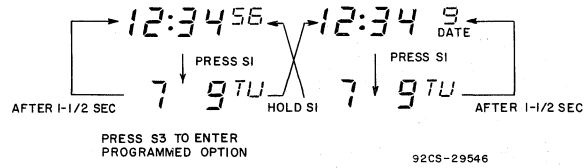


Fig.2 – Digital display and operating sequence.

COS/MOS 2-Function Liquid-Crystal Digital-Watch Circuit

Objective Data

CD22009H: 2-Function (Hours and Minutes)
CD22009RH: Mirror Image of CD22009H

The CD22009H and CD22009RH are single-chip timekeeping complementary MOS integrated circuits for use in 2-function liquid-crystal-display watches. The circuit contains a self-biased input amplifier for use as a 32,768-Hz crystal oscillator, counters, level translators, a seven-segment decoder, and drivers to provide high-voltage ac drive for the segments of a 3-1/2 digit, 12-hour liquid-crystal display. An on-chip voltage multiplier, requiring a minimal number of external components provides the high voltage from a single 1.5-volt battery.

Display updating and time setting are accomplished by applying V_{DD} through two SPST switches, S1 and S2. Both inputs are protected against switch bounce for periods up to 30 milliseconds. Internal pull-down resistors establish the input level at V_{SS} when S1 and S2 are open. The updating method is outlined in Table I.

The CD22009H and CD22009RH are supplied in chip form.

Special Features:

- 3-1/2 digit display
- 32-kHz operation
- Hours and minutes decoding with 1-Hz flashing colon
- Single-cell operation
- 2-SPST switch updating
- On-chip circuitry for:
  - Voltage multiplier
  - Oscillator feedback
  - Switch debounce
- Counter test input for high-speed testing
- Mirror-image layout option

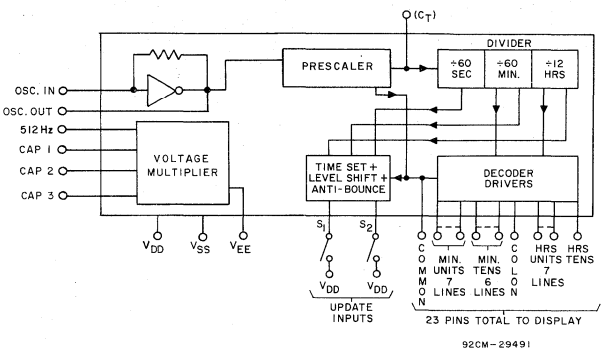
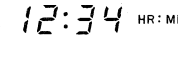


Fig. 1 – Functional block diagram.



92CS-29547

Fig. 2 – Digital display.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE:
($V_{DD}-V_{SS}$), ($V_{DD}-V_{EE}$) ..... −0.5 to +6 V
INPUT VOLTAGE RANGE:
OSC. IN, OSC. OUT, S1, S2 ..... $V_{SS} \leqslant V_I \leqslant V_{DD}$
C_T ..... $V_{EE} \leqslant V_I \leqslant V_{DD}$
DEVICE DISSIPATION ..... 200 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... −10 to +60°C
STORAGE-TEMPERATURE RANGE (T_{stg}) ..... −20 to +70°C

Table I

Operating State	Display Indication Before Switch Closure	Switch S1	Switch S2	Function After Switch Closure
1	Flashing Colon (1 Hz)	Open	Open	Normal Operation
2	Flashing Colon (1 Hz)	Open	V_{DD}	Hours set @ 1-Hz rate—minutes counting not affected
3	Flashing Colon (1 Hz)	Open-V_{DD}-open (Momentary)	Open	Seconds Reset (Colon "on" continuously) (Switch S2 function is now "minutes set")
4	Colon "on" Cont'ly	Open	V_{DD}	Minutes set @ 1-Hz rate—hours counting not affected
5	Colon "on" Cont'ly	Open	Open	Hold (Colon "on")—not counting
6	Colon "on" Cont'ly	Open-V_{DD}-open (Momentary)	Open	Normal Operation—start (Switch S2 function is now "Hours Set")

CD22011E

Objective Data

COS/MOS Quartz Analog Clock Circuit

The RCA-CD22011E* is a silicon-on-sapphire COS/MOS timing circuit consisting of a counter that divides by 4,194,304, two inverter output drivers, a zener diode for transient protection, and an input inverters with internal biasing for use as a crystal oscillator.

The outputs, designed for bridge-type operation, are alternating, each with a 3% duty cycle. The input inverter is intended for use as a crystal oscillator/amplifier, but may also be used as a conventional logic inverter.

The CD22011E is supplied in an 8-lead dual-in-line plastic (Mini-DIP) package.

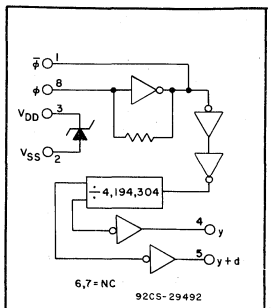
* Formerly RCA Developmental Type TA10294.

Features:

- **Single 1.5-volt battery**
- **Oscillator/amplifier with feedback resistor**
- **High output drive (2 mA typ., source and sink)**
- **Low operating power (60 μA typ., no load)**
- **Zener-diode transient protection**
- **8-lead dual-in-line plastic package**

Applications:

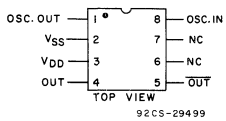
- **Analog display type digital wall clocks and other low voltage timers with stepping motor drives**
- **Digital timing reference**
- **Frequency divider**



FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE RANGE ($V_{DD} - V_{SS}$)	−0.5 to + 5 V
INPUT VOLTAGE RANGE	V_{SS} to V_{DD}
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −10 to +60°C	200 mW
OPERATING-TEMPERATURE RANGE (T_A)	−10 to + 60°C
STORAGE-TEMPERATURE RANGE (T_A)	−65 to + 150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	265°C



TERMINAL ASSIGNMENT

COS/MOS Quartz Analog Clock Circuit

The RCA-CD22012E* is a timing circuit consisting of a counter that divides by 8,388,608, two inverter output drivers, a zener diode for transient protection, and an input inverter for use as a crystal oscillator.

The outputs, designed for bridge-type operation, are alternating, each with a 3% duty cycle. The input inverter is intended for use as a crystal oscillator/amplifier, but may also be used as a conventional logic inverter. The CD22012E is supplied in a 14-lead dual-in-line plastic package.

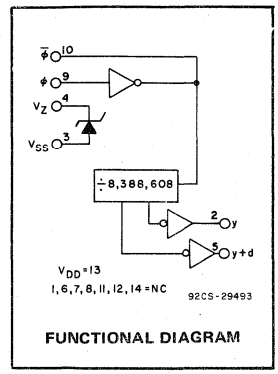
* Formerly RCA Developmental Type TA6489.

Features:

- **Oscillator/amplifier on chip**
- **Operating voltage 12 volts nominal**
- **Operating temperature –40°C to +85°C**
- **High drive capability (6 mA typ., source & sink)**
- **Zener-diode transient protection**
- **14-lead dual-in-line plastic package**

Applications:

- **Automotive clocks, wall clocks, and table clocks with synchronous or stepping motor drives**
- **Digital timing reference**
- **Frequency divider**

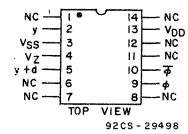


FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE RANGE ($V_{DD} - V_{SS}$)*	–0.5 to + 18 V
INPUT VOLTAGE RANGE	–0.5 to V_{DD} + 0.5 V
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = –40 to +60°C	500 mW
For T_A = +60 to +85°C	Derate linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:	
For T_A = –40 to +85°C	100 mW
OPERATING TEMPERATURE RANGE (T_A)	–40 to +85°C
STORAGE-TEMPERATURE RANGE (T_A)	–65 to + 150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.70 mm) from case for 10 s max.	265°C

* Zener diode not connected.

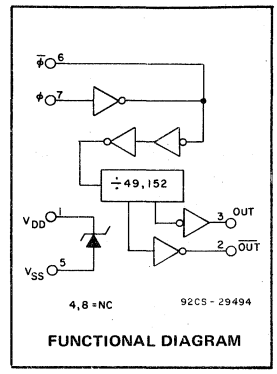


TERMINAL ASSIGNMENT

CD22013E

Objective Data

COS/MOS Quartz Analog Clock Circuit



FUNCTIONAL DIAGRAM

The RCA-CD22013E* is a timing circuit consisting of a counter that divides by 49,152, two inverter output drivers, a zener diode for transient protection, and an input inverter for use as a crystal oscillator.

The outputs are designed for bridge-type operation, and are 180° out of phase, and provide a 50% duty cycle. The input inverter is intended for use as a crystal oscillator/amplifier, but may also be used as a conventional logic inverter. The CD22013E is supplied in an 8-lead dual-in-line plastic (Mini-DIP) package.

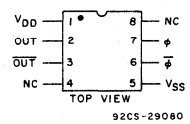
* Formerly RCA Developmental Type TA10176.

Features:

- **Oscillator/amplifier on chip**
- **Operating voltage 12 volts nominal**
- **Operating temperature −40°C to +85°C**
- **Zener-diode transient protection**
- **High push-pull drive (10 mA typical)**
- **8-lead dual-in-line plastic package**

Applications:

- **Automotive clocks, wall clocks, and table clocks with synchronous or stepping motor drives**
- **Digital timing reference**
- **Frequency divider**



TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE RANGE ($V_{DD} - V_{SS}$)	−0.5 to + VZ*
INPUT VOLTAGE RANGE	−0.5 to V_{DD} + 0.5 V
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to + 60°C	500 mW
For T_A = + 60 to + 85°C	Derate linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:	
For T_A = −40 to + 85°C	100 mW
OPERATING TEMPERATURE RANGE (T_A)	−40 to + 85°C
STORAGE-TEMPERATURE RANGE (T_A)	−65 to + 150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	265°C

* Zener breakdown voltage.

COS/MOS Quartz Analog Clock Circuit

The RCA-CD22014E* is a timing circuit consisting of a counter that divides by 65,536, an inverting output buffer, and input inverters for use as a crystal oscillator.

The output provides a 50% duty cycle. The input inverter is intended for use as a crystal oscillator/amplifier, but may also be used as a conventional logic inverter. The CD22014E is supplied in an 8-lead dual-in-line plastic (Mini-DIP) package.

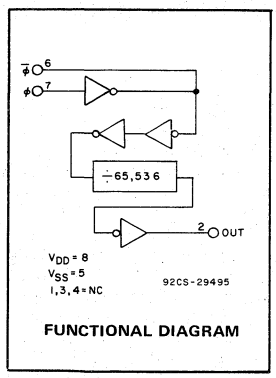
* Formerly RCA Development Type TA6817.

Features:

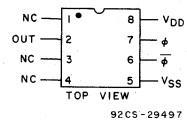
- **Oscillator/amplifier on chip**
- **Nominal 12-volt operation**
- **High output drive (27 mA minimum, source and sink)**
- **Operating temperature −40° to + 80°C**
- **8-lead dual-in-line plastic package**

Applications:

- **Automotive clocks, wall clocks, and table clocks with stepping motor drives**
- **Digital timing reference**
- **Frequency divider**



FUNCTIONAL DIAGRAM



TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE RANGE ($V_{DD} - V_{SS}$)	−0.5 to + 18 V
INPUT VOLTAGE RANGE	−0.5 to V_{DD} + 0.5 V
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C	500 mW
For T_A = +60 to +85°C	Derate linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:	
For T_A = −40 to +85°C	100 mW
OPERATING TEMPERATURE RANGE (T_A)	−40 to +85° C
STORAGE-TEMPERATURE RANGE (T_A)	−65 to + 150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0 70 mm) from case for 10 s max.	265°C

CD22015E

Objective Data

COS/MOS Quartz Analog Clock Circuit

The RCA-CD22015E* is a timing circuit consisting of a counter that divides by 65,536, two inverting output drivers, two 6-V zener diodes for 6-V or 12-V transient protection, and input inverters for use as a crystal oscillator.

The outputs are designed for bridge-type operation, are 180° out of phase, and provide a 50% duty cycle. The input inverter is intended for use as a crystal oscillator/amplifier, but may also be used as a conventional logic inverter.

The CD22015E is supplied in an 8-lead dual-in-line plastic (Mini-DIP) package.

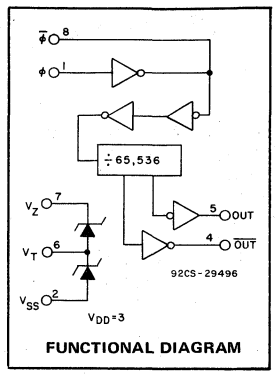
* Formerly RCA Developmental Type TA10177.

Features:

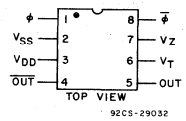
- **Oscillator/amplifier on chip**
- **Zener-diode transient protection**
- **Operating temperature −40°C to + 85°C**
- **Nominal 12 volt operation**
- **High output dirve (10 mA typical, source and sink)**
- **8-lead dual-in-line plastic package**

Applications:

- **Automotive clocks, wall clocks, and table clocks with synchronous or stepping motor drives**
- **Digital timing reference**
- **Frequency divider**



FUNCTIONAL DIAGRAM



TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE RANGE ($V_{DD} - V_{SS}$)	−0.5 to + 18 V
INPUT VOLTAGE RANGE	−0.5 to V_{DD} + 0.5 V
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C	500 mW
For T_A = +60 to +85°C	Derate linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:	
For T_A = −40 to +85°C	100 mW
OPERATING TEMPERATURE RANGE (T_A)	−40 to +85° C
STORAGE-TEMPERATURE RANGE (T_A)	−65 to + 150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.70 mm) from case for 10 s max.	265°C

COS/MOS Industrial Timer

High-Voltage Type (20-V Rating)

Objective Data

The RCA-CD22017E industrial timer consists of an RC oscillator and external input with clock conditioning, ÷5/÷6, ÷10, and ÷ 2^{12} counters with intermediate outputs available for time delay and pulse width decoding; a master-reset; and a 1 Hz output. The three modes of operation — single transition, single pulse, and recycle — are implemented by an output control circuit as instructed by the mode control input.

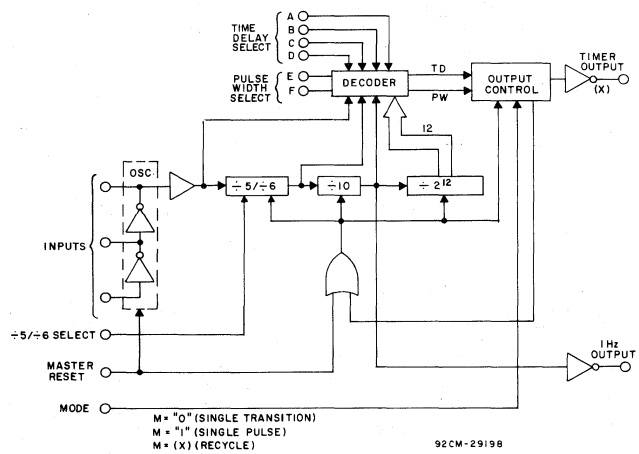
The CD22017E is supplied in a 16-lead dual-in-line plastic package.

Features:

- **External reset**
- **Operates as single transition, single pulse, cyclic timer, or 2^N divider**
- **Clock conditioning**
- **50/60 Hz input select or RC oscillator**
- **Time delay from 0.05 to 2048 sec. or to count of 122,880**
- **1 Hz output digitally derived from line frequency**
- **Output pulse duration digitally selectable**
- **Counter status available via multiplexing onto timer output terminal**
- **Cascadable**

Applications:

- **Industrial control — delay on operate (single transition timer)**
- **Process control — single-pulse timing: cooking, heating, etc. or cyclic timer**
- **Flasher — cyclic timer mode, variable duty cycle.**



Functional Block Diagram

CD22100

Preliminary Data

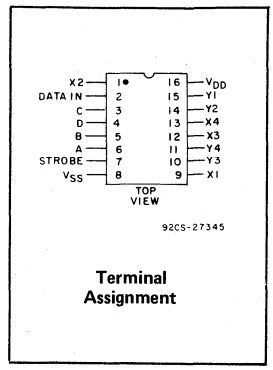
COS/MOS 4 x 4 Crosspoint Switch with Control Memory

The RCA-CD22100 combines a 4 x 4 array of crosspoints (transmission gates) with a 4-line-to-16-line decoder and 16 latch circuits. Any one of the sixteen transmission gates (crosspoints) can be selected by applying the appropriate four line address. The selected transmission gate can be turned on or off by applying a logical one or zero, respectively, to the data input and strobing the strobe input to a logical one. Any number of the transmission gates can be ON simultaneously.

The CD22100 is supplied in 16-lead dual-in-line ceramic packages (D and F suffixes), 16-lead ceramic flat packages (K suffix), 16-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

Features:

- **Low ON resistance — 85 ohms typ. at V_{DD} = 12 volts**
- **"Built-in" control latches**
- **Large analog signal capability: ± $V_{DD}/2$**
- **Transmits signals up to 10 MHz**
- **Matched switch characteristics**
  ΔR_{ON} = 5 ohms typical at
  $V_{DD} - V_{SS}$ = 12 volts
- **High linearity: — 0.5% distortion (typical) at 1 kHz,**
  V_{IN} = 5 volts peak to peak,
  $V_{DD} - V_{SS}$ = 10 V, R_L = 10 kΩ
- **Standard COS/MOS noise immunity**



Terminal Assignment

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE		−65 to +150°C
OPERATING-TEMPERATURE RANGE :		
Package Types D, F, K, H		−55 to +125°C
Package Type E		−40 to +85°C
DC SUPPLY VOLTAGE RANGE, V_{DD} (Voltages referenced to V_{SS} Terminal)		−0.5 to +20 V
POWER DISSIPATION PER PACKAGE:		
For T_A = −40 to +60°C (Package Type E)		500 mW
For T_A = +60 to +85°C (Package Type E)	Derate linearly to	200 mW
For T_A = −55 to +100°C (Package Types D, F, K)		500 mW
For T_A = +100 to +125°C (Package Types D, F, K)	Derate linearly to	200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR		
For T_A = Full Package-Temperature Range (All Package Types)		100 mW
INPUT VOLTAGE RANGE, ALL INPUTS		−0.5 to V_{DD} +0.5 V
CURRENT THROUGH CROSSPOINT		10 mA
LEAD TEMPERATURE (DURING SOLDERING):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.		+265°C

TRUTH TABLE

Address				Select	Address				Select
A	B	C	D		A	B	C	D	
0	0	0	0	X1Y1	0	0	0	1	X1Y3
1	0	0	0	X2Y1	1	0	0	1	X2Y3
0	1	0	0	X3Y1	0	1	0	1	X3Y3
1	1	0	0	X4Y1	1	1	0	1	X4Y3
0	0	1	0	X1Y2	0	0	1	1	X1Y4
1	0	1	0	X2Y2	1	0	1	1	X2Y4
0	1	1	0	X3Y2	0	1	1	1	X3Y4
1	1	1	0	X4Y2	1	1	1	1	X4Y4

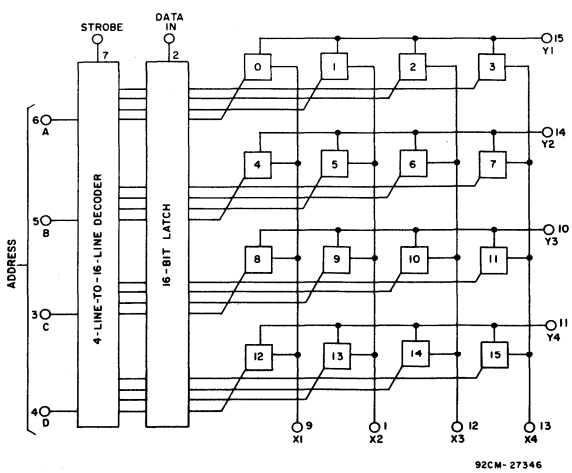


Fig. 1 — Functional diagram.

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	TYPICAL VALUE	UNITS
Quiescent Device Current, I_L	Switches OFF or ON		20	nA
Crosspoint: OFF Leakage Current, I_L	R_L = 10 kΩ		100	pA
ON Resistance, R_{ON}			85	Ω
ΔON Resistance, ΔR_{ON}			5	Ω
Feedthrough Capacitance, C_{IOS}			0.2	pF
Channel Input or Output Capacitance, C_{IS}, C_{OS}		12	30	pF
Control Input Capacitance, C_I			5	pF
Sine Wave Response (Distortion)	f_{IS} = 1 kHz, R_L = 10 kΩ		0.4	%
Feedthrough, Crosspoints OFF	f_{IS} = 1.6 kHz, R_L = 1 kΩ		−95	dB

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	TYPICAL VALUE	UNITS
Propagation Delay Time: Address or Strobe Inputs To Output, t_{PHL}, t_{PLH}	R_L = 10 kΩ, C_L = 50 pF	12	200	ns
Across Crosspoint, t_{PHL}, t_{PLH}			20	ns
Minimum Strobe Pulse Width			80	ns

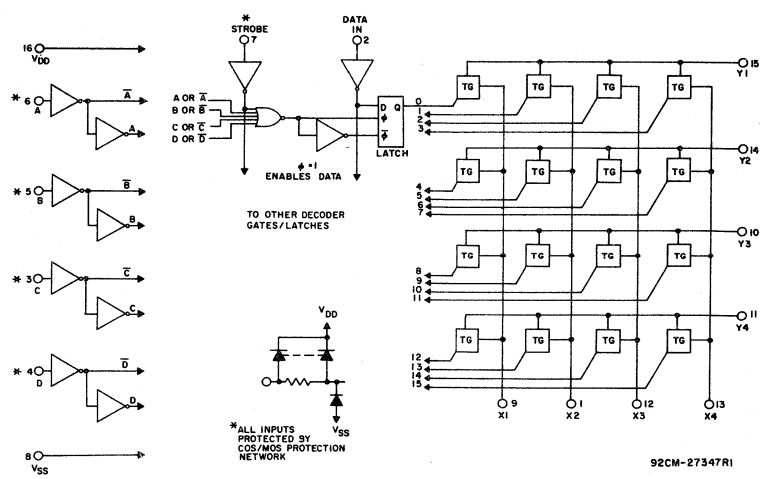


Fig.2 — Logic diagram.

CD22101 CD22102

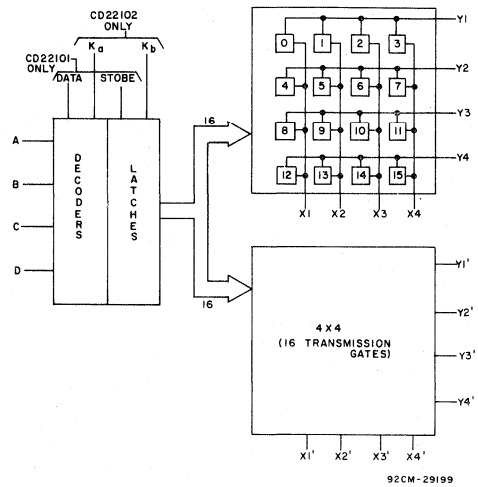
COS/MOS 4x4x2 Crosspoint Switches With Control Memory

Objective Data

The RCA-CD22101 and CD22102 crosspoint switches consist of 4 x 4 x 2 arrays of crosspoints (transmission gates), 4-line to 16-line decoders, and 16 latch circuits. Any one of the sixteen crosspoint pairs can be selected by applying the appropriate four-line address, and any number of crosspoints can be ON simultaneously.

In the CD22101 the selected crosspoint pair can be turned on or off by applying a logical ONE or ZERO, respectively, to the data input, and applying a ONE to the strobe input.

The selected pair of crosspoints in the CD22102 are turned on by applying a logical ONE to the K_a (set) input and turned off by applying a logical ZERO to the K_b (reset) input. In this respect, the control latches of the CD22102 are similar to SET/RESET flip-flops. They differ, however, in that the simultaneous application of ONEs to the K_a and K_b inputs turns off (resets) all crosspoints.



Functional Block Diagram

Features:

- Low ON resistance — 85 Ω typ. at V_{DD} = 12 V
- "Built-in" latched inputs
- Large analog signal capability — ± $V_{DD}/2$
- 10 MHz switch bandwidth
- Matched switch characteristics ΔR_{ON} = 5 Ω typ. at V_{DD} = 12 V
- High linearity — 0.5% distortion (typ.) at f = 1 kHz, V_{IN} = 5 V_{p-p}, $V_{DD} - V_{SS}$ = 10 V, and R_L = 10 kΩ
- Standard COS/MOS noise immunity

Applications:

- Telephone systems
- PBX
- Studio audio switching
- Multisystem bus interconnect

DECODER TRUTH TABLE

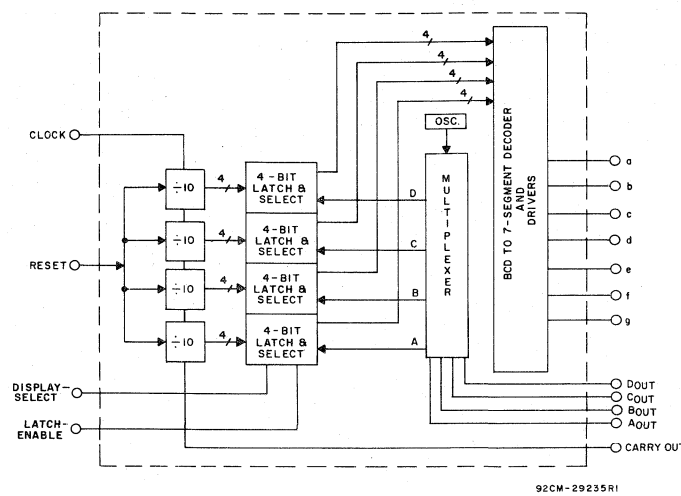
Address				Select	Address				Select
A	B	C	D		A	B	C	D	
0	0	0	0	X1Y1	0	0	0	1	X1Y3
1	0	0	0	X2Y1	1	0	0	1	X2Y3
0	1	0	0	X3Y1	0	1	0	1	X3Y3
1	1	0	0	X4Y1	1	1	0	1	X4Y3
0	0	1	0	X1Y2	0	0	1	1	X1Y4
1	0	1	0	X2Y2	1	0	1	1	X2Y4
0	1	1	0	X3Y2	0	1	1	1	X3Y4
1	1	1	0	X4Y2	1	1	1	1	X4Y4

COS/MOS Counter and 7-Segment Decoder With Multiplexer Driver

Objective Data

The RCA-CD22925,CD22926,CD22927, and CD22928 each consists of a counter, latch and select, 7-segment display with n-p-n output drivers, and a multiplexer/oscillator with outputs. The block diagram is for the CD22926. The CD22925 is the same as the CD22926 but does not have DISPLAY SELECT or CARRY OUT. The CD22927 is identical to the CD22925 except that the second most significant digit divides by 6 rather than 10. The CD22928 is a 3½-digit counter that divides the most significant digit by 2 rather than 10 and the CARRY OUT becomes a latching OVERFLOW.

On all types a high level at the counter input resets the counter to zero and the CARRY OUT to a low level. A transition to a low level at the LATCH ENABLE input latches the number in the output latches. The numbers in the counter and output latch are selected by high and low levels, respectively, at the DISPLAY SELECT input.



CD22926 Functional Block Diagram

Features:

- **High segment-current capability (80 ma typ.) for direct LED drive**
- **Internal multiplexing circuit**
- **High noise immunity**
- **Supply-voltage range of 3 to 6 V**
- **Input protection network similar to CD4049UB (Input signals exceeding V_{DD} will not be clamped)**
- **Input-signal range compatible with COS/MOS B-series standard**

Applications:

- **General-purpose 4-digit or less counter with numeric display**
- **Instrument display driver**
- **Computer/calculator display driver**
- **Clock, watch, and timer applications**

CDP1800-Series Microprocessor Products

Technical Data

CDP1802D, CDP1802CD
COSMAC Microprocessor

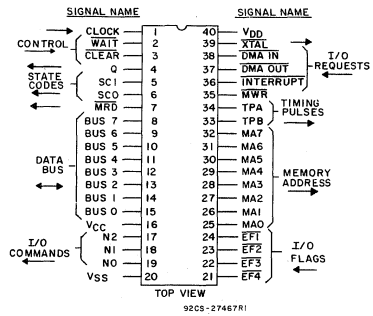
Preliminary Data

The RCA-CDP1802 is an LSI COS/MOS 8-bit register-oriented central-processing unit (CPU) designed for use as a general-purpose computing or control element in a wide range of stored-program systems or products.

The CDP1802 includes all of the circuits required for fetching, interpreting, and executing instructions which have been stored in standard types of memories. Extensive input/output (I/O) control features are also provided to facilitate system design.

The COSMAC architecture is designed with emphasis on the total microcomputer system as an integral entity so that systems having maximum flexibility and minimum cost can be realized. The COSMAC CPU also provides a synchronous interface to memories and external controllers for I/O devices, and minimizes the cost of interface controllers. Furthermore, the I/O interface is capable of supporting devices operating in polled, interrupt-driven, or direct memory-access modes.

The CDP1802D and CD1802D are functionally identical. They differ in that the CDP1802D has a recommended operating voltage range of 3–12 volts, and the CDP1802CD, a recommended operating voltage range of 4–6 volts. These types are supplied in 40-lead dual-in-line ceramic packages (D suffix).



Terminal Assignment for CDP1802

Features:

- **Instruction fetch-execute time of 2.5/3.75 μs at V_{DD} = 10 V; 5/1.5 μs at V_{DD} = 5 V**
- **Compatible with CDP1801 software**
- **Full military-temperature range (–55 to +125°C)**
- **High noise immunity, wide operating-voltage range**
- **Single voltage supply**
- **No minimum clock frequency**
- **Low power**
- **TTL compatible**
- **Single-phase clock; optional on-chip crystal-controlled oscillator**
- **Simple control of reset, run, and pause**
- **8-bit parallel organization with bidirectional data bus**
- **Any combination of standard RAM and ROM**
- **Memory addressing up to 65,536 bytes**
- **Flexible programmed I/O mode**
- **Program interrupt mode**
- **On-chip DMA**
- **Four I/O flag inputs directly tested by branch instructions**
- **Programmable output port**
- **91 easy-to-use instructions**
- **16 x 16 matrix of registers for use as multiple program counters, data pointers, or data registers**

OPERATING CONDITIONS at T_A = 25°C Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	CONDITIONS		TYPICAL VALUES		UNITS
	V_{CC}[1] (V)	V_{DD} (V)	CDP1802D	CDP1802CD	
Supply-Voltage Range (At T_A = Full Package-Temperature Range)	–	–	3 to 12	4 to 6	V
Input Voltage Range	–	–	V_{SS} to V_{CC}	V_{SS} to V_{CC}	V
Maximum Clock Input Rise or Fall Time, t_r or t_f	3-12	3-12	1	1	μs
Instruction Time[2] (See Fig. 3)	5	5	5	5	μs
	5	10	4	–	
	10	10	2.5	–	
Maximum DMA Transfer Rate	5	5	400	400	KBytes/sec
	5	10	500	–	
	10	10	800	–	
Maximum Clock Input Frequency, f_{CL}[3]	5	5	DC–3.2	DC–3.2	MHz
	5	10	DC–4	–	
	10	10	DC–6.4	–	

Notes:

1. $V_{CC} \leqslant V_{DD}$; for CDP1802CD $V_{DD} = V_{CC} = 5$ volts.
2. Equals 2 machine cycles—one Fetch and one Execute operation for all instructions except Long Branch and Long Skip, which require 3 machine cycles—one Fetch and two Execute operations.
3. Load capacitance (C_L) = 500 pF.

MAXIMUM RATINGS,
Absolute-Maximum Values

Storage-Temperature Range (T_{stg}) ..... –65 to +150°C

Operating-Temperature Range (T_A) ..... –55 to +125°C

DC Supply-Voltage Range (V_{CC}, V_{DD})
(All voltage values referenced to V_{SS} terminal)
$V_{CC} \leqslant V_{DD}$:
CDP1802D ..... 0.5 to +15 V
CDP1802CD ..... –0.5 to +7 V

Power Dissipation Per Package (P_D):
For T_A = –55 to +100°C ..... 500 mW
For T_A = +100 to +125°C ..... Derate Linearly to 200 mW

Device Dissipation Per Output Transistor:
For T_A = –55°C to +125°C ..... 100 mW

Input Voltage Range, All Inputs ..... –0.5 to V_{DD} +0.5 V

DC Input Current, Any One Input ..... ±10 mA

Lead Temperature (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

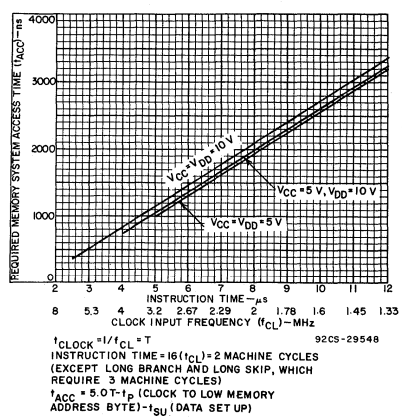


Fig. 1 – Required memory system access time as a function of instruction time.

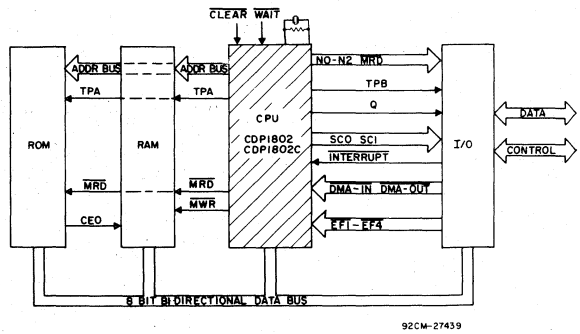


Fig.2 – Typical CDP1802 microprocessor system.

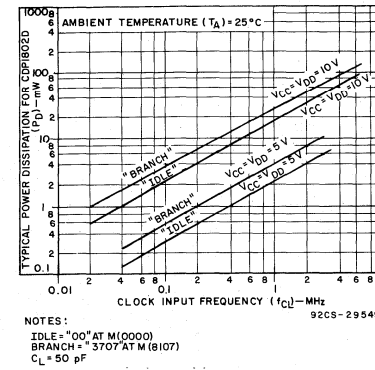


Fig.3 – Typical power dissipation as a function of clock frequency for BRANCH instruction and IDLE instruction for CDP1802D.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
				VALUES				+25			
	V_O (V)	V_{IN} (V)	V_{CC}, V_{DD} (V)	–55	–40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_L Max.	–	–	5	–	–	–	–	–	1	100	μA
	–	–	10	–	–	–	–	–	10	500	
CDP1802D	–	–	15	–	–	–	–	–	–	1000	
CDP1802CD	–	–	5	–	–	–	–	–	–	500	
Output Low Drive (Sink) Current, I_{OL} Min.	0.4	0,5	5	1.98	1.89	1.14	0.90	1.5	2.2	–	mA
(Except $\overline{XTAL}$)	0.5	0,10	10	3.70	3.53	2.13	1.68	2.8	5.2	–	
$\overline{XTAL}$ Output I_{OL} Min.	0.4	5	5	132	126	76	60	100	–	–	μA
Output High Drive (Source Current) I_{OH} Min.	4.6	0,5	5	–0.46	–0.44	–0.27	–0.21	–0.35	–0.51	–	mA
(Except $\overline{XTAL}$)	9.5	0,10	10	–1.12	–1.07	–0.65	–0.51	–0.85	–1.3		
$\overline{XTAL}$ Output I_{OH} Min.	4.6	0	5	66	63	38	30	–50	–	–	μA
Output Voltage Low-Level V_{OL} Max.	–	0,5	5	0.00				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
Output Voltage High Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
Input Low Voltage V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	0.5,4.5	–	5,10	1				–	–	1	
	1,9	–	10	3				–	–	3	
Input High Voltage V_{IL} Max.	0.5,4.5	–	5	3.5				3.5	–	–	
	0.5,4.5	–	5,10	4				4	–	–	
	1,9	–	10	7				7	–	–	
Input Leakage Current I_{IN} Max.	Any Input	0,15	15	±1				–	–	±1	μA
3-State Output Leakage Current I_{OUT} Max.	0,15	0,15	15	±1	±1	±12	±12	–	$\pm 10^{-4}$	±1	μA

ARCHITECTURE

The COSMAC block diagram is shown in Fig. 5. The principal feature of this system is a register array (R) consisting of sixteen 16-bit scratchpad registers. Individual registers in the array (R) are designated (selected) by a 4-bit binary code from one of the 4-bit registers labeled N, P, and X. The contents of any register can be directed to any one of the following three paths:

1. the external memory (multiplexed, higher-order byte first, on to 8 memory address lines);
2. the D register (either of the two bytes can be gated to D);
3. the increment/decrement circuit where it is increased or decreased by one and stored back in the selected 16-bit register.

The three paths, depending on the nature of the instruction, may operate independently or in various combinations in the same machine cycle.

With two exceptions, COSMAC instructions consist of two 8-clock-pulse machine cycles. The first cycle is the fetch cycle, and the second—and third, if necessary—are execute cycles. During the fetch cycle the four bits in the P designator select one of the 16 registers R(P) as the current program counter. The selected register R(P) contains the address of the memory location from which the instruction is to be fetched. When the instruction is read out from the memory, the higher-order 4 bits of the instruction byte are loaded into the I register and the lower-order 4 bits into the N register. The content of the program counter is automatically incremented by one so that R(P) is now "pointing" to the next byte in the memory.

The X designator selects one of the 16 registers R(X) to "point" to the memory for an operand (or data) in certain ALU or I/O operations.

The N designator can perform the following five functions depending on the type of instruction fetched:

1. designate one of the 16 registers in R to be acted upon during register operations;

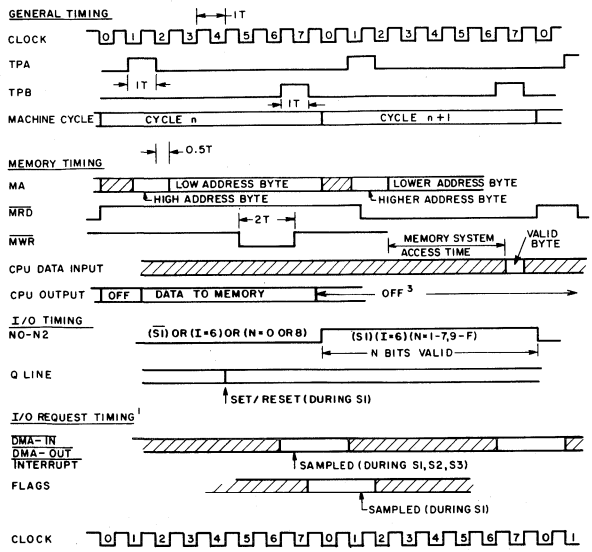


Fig. 4 – Timing diagram.

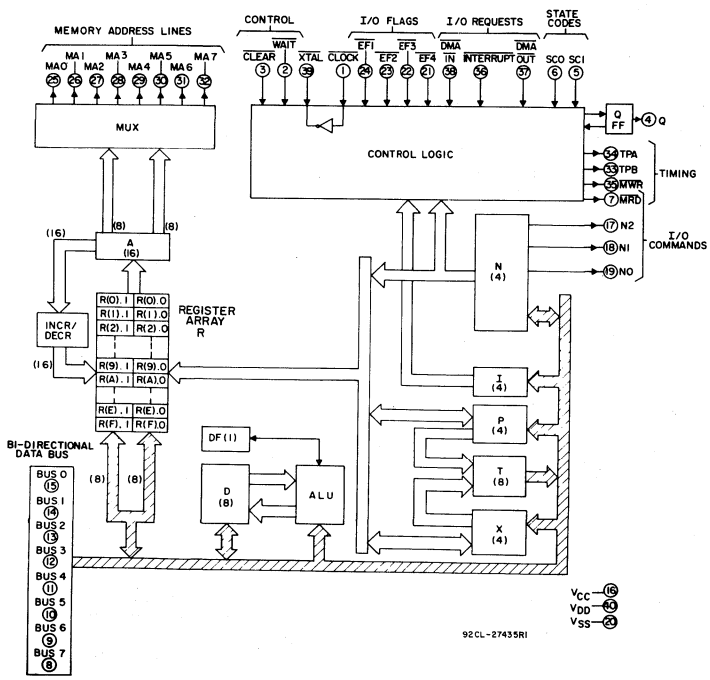


Fig. 5—CDP1802 block diagram.

2. indicate to the I/O devices a command code or device-selection code for peripherals;
3. indicate the specific operation to be executed during the ALU instructions, types of tests to be performed during the Branch instructions, or the specific operation required in a class of miscellaneous instructions (70-73 and 78-7B);
4. indicate the value to be loaded into P to designate a new register to be used as the program counter R(P);
5. indicate the value to be loaded into X to designate a new register to be used as data pointer R(X).

The registers in R can be assigned by a programmer in three different ways: as program counters, as data pointers, or as scratchpad locations (data registers) to hold two bytes of data.

Program Counters

Any register can be the main program counter; the address of the selected register is held in the P designator. Other registers in R can be used as subroutine program counters. By a single instruction the contents of the P register can be changed to effect a "call" to a subroutine. When interrupts are being serviced, register R(1) is used as the program counter for the user's interrupt servicing routine. After reset, and during a DMA operation, R (0) is used as the program counter. At all other times the register designated as program counter is at the discretion of the user.

Data Pointers

The registers in R may be used as data pointers to indicate a location in memory. The register designated by X (i.e., R(X)) points to memory for the following instructions (see Table I):

1. ALU operations F1-F5, F7, 74, 75, 77;
2. output instructions 61 through 67;
3. input instructions 69 through 6F;
4. certain miscellaneous instructions—70-73, 78, 60, F0.

The register designated by N (i.e., R(N)) points to memory for the "load D from memory" instructions 0N and 4N and the "Store D" instruction 5N. The register designated by P (i.e., the program counter) is used as the data pointer for ALU instructions F8-FD, FF, 7C, 7D, 7F. During these instruction executions the operation is referred to as "data immediate".

Another important use of R as a data pointer supports the built-in Direct-Memory-Access (DMA) function. When a DMA-In or DMA-Out request is received, one machine cycle is "stolen". This operation occurs at the end of the execute machine cycle in the current instruction. Register R(0) is always used as the data pointer during the DMA operation. The data is read from (DMA-Out) or written into (DMA-In) the memory location pointed to by the R(0) register. At the end of the transfer, R(0) is incremented by one so that the processor is ready to act upon the next DMA byte transfer request. This feature in the COSMAC architecture saves a substantial

amount of logic when fast exchanges of blocks of data are required, such as with magnetic discs or during CRT-display-refresh cycles.

A program load facility, using the DMA-In channel, is provided to enable users to load programs into the memory. This facility provides a simple, one-step means for initially entering programs into the microprocessor system and eliminates the requirement for specialized "bootstrap" ROM's.

Data Registers

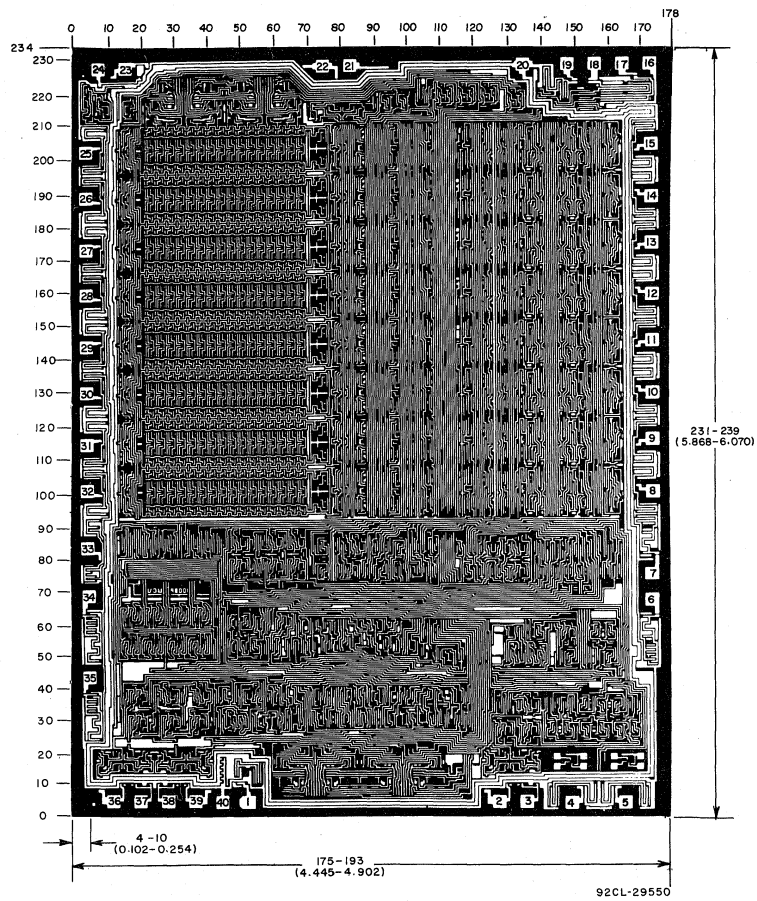
When registers in R are used to store bytes of data, four instructions are provided which allow D to receive from or write into either the higher-order- or lower-order-byte portions of the register designated by N. By this mechanism (together with loading by data immediate) program pointer and data pointer designations are initialized. Also, this technique allows scratchpad registers in R to be used to hold general data. By employing increment or decrement instructions, such registers may be used as loop counters.

The Q Flip Flop

An internal flip flop, Q, can be set or reset by instruction and can be sensed by conditional branch instructions. The output of Q is also available as a microprocessor output.

Interrupt Servicing

Register R(1) is always used as the program counter whenever interrupt servicing is initiated. When an interrupt request comes in and the interrupt is allowed by the program (again, nothing takes place until the completion of the current instruction) the contents of the X and P registers are stored in the temporary register T, and X and P are set to new values; hex digit 2 in X and hex digit 1 in P. Interrupt enable is automatically deactivated to inhibit further interruptions. The user's interrupt routine is now in control; the contents of T may be saved by means of a single instruction (78) in the memory location pointed to by R (X). At the conclusion of the interrupt, the user's routine may restore the pre-interrupted value of X and P with a single instruction (70 or 71). The interrupt-enable flip-flop can be activated to permit further interrupts or can be disabled to prevent them.



Dimensions and pad layout of CDP1802.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

TABLE I – INSTRUCTION SUMMARY
(For Notes, see below)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
MEMORY REFERENCE			
LOAD VIA N	LDN	0N	M(R(N))→D; FOR N NOT 0
LOAD ADVANCE	LDA	4N	M(R(N))→D; R(N) +1
LOAD VIA X	LDX	F0	M(R(X))→D
LOAD VIA X AND ADVANCE	LDXA	72	M(R(X))→D; R(X) +1
LOAD IMMEDIATE	LDI	F8	M(R(P))→D; R(P) +1
STORE VIA N	STR	5N	D→M(R(N))
STORE VIA X AND DECREMENT	STXD	73	D→M(R(X)); R(X) –1
REGISTER OPERATIONS			
INCREMENT REG N	INC	1N	R(N) +1
DECREMENT REG N	DEC	2N	R(N) –1
INCREMENT REG X	IRX	60	R(X) +1
GET LOW REG N	GLO	8N	R(N).0→D
PUT LOW REG N	PLO	AN	D→R(N).0
GET HIGH REG N	GHI	9N	R(N).1→D
PUT HIGH REG N	PHI	BN	D→R(N).1
LOGIC OPERATIONS♦♦			
OR	OR	F1	M(R(X)) OR D→D
OR IMMEDIATE	ORI	F9	M(R(P)) OR D→D; R(P) +1
EXCLUSIVE OR	XOR	F3	M(R(X)) XOR D→D
EXCLUSIVE OR IMMEDIATE	XRI	FB	M(R(P)) XOR D→D; R(P) +1
AND	AND	F2	M(R(X)) AND D→D
AND IMMEDIATE	ANI	FA	M(R(P)) AND D→D; R(P) +1
SHIFT RIGHT	SHR	F6	SHIFT D RIGHT, LSB(D)→DF, 0→MSB(D)
SHIFT RIGHT WITH CARRY	SHRC	76♦	SHIFT D RIGHT, LSB(D)→DF, DF→MSB(D)
RING SHIFT RIGHT	RSHR		
SHIFT LEFT	SHL	FE	SHIFT D LEFT, MSB(D)→DF, 0→LSB(D)
SHIFT LEFT WITH CARRY	SHLC	7E♦	SHIFT D LEFT, MSB(D)→DF, DF→LSB(D)
RING SHIFT LEFT	RSHL		
ARITHMETIC OPERATIONS♦♦			
ADD	ADD	F4	M(R(X)) +D→DF, D
ADD IMMEDIATE	ADI	FC	M(R(P)) +D→DF, D; R(P) +1
ADD WITH CARRY	ADC	74	M(R(X)) +D +DF→DF, D
ADD WITH CARRY, IMMEDIATE	ADCI	7C	M(R(P)) +D +DF→DF, D R(P) +1
SUBTRACT D	SD	F5	M(R(X))–D→DF, D
SUBTRACT D IMMEDIATE	SDI	FD	M(R(P))–D→DF, D; R(P) +1
SUBTRACT D WITH BORROW	SDB	75	M(R(X))–D–(NOT DF)→DF, D
SUBTRACT D WITH BORROW, IMMEDIATE	SDBI	7D	M(R(P))–D–(NOT DF)→DF, D; R(P) +1
SUBTRACT MEMORY	SM	F7	D–M(R(X))→DF, D
SUBTRACT MEMORY IMMEDIATE	SMI	FF	D–M(R(P))→DF, D; R(P) +1
SUBTRACT MEMORY WITH BORROW	SMB	77	D–M(R(X))–(NOT DF)→DF, D
SUBTRACT MEMORY WITH BORROW, IMMEDIATE	SMBI	7F	D–M(R(P))–(NOT DF)→DF, D R(P) +1
BRANCH INSTRUCTIONS–SHORT BRANCH			
SHORT BRANCH	BR	30	M(R(P))→R(P).0
NO SHORT BRANCH (SEE SKP)	NBR	38♦	R(P) +1
SHORT BRANCH IF D=0	BZ	32	IF D=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF D NOT 0	BNZ	3A	IF D NOT 0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF DF=1	BDF	33♦	IF DF=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF POS OR ZERO	BPZ		
SHORT BRANCH IF EQUAL OR GREATER	BGE		
SHORT BRANCH IF DF=0	BNF	3B♦	IF DF=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF MINUS	BM		
SHORT BRANCH IF LESS	BL		
SHORT BRANCH IF Q=1	BQ	31	IF Q=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF Q=0	BNQ	39	IF Q=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF1=1 1 = V_{SS}	B1	34	IF EF1=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF1=0 0 = V_{CC}	BN1	3C	IF EF1=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF2=1 1 = V_{SS}	B2	35	IF EF2=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF2=0 0 = V_{CC}	BN2	3D	IF EF2=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF3=1 1 = V_{SS}	B3	36	IF EF3=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF3=0 0 = V_{CC}	BN3	3E	IF EF3=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF4=1 1 = V_{SS}	B4	37	IF EF4=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF4=0 0 = V_{CC}	BN4	3F	IF EF4=0, M(R(P))→R(P).0 ELSE R(P) +1

INSTRUCTION SUMMARY (CONT'D)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
BRANCH INSTRUCTIONS–LONG BRANCH			
LONG BRANCH	LBR	C0	M(R(P))→R(P).1 M(R(P) +1)→R(P).0
NO LONG BRANCH (SEE LSKP)	NLBR	C8♦	R(P) +2
LONG BRANCH IF D=0	LBZ	C2	IF D=0, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2
LONG BRANCH IF D NOT 0	LBNZ	CA	IF D NOT 0, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2
LONG BRANCH IF DF=1	LBDF	C3	IF DF=1, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2
LONG BRANCH IF DF=0	LBNF	CB	IF DF=0, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2
LONG BRANCH IF Q=1	LBQ	C1	IF Q=1, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2
LONG BRANCH IF Q=0	LBNQ	C9	IF Q=0, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2
SKIP INSTRUCTIONS			
SHORT SKIP (SEE NBR)	SKP	38♦	R(P) +1
LONG SKIP (SEE NLBR)	LSKP	C8♦	R(P) +2
LONG SKIP IF D=0	LSZ	CE	IF D=0, R(P) +2 ELSE CONTINUE
LONG SKIP IF D NOT 0	LSNZ	C6	IF D NOT 0, R(P) +2 ELSE CONTINUE
LONG SKIP IF DF=1	LSDF	CF	IF DF=1, R(P) +2 ELSE CONTINUE
LONG SKIP IF DF=0	LSNF	C7	IF DF=0, R(P) +2 ELSE CONTINUE
LONG SKIP IF Q=1	LSQ	CD	IF Q=1, R(P) +2 ELSE CONTINUE
LONG SKIP IF Q=0	LSNQ	C5	IF Q=0, R(P) +2 ELSE CONTINUE
LONG SKIP IF IE=1	LSIE	CC	IF IE=1, R(P) +2 ELSE CONTINUE
CONTROL INSTRUCTIONS			
IDLE	IDL	00#	WAIT FOR DMA OR INTERRUPT; M(R(0))→BUS
NO OPERATION	NOP	C4	CONTINUE
SET P	SEP	DN	N→P
SET X	SEX	EN	N→X
SET Q	SEQ	7B	1→Q
RESET Q	REQ	7A	0→Q
SAVE	SAV	78	T→M(R(X))
PUSH X,P TO STACK	MARK	79	(X,P)→T; (X,P)→M(R(2)) THEN P→X; R(2)–1
RETURN	RET	70	M(R(X))→(X,P); R(X) +1 1→IE
DISABLE	DIS	71	M(R(X))→(X,P); R(X) +1 0→IE
INPUT–OUTPUT BYTE TRANSFER			
OUTPUT 1	OUT 1	61	M(R(X))→BUS; R(X) +1; N LINES = 1
OUTPUT 2	OUT 2	62	M(R(X))→BUS; R(X) +1; N LINES = 2
OUTPUT 3	OUT 3	63	M(R(X))→BUS; R(X) +1; N LINES = 3
OUTPUT 4	OUT 4	64	M(R(X))→BUS; R(X) +1; N LINES = 4
OUTPUT 5	OUT 5	65	M(R(X))→BUS; R(X) +1; N LINES = 5
OUTPUT 6	OUT 6	66	M(R(X))→BUS; R(X) +1; N LINES = 6
OUTPUT 7	OUT 7	67	M(R(X))→BUS; R(X) +1; N LINES = 7
INPUT 1	INP 1	69	BUS→M(R(X)); BUS→D; N LINES = 1
INPUT 2	INP 2	6A	BUS→M(R(X)); BUS→D; N LINES = 2
INPUT 3	INP 3	6B	BUS→M(R(X)); BUS→D; N LINES = 3
INPUT 4	INP 4	6C	BUS→M(R(X)); BUS→D; N LINES = 4
INPUT 5	INP 5	6D	BUS→M(R(X)); BUS→D; N LINES = 5
INPUT 6	INP 6	6E	BUS→M(R(X)); BUS→D; N LINES = 6
INPUT 7	INP 7	6F	BUS→M(R(X)); BUS→D; N LINES = 7

♦NOTE: THIS INSTRUCTION IS ASSOCIATED WITH MORE THAN ONE MNEMONIC. EACH MNEMONIC IS INDIVIDUALLY LISTED.

♦♦NOTE: THE ARITHMETIC OPERATIONS AND THE SHIFT INSTRUCTIONS ARE THE ONLY INSTRUCTIONS THAT CAN ALTER THE DF.
AFTER AN ADD INSTRUCTION:
DF = 1 DENOTES A CARRY HAS OCCURRED
DF = 0 DENOTES A CARRY HAS NOT OCCURRED
AFTER A SUBTRACT INSTRUCTION:
DF = 1 DENOTES NO BORROW. D IS A TRUE POSITIVE NUMBER
DF = 0 DENOTES A BORROW. D IS TWO'S COMPLEMENT
THE SYNTAX "–(NOT DF)" DENOTES THE SUBTRACTION OF THE BORROW

#An idle instruction initiates a repeating S1 cycle. The processor will continue to idle until an I/O request (INTERRUPT, DMA-IN, or DMA-OUT) is activated. When the request is acknowledged, the IDLE cycle is terminated and the I/O request is serviced, and then normal operation is resumed.

♦NOTE: THIS INSTRUCTION IS ASSOCIATED WITH MORE THAN ONE MNEMONIC. EACH MNEMONIC IS INDIVIDUALLY LISTED.

1. Long-Branch, Long-Skip and No Op instructions are the only instructions that require three cycles to complete (1 fetch + 2 execute).

   Long-Branch instructions are three bytes long. The first byte specifies the condition to be tested; and the second and third byte, the branching address.

   The long-branch instructions can:
   a) Branch unconditionally
   b) Test for D=0 or D≠0
   c) Test for DF=0 or DF=1
   d) Test for Q=0 or Q=1
   e) effect an unconditional no branch

   If the tested condition is met, then branching takes place; the branching address bytes are loaded in the high-and-low-order bytes of the current program counter, respectively. This operation effects a branch to any memory location.

   If the tested condition is not met, the branching address bytes are skipped over, and the next instruction in sequence is fetched and executed. This operation is taken for the case of unconditional no branch (NLBR).

2. The short-branch instructions are two bytes long. The first byte specifies the condition to be tested, and the second specifies the branching address.

   The short-branch instructions can:
   a) Branch unconditionally
   b) Test for D=0 or D≠0
   c) Test for DF=0 or DF=1
   d) Test for Q=0 or Q=1
   e) Test the status (1 or 0) of the four EF flags
   f) Effect an unconditional no branch

   If the tested condition is met, then branching takes place; the branching address byte is loaded into the low-order byte position of the current program counter. This effects a branch with the current 256-byte page of the memory, i.e., the page which holds the branching address. If the tested condition is not met, the branching address byte is skipped over, and the next instruction in sequence is fetched and executed. This same action is taken in the case of unconditional no branch (NBR)

3. The skip instructions are one byte long. There is one Unconditional Short-Skip (SKP) and eight Long-Skip instructions.

   The Unconditional Short-Skip instruction takes 2 cycles to complete (1 fetch + 1 execute). Its action is to skip over the byte following it. Then the next instruction in sequence is fetched and executed. This SKP instruction is identical to the unconditional no-branch instruction (NBR) except that the skipped-over byte is not considered part of the program.

   The Long-Skip instructions take three cycles to complete (1 fetch + 2 execute).

   They can:
   a) Skip unconditionally
   b) Test for D=0 or D≠0
   c) Test for DF=0 or DF=1
   d) Test for Q=0 or Q=1
   e) Test for IE=1

   If the tested condition is met, then Long Skip takes place; the current program counter is incremented twice. Thus two bytes are skipped over and the next instruction in sequence is fetched and executed. If the tested condition is not met, then no action is taken. Execution is continued by fetching the next instruction in sequence.

COSMAC Register Summary

D	8 Bits	Data Register (Accumulator)
DF	1 Bit	Data Flag (ALU Carry)
R	16 Bits	1 of 16 Scratchpad Registers
P	4 Bits	Designates which register is Program Counter
X	4 Bits	Designates which register is Data Pointer

N	4 Bits	Holds Low-Order Instr. Digit
I	4 Bits	Holds High-Order Instr. Digit
T	8 Bits	Holds old X, P after Interrupt (X is high byte)
IE	1 Bit	Interrupt Enable
Q	1 Bit	Output Flip Flop

INSTRUCTION SET

The COSMAC instruction summary is given in Table I. Hexadecimal notation is used to refer to the 4-bit binary codes.

In all registers bits are numbered from the least significant bit (LSB) to the most significant bit (MSB) starting with 0.

R(W): Register designated by W, where W=N or X, or P

R(W).0: Lower-order byte of R(W)
R(W).1: Higher-order byte of R(W)
N0 = Least significant Bit of N Register

Operation Notation
M(R(N)) →D; R(N) + 1

This notation means: The memory byte pointed to by R(N) is loaded into D, and R(N) is incremented by 1.

SIGNAL DESCRIPTIONS

BUS 0 to BUS 7 (Data Bus)

8-bit directional DATA BUS lines. These lines are used for transferring data between the memory, the microprocessor, and I/O devices.

N0 to N2 (I/O Lines)

Activated by an I/O instruction to signal the I/O control logic of a data transfer between memory and I/O interface. These lines can be used to issue command codes or device selection codes to the I/O devices (independently or combined with the memory byte on the data bus when an I/O instruction is being executed). The N bits are low at all times except when an I/O instruction is being executed. During this time their state is the same as the corresponding bits in the N register.

The direction of data flow is defined in the I/O instruction by bit N3 (internally) and is indicated by the level of the MRD signal.

$\overline{MRD} = V_{CC}$: Data from I/O to CPU and Memory

$\overline{MRD} = V_{SS}$: Data from Memory to I/O

$\overline{EF1}$ to $\overline{EF4}$ (4 Flags)

These inputs enable the I/O controllers to transfer status information to the processor. The levels can be tested by the conditional branch instructions. They can be used in conjunction with the INTERRUPT request line to establish interrupt priorities. These flags can also be used by I/O devices to "call the attention" of the processor, in which case the program must routinely test the status of these flag(s). The flag(s) are sampled at the beginning of every S1 cycle.

SIGNAL DESCRIPTION (Cont'd)

$\overline{\text{INTERRUPT}}$, $\overline{\text{DMA-IN}}$, $\overline{\text{DMA-OUT}}$ (3 I/O Requests)

These inputs are sampled by the CDP1802 during the interval between the leading edge of TPB and the leading edge of TPA.

Interrupt Action: X and P are stored in T after executing current instruction; designator X is set to 2; designator P is set to 1; interrupt enable is reset to 0 (inhibit); and instruction execution is resumed. The interrupt action requires one machine cycle (S3).

DMA Action: Finish executing current instruction; R(0) points to memory area for data transfer; data is loaded into or read out of memory; and increment R(0).

Note: In the event of concurrent DMA and INTERRUPT requests, DMA-IN has priority followed by DMA-OUT and then INTERRUPT.

SC0, SC1, (2 State Code Lines)

These outputs indicate that the CPU is: 1 fetching an instruction, or 2) executing an instruction, or 3) processing a DMA request, or 4) acknowledging an interrupt request. The levels of state code are tabulated below. All states are valid at TPA. H = V_{CC}, L = V_{SS}.

State Type	State Code Lines	
	SC1	SC0
S0 (Fetch)	L	L
S1 (Execute)	L	H
S2 (DMA)	H	L
S3 (Interrupt)	H	H

TPA, TPB (2 Timing Pulses)

Positive pulses that occur once in each machine cycle (TPB follows TPA). They are used by I/O controllers to interpret codes and to time interaction with the data bus. The trailing edge of TPA is used by the memory system to latch the higher-order byte of the 16-bit memory address. TPA is suppressed in IDLE when the CPU is in the load mode.

MA0 to MA7 (8 Memory Address Lines)

The higher-order byte of a 16-bit COSMAC memory address appears on the memory address lines MA0-7 first. Those bits required by the memory system may be strobed into external address latches by timing pulse TPA. The low-order byte of the 16-bit address appears on the address lines after the termination of TPA. Latching of all 8 higher-order address bits would permit a memory system of 64K bytes.

$\overline{\text{MWR}}$ (Write Pulse)

A negative pulse appearing in a memory-write cycle, after the address lines have stabilized.

$\overline{\text{MRD}}$ (Read Level)

A low level on $\overline{\text{MRD}}$ indicates a memory read cycle. It can be used to control three-state outputs from the addressed memory which may have a common data input and output bus. If a memory **does** not have a three-state high-impedance output, $\overline{\text{MRD}}$ is useful for driving memory/bus separator gates. It is also used to indicate the direction of data transfer during an I/O instruction.

Q

Single bit output from the CPU which can be set or reset under program control. During SEQ or REQ instruction execution, Q is set or reset between the trailing edge of TPA and the leading edge of TPB.

CLOCK

Input for externally generated single-phase clock. A typical clock frequency is 6.4 MHz at V_{CC} = V_{DD} = 10 volts. The clock is counted down internally to 8 clock pulses per machine cycle.

$\overline{\text{XTAL}}$

Connection to be used with clock input terminal, for an external crystal, if the on-chip oscillator is utilized. The crystal is connected between terminals 1 and 39 (CLOCK and $\overline{\text{XTAL}}$) in parallel with a resistance (10 megohms typ.). Frequency trimming capacitors may be required at terminals 1 and 39. For additional information see ICAN-6565.

SIGNAL DESCRIPTION (Cont'd)

$\overline{WAIT}$, $\overline{CLEAR}$ (2 Control Lines)

Provide four control modes as listed in the following truth table:

$\overline{CLEAR}$	$\overline{WAIT}$	MODE
L	L	Load
L	H	Reset
H	L	Pause
H	H	Run

The function of the modes are defined as follows:

Load

Holds the CPU in the IDLE execution state and allows an I/O device to load the memory without the need for a "bootstrap" loader. It modifies the IDLE condition so that DMA-IN operation does not force execution of the next instruction.

Reset

Registers I, N, Q are reset, IE is set and 0's (V_{SS}) are placed on the data bus. TPA and TPB are suppressed while reset is held and the CPU is placed in S1. The first machine cycle after termination of reset is an ilitialization cycle which requires 9 clock pulses. During this cycle the CPU remains in S1 and registers X, P, and R(0) are reset. Interrupt and DMA servicing are suppressed during the initialization cycle.

The next cycle is an S0, S1, or an S2 but never an S3. With the use of a 71 instruction followed by 00 at memory locations 0000 and 0001, this feature may be used to reset IE, so as to preclude interrupts until ready for them. Power-up reset can be realized by connecting a buffered RC network to $\overline{CLEAR}$. For additional information see ICAN-6581.

Pause

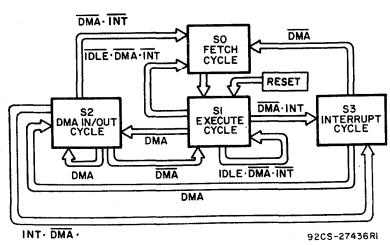
Stops the internal CPU timing generator on the first negative high-to-low transition of the input clock. The oscillator continues to operate, but subsequent clock transitions are ignored.

Run

May be initiated from the Pause or Reset mode functions. If initiated from Pause, the CPU resumes operation on the first negative high-to-low transition of the input clock. When initiated from the Reset operation, the first machine cycle following Reset is always the initialization cycle. The initialization cycle is then followed by a DMA (S2) cycle or fetch (S0) from location 0000 in memory.

V_{DD}, V_{SS}, V_{CC} (Power Levels)

The internal voltage supply V_{DD} is isolated from the Input/Output voltage supply V_{CC} so that the processor may operate at maximum speed while interfacing with various external circuit technologies, including T^2L at 5 volts. V_{CC} must be less than or equal to V_{DD}. All outputs swing from V_{SS} to V_{CC}. The recommended input voltage swing is V_{SS} to V_{CC}.



The CDP1802 and CDP1802C CPU state transitions when in the RUN mode are shown in Fig. 6. Each machine cycle requires the same period of time—8 clock pulses except the initialization cycle, which requires 9 clock pulses. The execution of an instruction requires either two or three machine cycles. S0 followed by a single S1 cycle or two S1 cycles. S2 is the response to a DMA request and S3 is the interrupt request.

CDP1821SD, CDP1821SCD

1024-Word x 1-Bit Static Random-Access Memory

Preliminary Data

The RCA-CDP1821SD and CDP1821SCD are 1024-word x 1-bit COS/MOS silicon-on-sapphire (SOS), fully static, random-access memories for use in CDP1800 microprocessor systems.

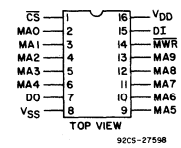
The output state of the CDP1821S is a function of the input address and chip-select states only. Valid data will appear at the output in one access time following the latest address change to a selected chip. After valid data appears, the address may then be changed immediately. It is not necessary to clock the chip-select input or any other input terminal for fully static operation; therefore, the chip-select input may be used as an additional address input. When the device is in an unselected state ($\overline{CS}$=1), the internal write circuitry and output sense amplifier are disabled. This feature allows the three-state data outputs from many arrays to be OR-tied to a common bus for ease of memory expansion.

The CDP1821SD is functionally identical to the CDP1821SCD. The CDP1821SD has a recommended operating voltage range of 4 to 10 volts, and the CDP1821SCD has a recommended operating voltage range of 4 to 6 volts.

The CDP1821SD and CDP1821SCD are supplied in 16-lead, hermetic, dual-in-line ceramic packages.

Features:

- **Static COS/MOS Silicon-On-Sapphire circuitry—CD4000-series compatible**
- **Compatible with CDP1800—series microprocessors at maximum speed**
- **Fast access time:**
  350 ns typ. at V_{DD} = 5 V;
  200 ns typ. at V_{DD} = 10 V
- **Single voltage supply**
- **No precharge or external clocks required**
- **Low quiescent and operating power**
- **Separate data inputs and outputs**



Terminal Assignment

MAXIMUM RATINGS,
Absolute-Maximum Values

Storage-Temperature Range (T_{stg}) ..... −65 to +150°C

Operating-Temperature Range (T_A) ..... −20 to +85°C

DC Supply-Voltage Range (V_{DD}-V_{SS}):

CDP1821SD ..... −0.5 to +11 V

CDP1821SCD ..... −0.5 to +7 V

Input Voltage Range, All Inputs ..... −0.5 to V_{DD} +0.5 V

Lead Temperature (During Soldering):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATIONAL MODES

Mode	Input		Output
	$\overline{MRD}$	$\overline{CS}$	DO
Standby	X	1	High-Impedance
WRITE	0	0	High-Impedance
READ	1	0	Data

OPERATING CONDITIONS at T_A=25°C Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	Conditions V_{DD} (V)	LIMITS CDP1821SD Min.	CDP1821SD Max.	CDP1821SCD Min.	CDP1821SCD Max.	UNITS
Supply-Voltage Range (At T_A=Full Package-Temperature Range)	–	4	10	4	6	V
Recommended Input Voltage Range	–	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Input Signal Rise and Fall Time t_r,t_f	–	–	5	–	5	μs

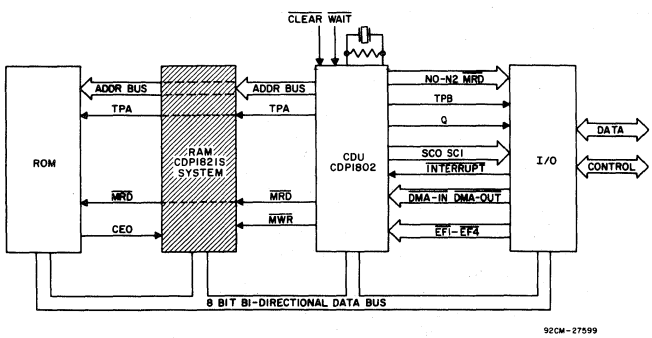
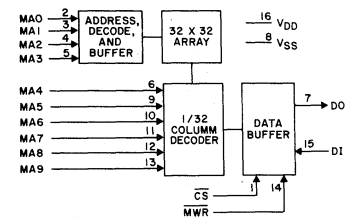
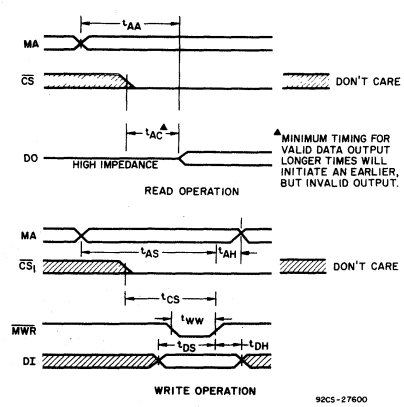


Fig. 1—Typical CDP1802 microprocessor system.



Functional Diagram



Timing Diagrams

ELECTRICAL CHARACTERISTICS at T_A=25°C

CHARACTERISTIC	TEST CONDITIONS			LIMITS		UNITS
				CDP1821SD	CDP1821SCD	
		V_O (V)	V_{DD} (V)	TYPICAL VALUES	TYPICAL VALUES	
Static						
Quiescent Device Current, I_L		–	5	100	500	μA
		–	10	500	–	
Total Power Dissipation, P_D at 1 μs cycle		–	5	5	8	mW
		–	10	20	–	
Output Voltage: Low-Level, V_{OL}		–	5-10	0.01	0.01	V
High-Level, V_{OH}		–	5	4.99	4.99	
		–	10	9.99	–	
Noise Margin: V_{NML}	Any Input	0.5	5	1	1	V
		1	10	1.5	–	
V_{NMH}	Any Input	4.5	5	1	1	
		9	10	1.5	–	
Output Drive Current: N-Channel (Sink), I_DN	Any Output	0.4	5	2	2	mA
		0.5	10	3.5	–	
P-Channel (Source), I_DP	Any Output	4.6	5	–1	–1	
		9.5	10	–15	–	
Data Output Off-Resistance, R_O(Off)	$\overline{CS}$ = H	–	5-10	5	5	MΩ
Input Leakage, I_{IL}, I_{IH}	Any Input	–	5-10	±1	±1	μA
Dynamic: t_r, t_f=10 ns, C_L=50 pF						
Read Operation						
Access Time From Address Change, t_{AA}		–	5	350	350	ns
		–	10	200	–	
Access Time From Chip Select, t_{AC}		–	5	250	250	ns
		–	10	150	–	
Write Operation						
Write Pulse Width, t_{WW}		–	5	150	150	ns
		–	10	100	–	
Data Setup Time, t_{DS}		–	5	150	150	ns
		–	10	100	–	
Data Hold Time, t_{DH}		–	5	100	100	ns
		–	10	50	–	
Chip Select Setup Time, t_{CS}		–	5	250	250	ns
		–	10	150	–	
Address Setup Time, t_{AS}		–	5	200	200	ns
		–	10	150	–	
Address Hold Time, t_{AH}		–	5	100	100	ns
		–	10	50	–	
Capacitance						
Input/Output, C_I/C_O		–	–	5	5	pF

Note:
The dynamic characteristics and timing diagrams indicate maximum performance capability of the CDP1821S. When used directly with the CDP1802 microprocessor, timing will be determined by the clock frequency and internal delays of the microprocessor.

The following general timing relationships will hold when the CDP1821S is used with the CDP1802 microprocessor:

$t_{WW} = 2\ t_c$

$t_{AH} = 1.0\ t_c$

$t_{AS} = 4.5\ t_c$

$t_{DH} = 1.0\ t_c$ } Data transfers from

$t_{DS} = 5.5\ t_c$ } CDP1802 to memory

$\overline{MRD}$ occurs one clock period (t_c) earlier than the address bits MA0-MA7.

where $t_c = \frac{1}{\text{CDP1802 clock frequency}}$

The CDP1821S is capable of operating at the maximum clock frequency of the CDP1802 microprocessor.

CDP1822SD, CDP1822SCD

256-Word x 4-Bit Static Random-Access Memory

Preliminary Data

The RCA-CDP1822SD and CDP1822SCD are 256-word x 4-bit COS/MOS SOS static random-access memories. These memories are compatible with the CDP1802 and will interface directly without additional components.

The CDP1822S has separate inputs and data outputs and is operated from a single voltage supply. Two Chip-Select inputs, of opposite polarity, are provided to simplify system expansion. The $\overline{MRD}$ signal (output disable control) provides WIRE-OR capability and is also useful in common input/output systems.

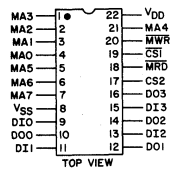
After valid data appears at the output, the address inputs may be changed immediately. This output data will be valid until either the $\overline{MRD}$ signal goes high or the device is de-selected ($\overline{CS1}$=H or CS2=L).

The CDP1822SD is functionally identical to the CDP1822SCD. The CDP1822SD has a recommended operating voltage range of 4 to 10 volts, and the CDP1822SCD has a recommended operating voltage range of 4 to 6 volts.

The CDP1822SD and CDP1822SCD are supplied in 22-lead, hermetic, dual-in-line ceramic packages.

Features:

- Static COS/MOS Silicon-On-Sapphire circuitry—CD4000-series compatible
- Compatible with CDP1800-series microprocessors at maximum speed
- Interfaces with CDP1802 microprocessor without additional components
- Fast access time:
  350 ns typ. at V_{DD} = 5 V;
  100 ns typ. at V_{DD} = 10 V
- Single voltage supply
- Separate data inputs and outputs
- Two-chip select inputs to simplify memory system expansion
- Output disable to allow common I/O system



Terminal Assignment

MAXIMUM RATINGS, *Absolute-Maximum Values*

Storage-Temperature Range (T_{stg}) ..... −65 to +150°C

Operating-Temperature Range (T_A) ..... −20 to +85°C

DC Supply-Voltage Range (V_{DD})
(All voltages referenced to V_{SS} terminal)
CDP1822SD ..... −0.5 to +11 V
CDP1822SCD ..... −0.5 to +7 V

Input Voltage Range, All Inputs ..... −0.5 to V_{DD} +0.5 V

Lead Temperature (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A=25°C Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	Conditions V_{DD} (V)	LIMITS CDP1822SD Min.	CDP1822SD Max.	CDP1822SCD Min.	CDP1822SCD Max.	UNITS
Supply-Voltage Range (At T_A=Full Package-Temperature Range)	–	4	10	4	6	V
Recommended Input Voltage Range	–	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Input Signal Rise and Fall Time, t_r,t_f	–	–	5	–	5	μs

OPERATIONAL MODES

Function	$\overline{MWR}$	$\overline{CS1}$	CS2	$\overline{MRD}$	Data Out DO
READ	1	0	1	0	Storage State of Addressed Cell
WRITE (Output Disabled)	0	0	1	1	High-Impedance
WRITE	0	0	1	0	New Data In State
Standby	X	1	X	X	High-Impedance
	X	X	0	X	High-Impedance
	1	0	1	1	High-Impedance

Logic 1 = High Logic 0 = Low X = Don't Care

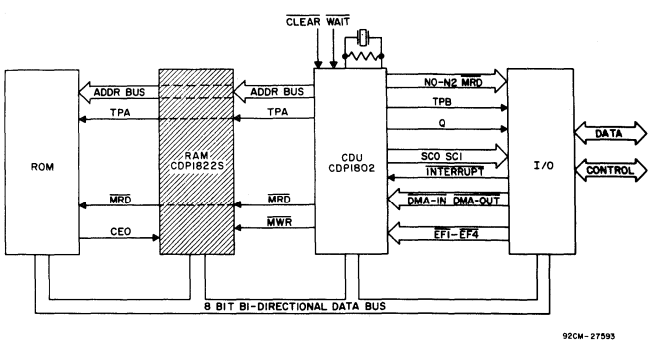
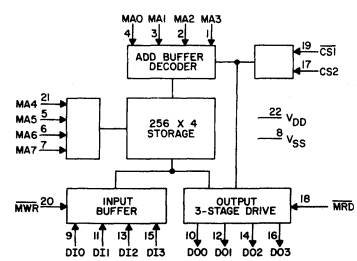


Fig. 1—Typical CDP1802 microprocessor system.

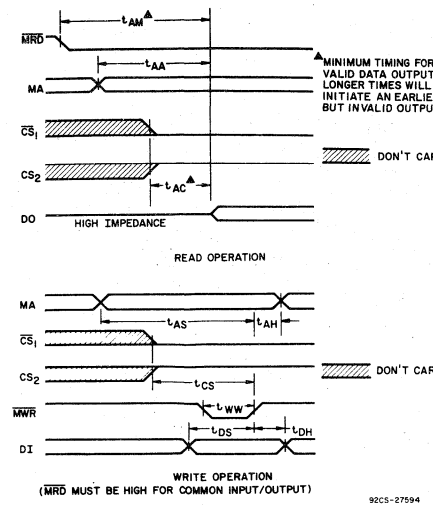


Functional Diagram

92CS-27595

ELECTRICAL CHARACTERISTICS at T_A=25°C

CHARACTERISTIC	TEST CONDITIONS			LIMITS		UNITS
				CDP1822SD	CDP1822SCD	
		V_O (V)	V_{DD} (V)	TYPICAL VALUES	TYPICAL VALUES	
Static						
Quiescent Device Current, I_L		–	5	100	500	μA
		–	10	500	–	
Total Power Dissipation, P_D, at 1 μs cycle		–	5	8	10	mW
		–	10	35	–	
Output Voltage: Low-Level, V_{OL}		–	5-10	0.01	0.01	V
High-Level, V_{OH}		–	5	4.99	4.99	
		–	10	9.99	–	
Noise Margin: V_{NML}	Any Input	0.5	5	1	1	V
		1	10	1.5	–	
V_{NMH}	Any Input	4.5	5	1	1	
		9	10	1.5	–	
Output Drive Current: N-Channel (Sink), I_DN	Any Output	0.4	5	0.8	0.8	mA
		0.5	10	1.8	–	
P-Channel (Source), I_DP	Any Output	4.6	5	–0.8	–0.8	
		9.5	10	–1.8	–	
Data Output Off-Resistance, R_O(Off)	$\overline{MRD}$ = H	–	5-10	5	5	MΩ
Input Leakage, I_{IL}, I_{IH}	Any Input	–	5-10	1	1	μA
Dynamic: t_r,t_f=10 ns, C_L=50 pF						
Read Operation						
Access Time From Address Change, t_{AA}		–	5	350	350	ns
		–	10	200	–	
Access Time From Chip Select, t_{AC}		–	5	250	250	ns
		–	10	150	–	
Output Active From $\overline{MRD}$, t_{AM}		–	5	250	250	ns
		–	10	150	–	
Write Operation						
Write Pulse Width, t_{WW}		–	5	150	150	ns
		–	10	100	–	
Data Setup Time, t_{DS}		–	5	150	150	ns
		–	10	100	–	
Data Hold Time, t_{DH}		–	5	100	100	ns
		–	10	50	–	
Chip Select Setup Time, t_{CS}		–	5	250	250	ns
		–	10	150	–	
Address Setup Time, t_{AS}		–	5	200	200	ns
		–	10	150	–	
Address Hold Time, t_{AH}		–	5	100	100	ns
		–	10	50	–	
Capacitance						
Input/Output, C_I/C_O		–	–	5	5	pF



Timing Diagrams

Note:
The dynamic characteristics and timing diagrams indicate maximum performance capability of the CDP1822S. When used directly with the CDP1802 microprocessor, timing will be determined by the clock frequency and internal delays of the microprocessor.

The following general timing relationships will hold when the CDP1822S is used with the CDP1802 microprocessor:

$t_{WW} = 2\ t_c$

$t_{AH} = 1.0\ t_c$

$t_{AS} = 4.5\ t_c$

$t_{DH} = 1.0\ t_c$, $t_{DS} = 5.5\ t_c$ } Data transfers from CDP1802 to memory

$\overline{MRD}$ occurs one clock period (t_c) earlier than the address bits MA0-MA7.

where $t_c = \frac{1}{\text{CDP1802 clock frequency}}$

The CDP1822S is capable of operating at the maximum clock frequency of the CDP1802 microprocessor.

CDP1823SD, CDP1823SCD

128-Word x 8-Bit Static Random-Access Memory

Preliminary Data

Features:

- **Static COS/MOS Silicon-On-Sapphire circuitry—CD4000-series compatible**
- **Compatible with CDP1800-series microprocessors at maximum speed**
- **Interfaces with CDP1802 microprocessor without additional components**
- **Fast access time:**
  350 ns typ. at V_{DD} = 5 V;
  200 ns typ. at V_{DD} = 10 V
- **Single voltage supply**
- **Common data inputs and outputs**
- **Multiple-chip select inputs to simplify memory system expansion**

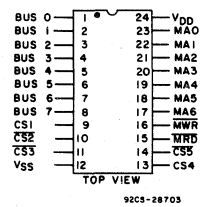
The RCA-CDP1823SD and CDP1823SCD are 128-word x 8-bit COS/MOS SOS static random-access memories. These memories are compatible with the CDP1802 microprocessor and will interface directly without additional components. The two memories are functionally identical. They differ in that the CDP1823SD has a recommended operating voltage range of 4 to 10 volts, and the CDP1823SCD has a recommended operating voltage range of 4 to 6 volts.

The CDP1823S memory has 8 common data input and data output terminals for direct connection to a bidirectional data bus and is operated from a single voltage supply. Five chip-select inputs are provided to simplify memory-system expansion. In order to enable the CDP1823S, the chip-select inputs $\overline{CS2}$, $\overline{CS3}$, and $\overline{CS4}$ require a low input signal, and the chip-select inputs CS1 and CS5 require a high input signal.

The $\overline{MRD}$ signal enables all 8 output drivers when in the low state and should be in a high state during a write cycle.

After valid data appear at the output, the address inputs may be changed immediately. Output data will be valid until either the $\overline{MRD}$ signal goes high, the device is deselected, or t_{AA} (access time) after address changes.

The CDP1823SD and CDP1823SCD are supplied in hermetic 24-lead dual-in-line ceramic packages.



Terminal Assignment

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE (V_{DD})
(All voltages referenced to V_{SS} terminal)
CDP1823SD . . . . . −0.5 to +11 V
CDP1823SCD . . . . . −0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A) . . . . . −20 to +85°C
LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

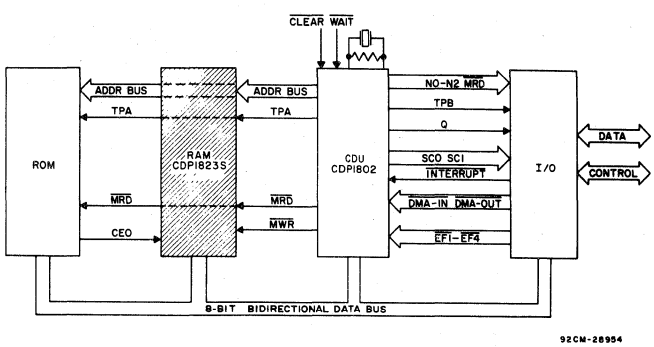
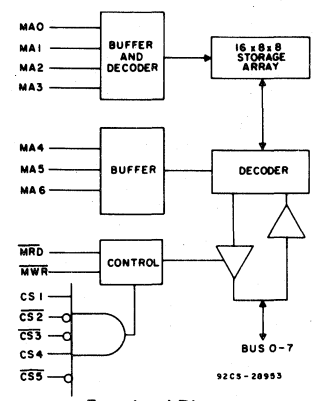


Fig. 1 — Typical CDP1802 microprocessor system.



Functional Diagram

OPERATING CONDITIONS at T_A = 25°C Unless Otherwise Specified

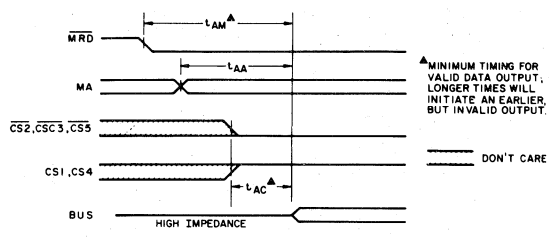
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1823SD		CDP1823SCD		
	Min.	Max.	Min.	Max.	
Supply-Voltage Range (At T_A = Full Package-Temperature Range)	4	10	4	6	V
Recommended Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Input Signal Rise and Fall Time, t_r,t_f	–	1	–	1	μs

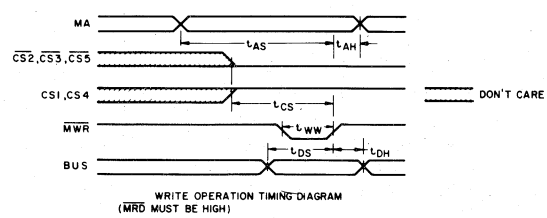
OPERATIONAL MODES

Function	$\overline{MRD}$	$\overline{MWR}$	CS1	$\overline{CS2}$	$\overline{CS3}$	CS4	$\overline{CS5}$	Bus Terminal State
READ	0	X	1	0	0	1	0	Storage State of Addressed Word
WRITE	1	0	1	0	0	1	0	Input High-Impedance
STAND-BY	1	1	1	0	0	1	0	High-Impedance
NOT SELECTED	X	X	0	X	X	X	X	High-Impedance
	X	X	X	1	X	X	X	
	X	X	X	X	1	X	X	
	X	X	X	X	X	0	X	
	X	X	X	X	X	X	1	

Logic 1 = High Logic 0 = Low X = Don't Care



READ OPERATION TIMING DIAGRAM



WRITE OPERATION TIMING DIAGRAM
($\overline{MRD}$ MUST BE HIGH)

Timing Diagrams

92CM-28955

Note:

The dynamic characteristics and timing diagrams indicate maximum performance capability of the CDP1823S. When used directly with the CDP1802 microprocessor, timing will be determined by the clock frequency and internal delays of the microprocessor.

The following general timing relationships will hold when the CDP1823S is used with the CDP1802 microprocessor:

$t_{WW} = 2\ t_c$

$t_{AH} = 1.0\ t_c$

$t_{AS} = 4.5\ t_c$

$t_{DH} = 1.0\ t_c$ } Data transfers from

$t_{DS} = 5.5\ t_c$ } CDP1802 to memory

$\overline{MRD}$ occurs one clock period (t_c) earlier than the address bits MA0-MA7.

where $t_c = \dfrac{1}{\text{CDP1802 clock frequency}}$

The CDP1823S is capable of operating at the maximum clock frequency of the CDP1802 microprocessor.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	TEST CONDITIONS	V_O (V)	V_{DD} (V)	TYPICAL VALUES CDP1823SD	TYPICAL VALUES CDP1823SCD	UNITS
Static						
Quiescent Device Current, I_L (Max.)		–	5	300	1000	μA
		–	10	1000	–	
Total Power Dissipation, P_D, at 1 μs cycle	C_L=50 pF READ Cycles	–	5	15	20	mW
		–	10	65	–	
Output Voltage: Low-Level, V_{OL}		–	5-10	0.01	0.01	V
High-Level, V_{OH}		–	5	4.99	4.99	V
		–	10	9.99	–	
Noise Margin: V_{NML}	Any Input	0.5	5	1	1	V
		1	10	1.5	–	
V_{NMH}	Any Input	4.5	5	1	1	V
		9	10	1.5	–	
Output Drive Current (Min.): N-Channel (Sink), I_{DN}	Any Output	0.4	5	1.2	1.2	mA
		0.5	10	1.8	–	
P-Channel (Source), I_{DP}	Any Output	4.6	5	–0.8	–0.8	mA
		9.5	10	–1.8	–	
Data Bus Leakage	$\overline{MRD}$ = H	–	5-10	±5	±5	μA
Input Leakage, I_{IL}, I_{IH}	Any Input	–	5-10	±1	±1	μA
Dynamic: t_r,t_f = 10 ns, C_L = 50 pF						
Read Operation						
Access Time From Address Change, t_{AA}		–	5	350	350	ns
		–	10	200	–	
Access Time From Chip Select, t_{AC}		–	5	250	250	ns
		–	10	150	–	
Output Active From $\overline{MRD}$, t_{AM}		–	5	250	250	ns
		–	10	150	–	
Write Operation						
Write Pulse Width, t_{WW}		–	5	150	150	ns
		–	10	100	–	
Data Setup Time, t_{DS}		–	5	150	150	ns
		–	10	100	–	
Data Hold Time, t_{DH}		–	5	100	100	ns
		–	10	50	–	
Chip Select Setup Time, t_{CS}		–	5	250	250	ns
		–	10	150	–	
Address Setup Time, t_{AS}		–	5	200	200	ns
		–	10	150	–	
Address Hold Time, t_{AH}		–	5	100	100	ns
		–	10	50	–	
Capacitance						
Input, C_I		–	–	5	5	pF
Output, C_O		–	–	5	5	pF
I/O		–	–	15	15	pF

Preliminary Data

32-Word x 8-Bit Static Random-Access Memory

The RCA-CDP1824D and CDP1824CD are 32-word x 8-bit fully static COS/MOS random-access memories for use in CDP1800 series microprocessor systems. These parts are compatible with the CDP1802 microprocessor and will interface directly without additional components.

The CDP1824 is fully decoded and does not require a precharge or clocking signal for proper operation. It has common input and output and is operated from a single voltage supply. The $\overline{MRD}$ signal (output disable control) enables the three-state output drivers, and overrides the $\overline{MWR}$ signal. A $\overline{CS}$ input is provided for memory expansion.

The CDP1824D is functionally identical to the CDP1824CD. The CDP1824D has a recommended operating voltage range of 3 to 12 volts, and the CDP1824CD has a recommended operating voltage range of 4 to 6 volts.

The CDP1824D and CDP1824CD are supplied in 18-lead, hermetic, dual-in-line ceramic packages.

Features:

- **Static Silicon-Gate CMOS circuitry—CD4000-series compatible**
- **Compatible with CDP1800-series microprocessors at maximum speed**
- **Interfaces with CDP1802 microprocessor without additional components**
- **Fast access time:**
  400 ns typ. at V_{DD} = 5 V;
  200 ns typ. at V_{DD} = 10 V
- **Single voltage supply**
- **No precharge or clock required**
- **Full military temperature range (−55°C to +125°C)**
- **Low quiescent and operating power**

MAXIMUM RATINGS, *Absolute-Maximum Values*

Storage-Temperature Range (T_{stg}) ..... −65 to +150°C

Operating-Temperature Range (T_A) ..... −55 to +125°C

DC Supply-Voltage Range (V_{DD})
(All voltage values referenced to V_{SS} terminal)
CDP1824D ..... −0.5 to +15 V
CDP1824CD ..... −0.5 to +7 V

Power Dissipation Per Package (P_D):
For T_A=−55 to +100°C ..... 500 mW
For T_A=+100 to +125°C ..... Derate Linearly to 200 mW

Device Dissipation Per Output Transistor:
For T_A=−55°C to +125°C ..... 100 mW

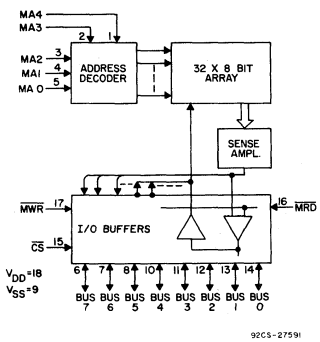
Input Voltage Range, All Inputs ..... −0.5 to V_{DD} +0.5 V

Lead Temperature (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A=25°C Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	Conditions V_{DD} (V)	LIMITS CDP1824D Min.	CDP1824D Max.	CDP1824CD Min.	CDP1824CD Max.	UNITS
Supply-Voltage Range (At T_A=Full Package-Temperature Range)	–	3	12	4	6	V
Recommended Input Voltage Range	–	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Input Signal Rise and Fall Time, t_r,t_f	–	–	5	–	5	μs



Functional Diagram

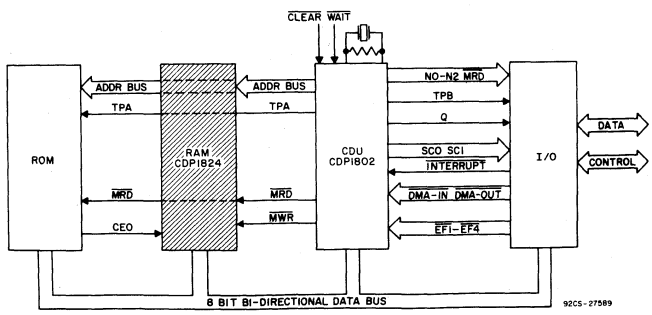


Fig. 1—Typical CDP1802 microprocessor system.

OPERATIONAL MODES

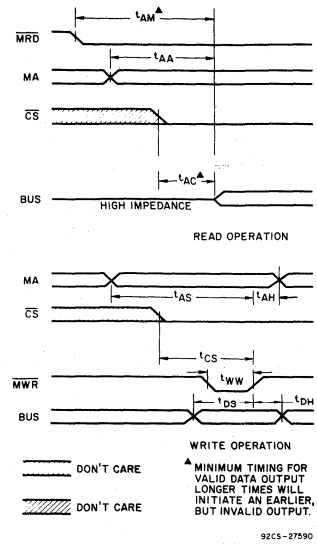
Function	$\overline{CS}$	$\overline{MRD}$	$\overline{MWR}$	Data Pins Status
READ	0	0	X	Output: High/Low Dependent on Data
WRITE	0	1	0	Input, Output Disabled
Not Selected	1	X	X	Output Disabled High-Impedance State
Standby	0	1	1	

Logic 1 = High Logic 0 = Low X = Don't Care

CDP1824D, CDP1824CD

ELECTRICAL CHARACTERISTICS at T_A=25°C

CHARACTERISTIC	TEST CONDITIONS	V_O (V)	V_{DD} (V)	LIMITS CDP1824D TYPICAL VALUES	LIMITS CDP1824CD TYPICAL VALUES	UNITS
Static						
Quiescent Device Current, I_L		–	5	100	500	μA
		–	10	500	–	
		–	15	1000	–	
Output Voltage: Low-Level, V_{OL}		–	5-10	0.01	0.01	V
High-Level, V_{OH}		–	5	4.99	4.99	
		–	10	9.99	–	
Noise Margin: V_{NML}	Any Input	0.5	5	1	1	V
		1	10	1.5	–	
V_{NMH}	Any Input	4.5	5	1	1	
		9	10	1.5	–	
Output Drive Current: N-Channel (Sink), I_{DN}	Any Output	0.4	5	1.6	1.6	mA
		0.5	10	3.6	–	
P-Channel (Source), I_{DP}	Any Output	4.6	5	−1.6	−1.6	
		9.5	10	−3.6	–	
Data Output Off-Resistance, R_O(Off)	$\overline{MRD}/\overline{CS}$=H	–	5-10	5	5	MΩ
Input Leakage, I_{IL}, I_{IH}	Any Input	–	5-10	±1	±1	μA
Dynamic: t_r,t_f=10 ns, C_L=50 pF						
Read Operation						
Access Time From Address Change, t_{AA}		–	5	400	400	ns
		–	10	200	–	
Access Time From Chip Select, t_{AC}		–	5	300	300	ns
		–	10	150	–	
Cutput Active From $\overline{MRD}$, t_{AM}		–	5	300	300	ns
		–	10	150	–	
Write Operation						
Write Pulse Width, t_{WW}		–	5	200	200	ns
		–	10	150	–	
Data Setup Time, t_{DS}		–	5	100	100	ns
		–	10	50	–	
Data Hold Time, t_{DH}		–	5	40	40	ns
		–	10	20	–	
Chip Select Setup Time, t_{CS}		–	5	550	550	ns
		–	10	300	–	
Address Setup Time, t_{AS}		–	5	500	500	ns
		–	10	300	–	
Address Hold Time, t_{AH}		–	5	100	100	ns
		–	10	50	–	



Timing Diagrams

Note:
The dynamic characteristics and timing diagrams indicate maximum performance capability of the CDP1824. When used directly with the CDP1802 microprocessor, timing will be determined by the clock frequency and internal delays of the microprocessor.

The following general timing relationships will hold when the CDP1824 is used with the CDP1802 microprocessor:

$t_{WW} = 2\ t_c$
$t_{AH} = 1.0\ t_c$
$t_{AS} = 4.5\ t_c$
$t_{DH} = 1.0\ t_c$ } Data transfers from
$t_{DS} = 5.5\ t_c$ } CDP1802 to memory

$\overline{MRD}$ occurs one clock period (t_c) earlier than the address bits MA0-MA7.

where $t_c = \frac{1}{\text{CDP1802 clock frequency}}$

The CDP1824 is capable of operating at the maximum clock frequency of the CDP1802 microprocessor.

Preliminary Data

512-Word x 8-Bit Static Read-Only Memory

The RCA-CDP1831D and CDP1831CD are static 4096-bit mask-programmable COS/MOS read-only memories organized as 512 words x 8 bits and designed for use in CDP1800-series microprocessor systems. They will directly interface with either the CDP1801 or CDP1802 microprocessors without additional components.

The CDP1831 responds to 16-bit address multiplexed on 8 address lines. Address latches are provided on-chip to store the 8 most significant bits of the 16-bit address. By mask option, this ROM can be programmed to operate in any 512-word byte of 64K memory space. Three Chip-Select signals—CS1, CS2, $\overline{MRD}$—are also provided.

The polarity of the clock (TPA), and CS1 and CS2 are user mask-programmable. The Chip-Enable output signal (CEO) goes "high" when the device is selected. This signal is intended for use as an output disable control for small memory systems.

The CDP1831D is functionally identical to the CDP1831CD. The CDP1831D has a recommended operating voltage range of 3 to 12 volts, and the CDP1831CD has a recommended operating voltage range of 4 to 6 volts.

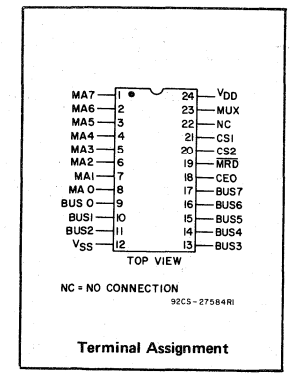
The CDP1831D and CDP1831CD are supplied in 24-lead, hermetic, dual-in-line ceramic packages.

MAXIMUM RATINGS,
Absolute-Maximum Values

Storage-Temperature Range (T_{stg}) ..... −65 to +150°C
Operating-Temperature Range (T_A) ..... −55 to +125°C
DC Supply-Voltage Range (V_{DD})
(All voltage values referenced to V_{SS} terminal)
CDP1831D ..... −0.5 to +15 V
CDP1831CD ..... −0.5 to +7 V
Power Dissipation Per Package (P_D):
For T_A=−55 to +100°C ..... 500 mW
For T_A=+100 to +125°C ..... Derate Linearly to 200 mW
Device Dissipation Per Output Transistor:
For T_A=−55°C to +125°C ..... 100 mW
Input Voltage Range, All Inputs ..... −0.5 to V_{DD} +0.5 V
Lead Temperature (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A=25°C Unless Otherwise Specified
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

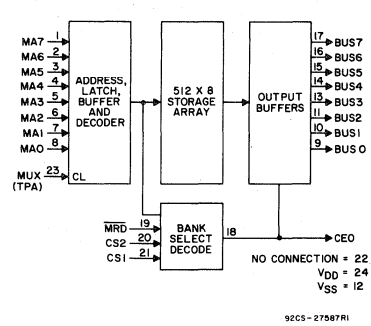
CHARACTERISTIC	CONDITIONS V_{DD} (V)	LIMITS CDP1831D Min.	CDP1831D Max.	CDP1831CD Min.	CDP1831CD Max.	UNITS
Supply-Voltage Range (At T_A=Full Package-Temperature Range)	–	3	12	4	6	V
Recommended Input Voltage Range	–	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
MUX Pulse Width (TPA), t_{PAW}		Typical		Typical		
	5	200		100		ns
	10	100		–		
Address Setup Time, t_{AS}	5	100		100		ns
	10	50		–		
Address Hold Time, t_{AH}	5	150		150		ns
	10	75		–		



Terminal Assignment

Features:

- **Static Silicon-Gate CMOS circuitry—CD4000-series compatible**
- **Compatible with CDP1800-series microprocessors at maximum speed**
- **Interfaces with CDP1801, CDP1802 microprocessors without additional components**
- **Fast access time: 400 ns typ. at V_{DD} = 10 V**
- **Single voltage supply**
- **On-chip address latch**
- **Full military temperature range (−55°C to +125°C)**
- **Optional programmable location within 64K memory space**
- **Low quiescent and operating power**



CDP1831 Functional Diagram

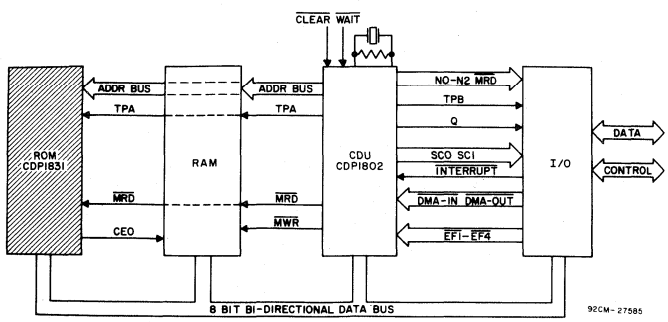
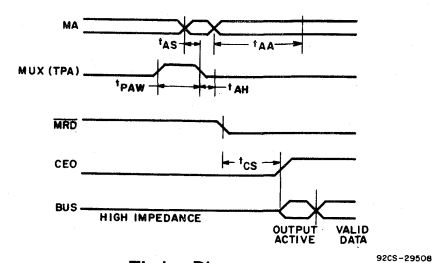


Fig. 1—Typical CDP1802 microprocessor system.



Timing Diagram

ELECTRICAL CHARACTERISTICS at T_A=25°C

CHARACTERISTIC	TEST CONDITIONS		LIMITS		UNITS
			CDP1831D	CDP1831CD	
	V_O (V)	V_{DD} (V)	TYPICAL VALUES	TYPICAL VALUES	
Static					
Quiescent Device Current, I_L	–	5	100	100	μA
	–	10	500	–	
	–	15	1000	–	
Output Drive Current:					mA
N-Channel (Sink), I_DN	0.4	5	0.8	0.8	
	0.5	10	1.8	–	
P-Channel (Source), I_DP	4.6	5	–0.8	–0.8	
	9.5	10	–1.8	–	
Dynamic: t_f,t_f=10 ns, C_L=50 pF					
Access Time From Address Change, t_{AA}	–	5	850	850	ns
	–	10	400	–	
Chip Enable Output Delay Time From CS, t_{CS}	–	5	400	400	ns
	–	10	200	–	

Note:
The dynamic characteristics and timing diagrams indicate maximum performance capability of the CDP1831. When used directly with the CDP1802 microprocessor, timing will be determined by the clock frequency and internal delays of the microprocessor.

The following general timing relationships will hold when the CDP1831 is used with the CDP1802 microprocessor:

$t_{AH} = 0.5\ t_c$

$t_{PAW} = 1.0\ t_c$

$\overline{MRD}$ occurs one clock period (t_c) earlier than the address bits MA0-MA7.

where $t_c = \frac{1}{\text{CDP1802 clock frequency}}$

The CDP1831 is capable of operating at the maximum clock frequency of the CDP1802 microprocessor.

Preliminary Data

512-Word x 8-Bit Static Read-Only Memory

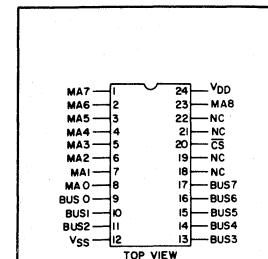
The RCA-CDP1832D and CDP1832CD are static 4096-bit mask-programmable COS/MOS read-only memories organized as 512 words x 8 bits and designed for use in CDP1800-series microprocessor systems. The CDP1832 ROM's are completely static—no clocks are required.

A Chip-Select input ($\overline{CS}$) is provided for memory expansion. Outputs are enabled when $\overline{CS}$=0.

The CDP1832 is a pin-for-pin compatible replacement for the industry types 2704/8704 Reprogrammable Read-Only Memories.

The CDP1832D is functionally identical to the CDP1832CD. The CDP1832D has a recommended operating voltage range of 3 to 12 volts, and the CDP1832CD has a recommended operating voltage range of 4 to 6 volts.

The CDP1832D and CDP1832CD are supplied in 24-lead, hermetic, dual-in-line ceramic packages.



Terminal Assignment

MAXIMUM RATINGS, *Absolute-Maximum Values*

Storage-Temperature Range (T_{stg}) ..... −65 to +150°C

Operating-Temperature Range (T_A) ..... −55 to +125°C

DC Supply-Voltage Range (V_{DD})
(All voltage values referenced to V_{SS} terminal)
CDP1832D ..... −0.5 to +15 V
CDP1832CD ..... −0.5 to +7 V

Power Dissipation Per Package (P_D):
For T_A=−55 to +100°C ..... 500 mW
For T_A=+100 to +125°C ..... Derate Linearly to 200 mW

Device Dissipation Per Output Transistor:
For T_A=−55°C to +125°C ..... 100 mW

Input Voltage Range, All Inputs ..... −0.5 to V_{DD} +0.5 V

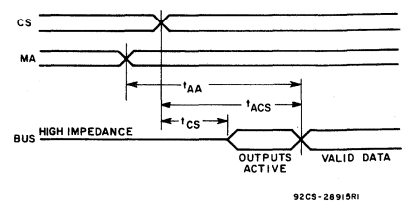
Lead Temperature (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

Features:

- **Static Silicon-Gate CMOS circuitry—CD4000-series compatible**
- **Compatible with CDP1800-series microprocessors at maximum speed**
- **Fast access time: 400 ns typ. at V_{DD} = 10 V**
- **Single voltage supply**
- **Full military temperature range (−55°C to +125°C)**
- **Functional replacement for industry type 8704 512 x 8 PROM**
- **Three-state outputs**
- **Low quiescent and operating power**

OPERATING CONDITIONS at T_A=25°C Unless Otherwise Specified
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITIONS V_{DD} (V)	LIMITS CDP1832D Min.	CDP1832D Max.	CDP1832CD Min.	CDP1832CD Max.	UNITS
Static						
Supply-Voltage Range (At T_A=Full Package-Temperature Range)	–	3	12	4	6	V
Recommended Input Voltage Range	–	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V



CDP1832
Timing Diagram

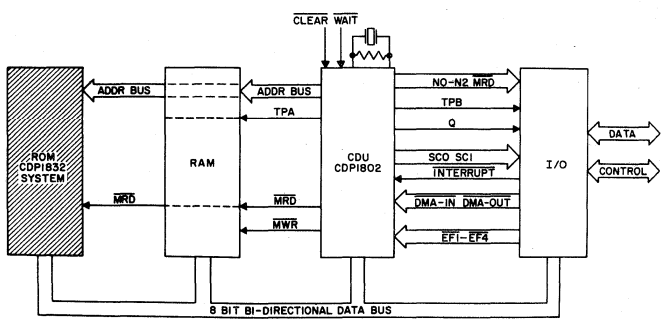
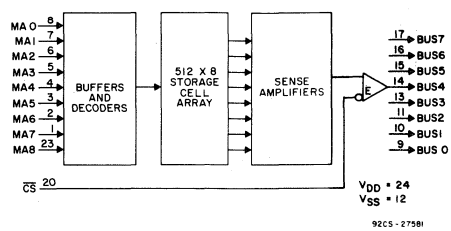


Fig. 1—Typical CDP1802 microprocessor system.



CDP1832
Functional Diagram

ELECTRICAL CHARACTERISTICS at T_A=25°C

CHARACTERISTIC	TEST CONDITIONS		LIMITS		UNITS
			CDP1832D	CDP1832CD	
	V_O (V)	V_{DD} (V)	TYPICAL VALUES	TYPICAL VALUES	
Static					
Quiescent Device Current, I_L	–	5	100	500	μA
	–	10	500	–	
	–	15	1000	–	
Output Drive Current: N-Channel (Sink), I_DN	0.4	5	0.8	0.8	mA
	0.5	10	1.8	–	
P-Channel (Source), I_DP	4.6	5	–0.8	–0.8	
	9.5	10	–1.8	–	
Dynamic: t_r,t_f=10 ns, C_L=50 pF					
Access Time From Address Change, t_{AA}	–	5	850	850	ns
	–	10	400	–	
Access Time From Chip Select, t_{ACS}	–	5	400	400	ns
	–	10	200	–	
Chip Select Delay, t_{CS}	–	5	400	400	ns
	–	10	200	–	

Preliminary Data

1024-Word x 8-Bit Static Read-Only Memory

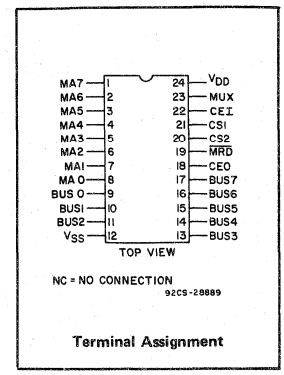
The RCA-CDP1833D and CDP1833CD are static 8192-bit mask-programmable COS/MOS read-only memories organized as 1024-words x 8 bits and designed for use in CDP1800-series microprocessor systems. They will directly interface with either the CDP1801 or CDP1802 microprocessors without additional components.

The CDP1833 responds to 16-bit address multiplexed on 8 address lines. Address latches are provided on-chip to store the 8 most significant bits of the 16-bit address. By mask option, this ROM can be programmed to operate in any 1024-word byte of 64K memory space. Two Chip-Select signals are also provided.

The polarity of MUX(TPA), CEI, MRD, CS1 and CS2 are user mask-programmable. The Chip-Enable output signal (CEO) is "high" when either CEI is high or the chip is selected. CEO and CEI can be connected in a daisy chain to control selection of RAM chips in a microprocessor system without additional components.

The CDP1833D is functionally identical to the CDP1833CD. The CDP1833D has a recommended operating voltage range of 3 to 12 volts, and the CDP1833CD has a recommended operating voltage range of 4 to 6 volts.

The CDP1833D and CDP1833CD are supplied in 24-lead hermetic dual-in-line ceramic packages.



Terminal Assignment

Features:

- Compatible with CDP1800-series microprocessors at maximum speed
- Static silicon-gate CMOS circuitry—CD4000-series compatible
- Interfaces with CDP1801, CDP1802 microprocessors without additional components
- Fast access time: 350 ns typ. at V_{DD} = 10 V
- Single voltage supply
- On-chip address latch
- Full military temperature range (−55°C to +125°C)
- Optional programmable location within 64K memory space
- Low quiescent and operating power

MAXIMUM RATINGS,
Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE (V_{DD})
(All voltage values referenced to V_{SS} terminal)
CDP1833D . . . . . −0.5 to +15 V
CDP1833CD . . . . . −0.5 to +7 V
INPUT VOLTAGE RANGE,
ALL INPUTS . . . . −0.5 to V_{DD} +0.5 V
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −55 to +100°C . . . . 500 mW
For T_A = +100 to +125°C . . . Derate Linearly to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = −55°C to +125°C . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A) . . . . . −55 to +125°C
STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

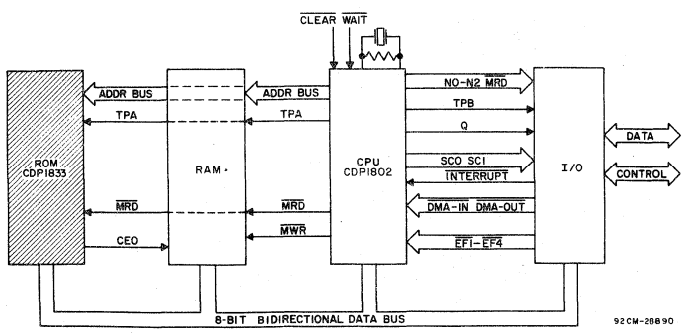


Fig. 1 – Typical CDP1802 microprocessor system.

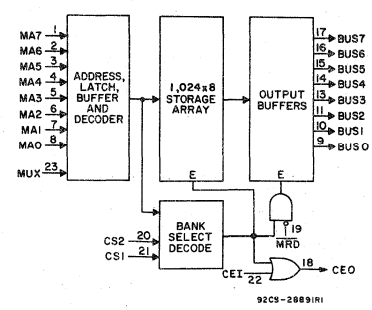


Fig. 2 – CDP1833 functional diagram.

OPERATING CONDITIONS at T_A=25°C Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITIONS V_{DD} (V)	LIMITS CDP1833D Min.	CDP1833D Max.	CDP1833CD Min.	CDP1833CD Max.	UNITS
Supply-Voltage Range (At T_A=Full Package-Temperature Range)	–	3	12	4	6	V
Recommended Input Voltage Range	–	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
MUX Pulse Width (TPA), t_{PAW}	5	Typical 200		Typical 200		ns
	10	100		–		
Address Setup Time, t_{AS}	5	50		50		ns
	10	25		–		
Address Hold Time, t_{AH}	5	150		150		ns
	10	75		–		

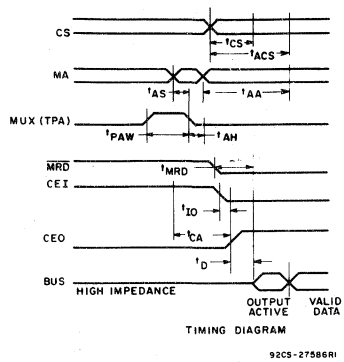


Fig. 3 – Timing diagram.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	TEST CONDITIONS V_O (V)	TEST CONDITIONS V_{DD} (V)	LIMITS CDP1833D TYPICAL VALUES	LIMITS CDP1833CD TYPICAL VALUES	UNITS
Static					
Quiescent Device Current, I_L Max.	–	5	100	1000	μA
	–	10	500	–	
	–	15	1000	–	
Output Drive Current: N-Channel (Sink), I_{DN} Min.	0.4	5	3.2	3.2	mA
	0.5	10	7.2	–	
P-Channel (Source), I_{DP} Min.	4.6	5	–2	–2	
	9.5	10	–5	–	
Dynamic: t_r, t_f = 10 ns, C_L = 50 pF					
Dynamic Power Dissipation* Chip Active CL = 3.2 MHz	–	5	30	30	mW
	–	10	120	–	
Chip Inactive CL = 3.2 MHz	–	5	5	5	
	–	10	20	–	
Access Time From Address Change, t_{AA}	–	5	850	850	ns
	–	10	350	–	
CEO From Address Change, t_{CA}	–	5	500	500	ns
	–	10	250	–	
Bus Contention Delay, t_D	–	5	300	300	ns
	–	10	150	–	
Daisy Chain Delay, t_{IO}	–	5	200	200	ns
	–	10	100	–	
Read Delay $t_{\overline{MRD}}$	–	5	500	500	ns
	–	10	250	–	
Chip Select Delay t_{CS}	–	5	600	600	ns
	–	10	300	–	
Access Time From Chip Select, t_{ACS}	–	5	700	700	ns
	–	10	300	–	

*Measured with random bit pattern at a system clock rate of 3.2 MHz, which results in a memory-cycle time of 2.5 μs. Power dissipation at other voltages and frequencies follows the relation $P = KfV^2$. Chip is inactive when deselected by either the Bank Select code or the Chip Select inputs.

Note:

The dynamic characteristics and timing diagrams indicate maximum performance capability of the CDP1833. When used directly with the CDP1802 microprocessor, timing will be determined by the clock frequency and internal delays of the microprocessor.

The following general timing relationships will hold when the CDP1833 is used with the CDP1802 microprocessor:

$t_{AH} = 0.5\ t_c$

$t_{PAW} = 1.0\ t_c$

$\overline{MRD}$ occurs one clock period (t_c) earlier than the address bits MA0-MA7.

where $t_c = \frac{1}{\text{CDP1802 clock frequency}}$

The CDP1833 is capable of operating at the maximum clock frequency of the CDP1802 microprocessor.

Preliminary Data

1024-Word x 8-Bit Static Read-Only Memory

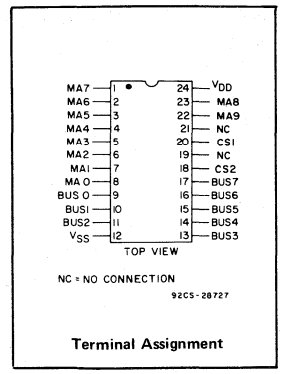
The RCA-CDP1834D and CDP1834CD are static 8192-bit mask-programmable COS/MOS read-only memories organized as 1024 words x 8 bits and designed for use in CDP1800-series microprocessor systems. The CDP1834 ROM's are completely static—no clocks are required.

Two CHIP-SELECT inputs (CS1, CS2) are provided for memory expansion. The polarity of each CHIP-SELECT input is user mask-programmable.

The CDP1834 is pin-compatible with industry type 2308 ROMs and 2708 PROMs.

The two memories are functionally identical. They differ in that the CDP1834D has a recommended operating voltage range of 3 to 12 volts, and the CDP1834CD has a recommended operating voltage range of 4 to 6 volts.

The CDP1834D and CDP1834CD are supplied in 24-lead, hermetic, dual-in-line ceramic packages.



Terminal Assignment

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE (V_{DD})
(All voltage values referenced to V_{SS} terminal):
- CDP1834D . . . . . −0.5 to +15 V
- CDP1834CD . . . . . −0.5 to +7 V

POWER DISSIPATION PER PACKAGE (P_D):
- FOR T_A = −55 to +100°C . . . . . 500 mW
- FOR T_A = +100 to +125°C . . . . . Derate Linearly to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
- FOR T_A = −55°C to +125°C . . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A) . . . . . −55 to +125°C
LEAD TEMPERATURE (DURING SOLDERING):
- At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

Features:

- Static Silicon-Gate CMOS circuitry-CD4000-series compatible
- Compatible with CDP1800-series microprocessors at maximum speed
- Fast access time: 350 ns typ. at V_{DD} = 10 V
- Single voltage supply
- Full military temperature range (−55°C to +125°C)
- Functional replacement for industry type 2708 1024 x 8 PROM
- Three-state outputs
- Low quiescent and operating power

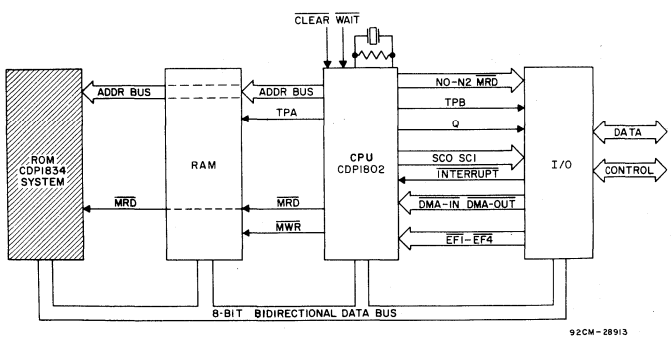
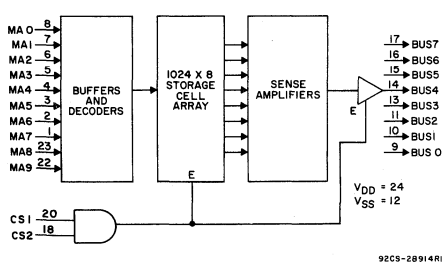
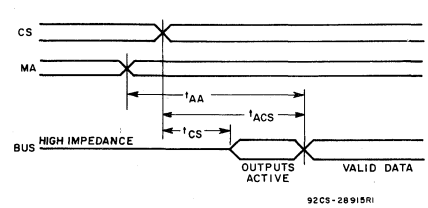


Fig. 1 – Typical CDP1802 microprocessor system.



CDP1834
Functional Diagram



CDP1834
Timing Diagram

OPERATING CONDITIONS at T_A = 25°C Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITIONS	LIMITS				UNITS
	V_{DD} (V)	CDP1834D		CDP1834CD		
		Min.	Max.	Min.	Max.	
Static						
Supply-Voltage Range (At T_A = Full Package-Temperature Range)	–	3	12	4	6	V
Recommended Input Voltage Range	–	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	TEST CONDITIONS		TYPICAL VALUES		UNITS
	V_O (V)	V_{DD} (V)	CDP1834D	CDP1834CD	
Static					
Quiescent Device Current, I_L (Max.)	–	5	100	1000	μA
	–	10	500	–	
	–	15	1000	–	
Output Drive Current: (Min.)	0.4	5	3.2	3.2	mA
N-Channel (Sink), I_DN	0.5	10	7.2	–	
P-Channel (Source), I_DP	4.6	5	–2	–3.2	
	9.5	10	–5	–	
Dynamic: t_r, t_f = 10 ns, C_L = 50 pF					
Dynamic Power Dissipation* (f_{CL} = 3.2 MHz)	–	5	15	15	mW
Chip Selected	–	10	60	–	
Chip Not Selected	–	5	2.5	2.5	mW
	–	10	10	–	
Access Time From Address	–	5	850	850	ns
Change, t_{AA}	–	10	350	–	
Access Time From Chip	–	5	700	700	ns
Select, t_{ACS}	–	10	300	–	
Chip Select Delay, t_{CS}	–	5	600	600	ns
	–	10	300	–	

* Measured with random bit pattern at a microprocessor system clock rate of 3.2 MHz which results in a memory cycle time of 2.5 μs. Power dissipation at other voltages and frequencies follows the relation $P = KfV^2$

Preliminary Data

8-Bit Input/Output Port

The RCA-CDP1852D and CDP1852CD are parallel, 8-bit, mode-programmable COS/MOS input/output ports designed for use in CDP-1800 series microprocessor systems. These input/output ports are compatible and will interface directly with the CDP1802 without additional components.

The mode control is used to program the device as an input port (mode=0) or output port (mode=1). If the CDP1852 is used as an input port (mode=0), data is strobed into the port's 8-bit register by a high (1) level on the clock line. The negative, high-to-low transition of the clock sets the Service Request Flip-Flop ($\overline{SR}$=0) and latches the data in the register. The $\overline{SR}$ output can be used to signal the microprocessor. When CS1•CS2=1 the three-state output drivers are enabled, the negative high-to-low transition of CS1•$\overline{CS2}$ resets the Service Request Flip-Flop, $\overline{SR}$=1.

If the CDP1852 is used as an output port (mode=1), data is strobed into the port's 8-bit register when $\overline{CS1}$•CS2•CLOCK=1. The three-state output drivers are enabled at all times when the CDP1852 is configured as an output port. The service request signal is generated at the termination of $\overline{CS1}$•CS2=1 and will be present, 1 level, until the following negative, high-to-low transition of the clock.

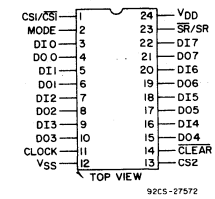
A $\overline{CLEAR}$ control is provided for resetting the port's register and service request flip-flop.

The CDP1852D is functionally identical to the CDP1852CD. The CDP1852D has a recommended operating voltage range of 3 to 12 volts, and the CDP1852CD has a recommended operating voltage range of 4 to 6 volts.

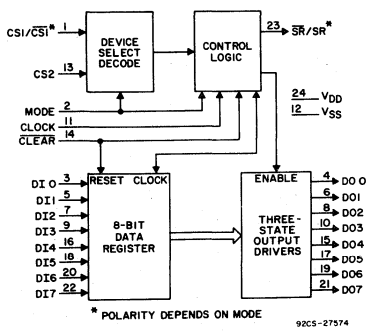
The CDP1852D and CDP1852CD are supplied in 24-lead, hermetic, dual-in-line ceramic packages.

Features:

- **Static Silicon-Gate CMOS circuitry—CD4000-series compatible**
- **Compatible with CDP1800-series microprocessors at maximum speed**
- **Interfaces with CDP1802 microprocessor without additional components**
- **Single voltage supply**
- **Full military temperature range (–55°C to +125°C)**
- **Parallel 8-bit data register and buffer**
- **Flip-flop for service request**
- **Asynchronous register clear**
- **Low quiescent and operating power**



Terminal Assignment



Functional Diagram

MAXIMUM RATINGS,
Absolute-Maximum Values

Storage-Temperature Range (T_{stg}) ..... –65 to +150°C

Operating-Temperature Range (T_A) ..... –55 to +125°C

DC Supply-Voltage Range (V_{DD})
(All voltage values referenced to V_{SS} terminal)
CDP1852D ..... –0.5 to +15 V
CDP1852CD ..... –0.5 to +7 V

Power Dissipation Per Package (P_D):
For T_A=–55 to +100°C ..... 500 mW
For T_A=+100 to +125°C ..... Derate Linearly to 200 mW

Device Dissipation Per Output Transistor:
For T_A=–55°C to +125°C ..... 100 mW

Input Voltage Range, All Inputs ..... –0.5 to V_{DD} +0.5 V

Lead Temperature (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A=25°C Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITIONS V_{DD} (V)	LIMITS CDP1852D Min.	CDP1852D Max.	CDP1852CD Min.	CDP1852CD Max.	UNITS
Supply-Voltage Range (At T_A=Full Package-Temperature Range)	–	3	12	4	6	V
Recommended Input Voltage Range	–	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Strobe Pulse Width, t_{WS}	5	Typical 200		Typical 200		ns
	10	100		–		
Data Setup Time, t_{DS}	5	0		0		ns
	10	0		–		
Data Hold Time, t_{DH}	5	100		100		ns
	10	50		–		

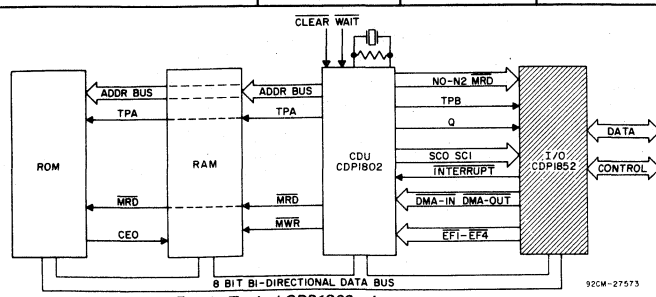
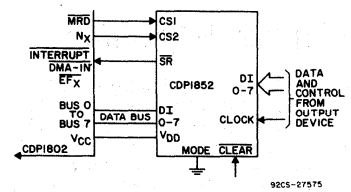


Fig. 1—Typical CDP1802 microprocessor system.

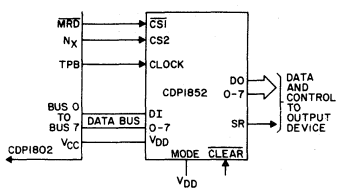
ELECTRICAL CHARACTERISTICS at T_A=25°C

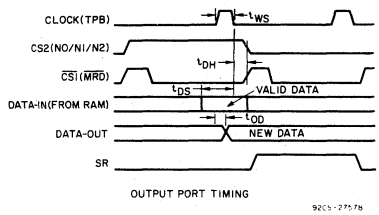
CHARACTERISTIC	TEST CONDITIONS V_O (V)	TEST CONDITIONS V_{DD} (V)	LIMITS CDP1852D TYPICAL VALUES	LIMITS CDP1852CD TYPICAL VALUES	UNITS
Static					
Quiescent Device Current, I_L	–	5	50	100	μA
	–	10	100	–	
	–	15	500	–	
Output Drive Current:					mA
N-Channel (Sink), I_{DN}	0.4	5	1.6	1.6	
	0.5	10	3.6	–	
P-Channel (Source), I_{DP}	4.6	5	−1.6	−1.6	
	9.5	10	−3.6	–	
Dynamic: t_r, t_f=10 ns, C_L=50 pF					
Propagation Delay Times:					ns
Output from CS, t_{CA}		5	200	200	
	–	10	100	–	
Data to Output, t_{OD}	–	5	200	200	
	–	10	100	–	

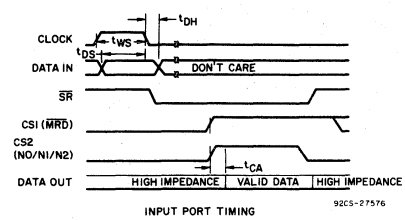


MODE = 0

CLOCK	CS1·CS2	$\overline{CLEAR}$	Data Out Equals
X	0	X	High-Impedance
0	1	0	0
0	1	1	Data Latch
1	1	X	Data In







MODE = 1

CLOCK	$\overline{CS1}$·CS2	$\overline{CLEAR}$	Data Out Equals
0	X	0	0
0	X	1	Data Latch
X	0	1	Data Latch
1	1	X	Data In

SR = 1▲	SR = 0
$\overline{CS1}$·CS2 ↘	CLOCK ↘ Or $\overline{CLEAR}$ ↘

Fig. 2—CDP1852 output port operation.

$\overline{SR}$ = 0	$\overline{SR}$ = 1▲
CLOCK ↘	CS1·CS2 ↘ Or $\overline{CLEAR}$ ↘

Fig. 3— CDP1852 input port operation.

Note:
The dynamic characteristics and timing diagrams indicate maximum performance capability of the CDP1852. When used directly with the CDP1802 microprocessor, timing will be determined by the clock frequency and internal delays of the microprocessor.

The following general timing relationships will hold when the CDP1852 is used as an output port with the CDP1802 microprocessor:

$$t_{WS}(TPB) = 1.0\ t_c$$

$$t_{DH} = 0.5\ t_c$$

$$t_c = \frac{1}{\text{CDP1802 clock frequency}}$$

of the port. The termination of the signal may improperly place the service request flip-flop in the "1" state. The transition used to set and reset $\overline{SR}$/SR may be positive or negative. The polarity will not affect circuit operation shown in Figs.2 and 3.

▲ The service request flip-flop is placed in the "1" state by the termination of the I/O port selection, CS1·CS2 or $\overline{CS1}$·CS2. System implementations should be avoided which cause a transient selection

Preliminary Data

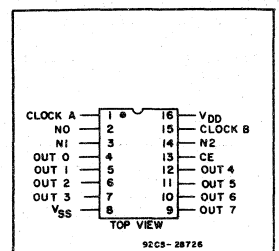
N-Bit 1of 8 Decoder

The RCA-CDP1853D and CDP1853CD are 1 of 8 decoders designed for use in CDP1800-series, microprocessor systems. These devices, which are functionally identical, are specifically designed for use as gated N-bit decoders and interface directly with the CDP1802 microprocessor without additional components. The CDP1853D has a recommended operating voltage range of 3 to 12 volts, and the CDP1853CD has a recommended operating voltage range of 4 to 6 volts.

When CHIP ENABLE (CE) is high, the selected output will be true (high) from the trailing edge of CLOCK A (high-to-low transition) to the trailing edge of CLOCK B (high-to-low transition). All outputs will be low when the device is not selected (CE = 0) and during conditions of CLOCK A and CLOCK B as shown in Fig. 2. The CDP1853 inputs N0, N1, N2, CLOCK A, and CLOCK B are connected to CDP1802 microprocessor outputs N0, N1, N2, TPA, and TPB respectively, when used to decode I/O commands as shown in Fig. 5. The CHIP ENABLE (CE) input provides the capability for multiple levels of decoding as shown in Fig. 6.

The CDP1853 can also be used as a general 1 of 8 decoder for I/O and memory system applications as shown in Fig. 4.

The CDP1853D and CDP1853CD are supplied in hermetic 16-lead dual-in-line ceramic packages.



TERMINAL ASSIGNMENT

Features:

- Static Silicon-Gate CMOS circuitry — CD4000-series compatible
- Compatible with CDP1800-series microprocessors at maximum speed
- Low quiescent and operating power
- Provides direct control of up to 7 input and 7 output devices
- CHIP ENABLE (CE) allows easy expansion for multi-level I/O systems
- Single voltage supply
- Full military temperature range (−55 to +125°C)

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE (V_{DD})
(All voltage values referenced to V_{SS} terminal):
- CDP1853D . . . . . −0.5 to +15 V
- CDP1853CD . . . . . −0.5 to +7 V

POWER DISSIPATION PER PACKAGE (P_D):
- FOR T_A = −55 to +100°C . . . . . 500 mW
- FOR T_A = +100 to +125°C . . . . . Derate linearly to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
- FOR T_A = −55°C to +125°C . . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A) . . . . . −55 to +125°C
LEAD TEMPERATURE (DURING SOLDERING):
- At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

OPERATING CONDITIONS at T_A = 25°C Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1853D		CDP1853CD		
	Min.	Max.	Min.	Max.	
Supply Voltage Range (At T_A = Full Package-Temperature Range)	3	12	4	6	V
Recommended Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

TRUTH TABLE

CE	CL A	CL B	EN
1	0	0	Qn-1*
1	0	1	1
1	1	0	0
1	1	1	1
0	X	X	0

N2	N1	N0	EN	0	1	2	3	4	5	6	7
0	0	0	1	0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	0	0	0	0	0
0	1	0	1	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	1	0	0	0	0
1	0	0	1	0	0	0	0	1	0	0	0
1	0	1	1	0	0	0	0	0	1	0	0
1	1	0	1	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1
X	X	X	0	0	0	0	0	0	0	0	0

1 = High level 0 = Low level X = Don't care

*Qn-1 = Enable remains in previous state.

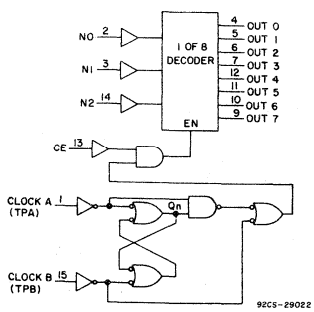


Fig. 1 — CDP1853 functional diagram.

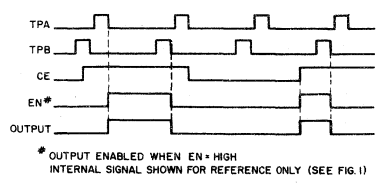


Fig. 2 — Timing diagram.

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	TEST CONDITIONS			TYPICAL VALUES		UNITS
		V_O (V)	V_{DD} (V)	CDP1853D	CDP1853CD	
Static						
Quiescent Device Current, I_L		–	5	50	100	μA
		–	10	100	–	
		–	15	500	–	
Output Voltage:						
Low-Level, V_{OL}		–	5-10	0.01	0.01	V
High-Level, V_{OH}		–	5	4.99	4.99	
		–	10	9.99	–	
Noise Margin:						
Inputs Low, V_{NML}	Any Input	0.5	5	1	1	V
		1	10	1.5	–	
Inputs High, V_{NMH}	Any Input	4.5	5	1	1	
		9	10	1.5	–	
Output Drive Current:						
N-Channel (Sink), I_{DN}	Any Output	0.4	5	1.6	1.6	mA
		0.5	10	3.6	–	
P-Channel (Source), I_{DP}	Any Output	4.6	5	–1.6	–1.6	
		9.5	10	–3.6	–	
Input Leakage, I_{IL}, I_{IH}	Any Input	–	5-10	±1	±1	μA

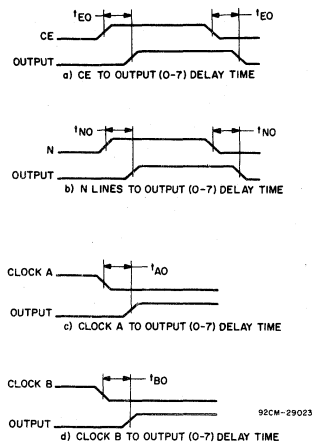


Fig. 3 – Propagation delay time diagrams.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	V_{DD} (V)	TYPICAL VALUES		UNITS
		CDP1853D	CDP1853CD	
t_r, t_f = 10 ns, C_L = 100 pF				
Propagation Delay Time:	5	200	200	ns
CE to Output, t_{EOH}, t_{EOL}	10	100	–	
	5	250	250	ns
N to Outputs, t_{NOH}, t_{NOL}	10	120	–	
	5	225	225	ns
Clock A to Output, t_{AO}	10	110	–	
Clock B to Output, t_{BO}	5	200	200	ns
	10	100	–	

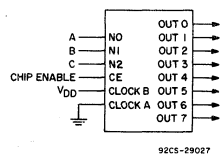


Fig. 4 – N-bit decoder used as a 1 of 8 decoder.

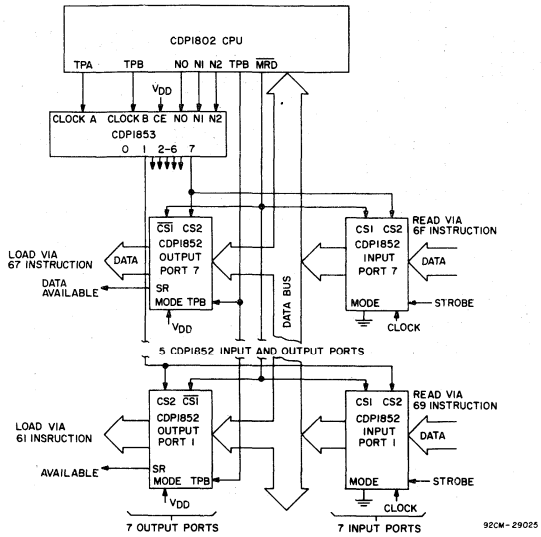


Fig. 5 – N-bit decoder in a one-level I/O system.

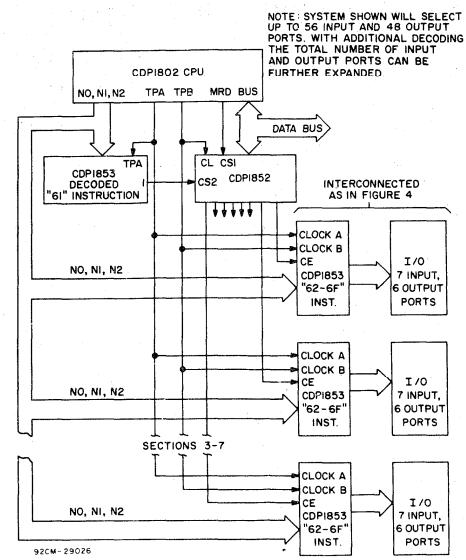


Fig. 6 – Two-level I/O using CDP1853 and CDP1852.

CDP1854D, CDP1854CD

Preliminary Data

CMOS Universal Asynchronous Receiver/Transmitter (UART)

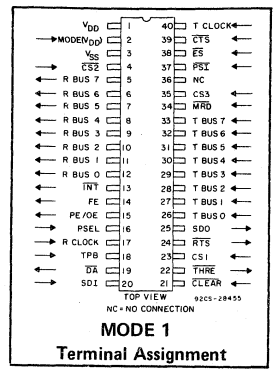
The CDP1854D and CDP1854CD are silicon-gate COS/MOS Universal Asynchronous Receiver/Transmitter (UART) circuits. They are designed to provide the necessary formatting and control for interfacing between serial and parallel data. For example, it can be used to interface between a peripheral or terminal with serial I/O ports and the 8-bit CDP1802 parallel data bus system. The CDP1854 is capable of full duplex operation, i.e., simultaneous conversion of serial input data to parallel output data and parallel input data to serial output data.

The CDP1854 UART can be programmed to operate in one of two modes by using the mode control input. When the mode input is high (MODE=1), the CDP1854 is directly compatible with the CDP1802 microprocessor system without additional interface circuitry.

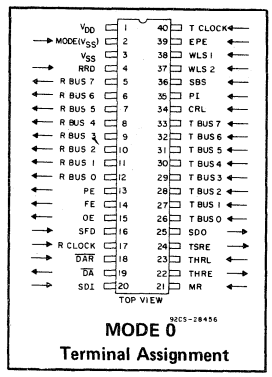
When the mode input is low (MODE=0), the device is functionally compatible with industry standard UART's such as the TR1602A. It is also pin compatible with these types, except that pin 2 is used for the mode control input instead of a V_{GG}=−12 V supply connection.

The CDP1854D and the CDP1854CD are functionally identical. The CDP1854D has a recommended operating-voltage range of 3-12 volts, and the CDP1854CD has a recommended operating-voltage range of 4-6 volts.

The CDP1854D and CDP1854CD are supplied in hermetic 40-lead dual-in-line ceramic packages.



MODE 1
Terminal Assignment



MODE 0
Terminal Assignment

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg})	−65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A)	−55 to +125°C
DC SUPPLY-VOLTAGE RANGE (V_{DD})	
(All voltage values referenced to V_{SS} terminal)	
CDP1854D	−0.5 to +15 V
CDP1854CD	−0.5 to +7 V
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −55 to +100°C	500 mW
For T_A = +100 to +125°C	Derate Linearly to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:	
For T_A = −55°C to +125°C	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm)	
from case for 10 s max.	+265°C

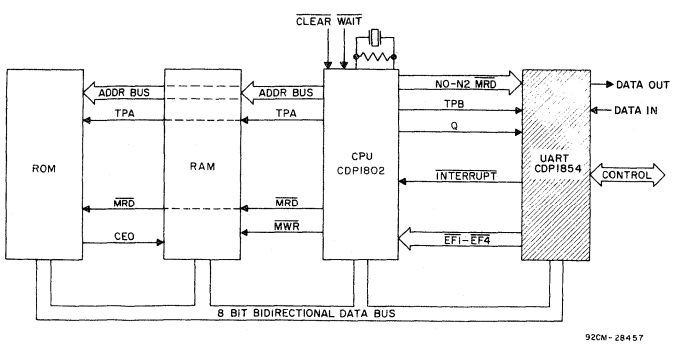


Fig. 1 – Typical CDP1802 microprocessor system.

Features:

- **Static silicon-gate CMOS circuitry— CD4000 Series compatible**
- **Two operating modes:**
  - **Mode 0—functionally compatible with industry standard types such as the TR1602A**
  - **Mode 1—interfaces directly with the CDP1802 Microprocessor without additional components**
- **Full- or half-duplex operation**
- **Baud rate— DC to 200K baud @ V_{DD}=5 V**
  DC to 400K baud @ V_{DD}=10 V
- **Fully programmable with externally selectable word length (5-8 bits), parity inhibit, even/odd parity, and 1, 1½, or 2 stop bits**
- **False start bit detection**
- **Parity, framing, and overrun error detection**
- **Low quiescent and operating power**
- **Single-voltage supply**
- **Wide operating-voltage range**
- **Full military temperature range: −55 to +125°C**

RECOMMENDED OPERATING CONDITIONS at T_A=25°C Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	V_{DD} (V)	TYPICAL VALUES		UNITS
		CDP1854D	CDP1854CD	
Supply-Voltage Range (At T_A=Full Package-Temperature Range)	–	3 to 12	4 to 6	V
Recommended Input Voltage Range	–	V_{SS} to V_{DD}	V_{SS} to V_{DD}	V
Clock Input Rise or Fall Time, t_r or t_f	3-15	5	5	μs
Clock Input Frequency, f_{CL} (16 times bit rate)	5	DC–3.2	DC–3.2	MHz
	10	DC–6.4	–	
Minimum Clock Pulse Width, t_{WL}, t_{WH}	5	150	150	ns
	10	75	–	
Minimum Master Reset, $\overline{CLEAR}$ Pulse Width	5	500	500	ns
	10	250	–	

ELECTRICAL CHARACTERISTICS at T_A=25°C

CHARACTERISTIC	CONDITIONS		TYPICAL VALUES		UNITS
	V_O (V)	V_{DD} (V)	CDP1854D	CDP1854CD	
Quiescent Device Current, I_L	–	5	100	500	μA
	–	10	500	–	
	–	15	1000	–	
Output Voltage: Low-Level, V_{OL}	–	5	0.01	0.01	V
	–	10	0.01	〃	
High-Level, V_{OH}	–	5	5	5	
	–	10	10	–	
Noise Immunity: Inputs Low, V_{NL}	0.5	5	2.25	2.25	V
	1	10	3.45	–	
Inputs High, V_{NH}	4.5	5	2.25	2.25	
	9	10	3.45	–	
Output Drive Current: N-Channel (Sink), I_DN	0.4	5	0.4	0.4	mA
	0.5	10	0.9	–	
P-Channel (Source), I_DP	2.5	5	–1.6	–1.6	
	4.6	5	–0.4	–0.4	
	9.5	10	–0.9	–	
Input Leakage Current (Any Input), I_{IL}, I_{IH}	–	5	±1	±1	μA
	–	15	±1	–	
Total Power Dissipation (f_{CL}=3.2 MHz)	–	5	5	7	mW
	–	10	15	–	

STANDARD MODE 0 (See Fig. 2)

RECOMMENDED OPERATING CONDITIONS at T_A=25°C Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	CONDITIONS	TYPICAL VALUES		UNITS
	V_{DD} (V)	CDP1854D	CDP1854CD	
Control Register Load (CRL) Pulse Width, t_{CLW}	5	200	200	ns
	10	150	–	
Transmitter Holding Register Load (THRL) Pulse Width, t_{TLW}	5	200	200	ns
	10	150	–	
Data Available Reset ($\overline{DAR}$) Pulse Width	5	200	200	ns
	10	150	–	
Input Data Setup Time, t_{DS}	5	150	150	ns
	10	75	–	
Input Data Hold Time, t_{DH}	5	150	150	ns
	10	75	–	
Control Input Overlap, t_{CLO} With CRL	5	200	200	ns
	10	100	–	
Control Input Hold Time, t_{CH}	5	100	100	ns
	10	50	–	

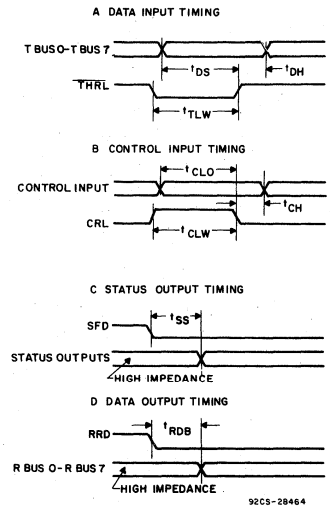


Fig. 2 – Standard Mode 0 timing diagrams.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C, C_L=50 pF

CHARACTERISTIC	CONDITIONS	TYPICAL VALUES		UNITS
	V_{DD} (V)	CDP1854D	CDP1854CD	
Status Flag Disconnect, (SFD) to STATUS OUT Delay, t_{SS}	5	200	200	ns
	10	100	–	
Receiver Register Disconnect, (RRD) to DATA OUT Delay, t_{RDB}	5	200	200	ns
	10	100	–	

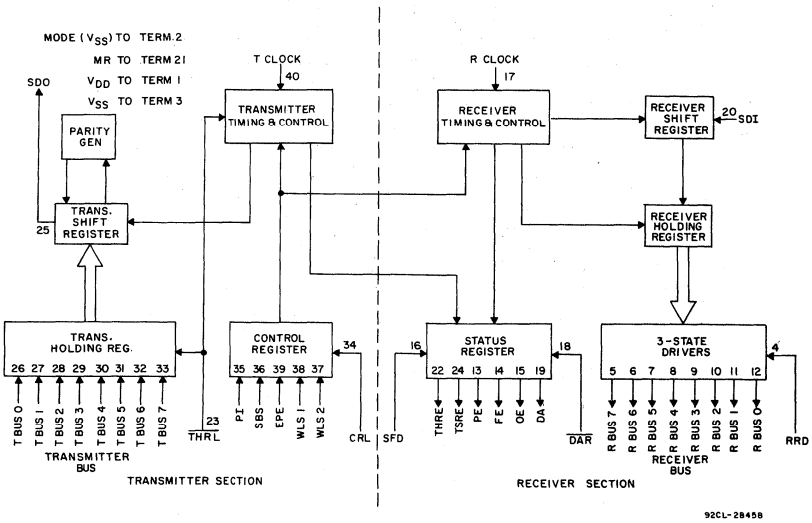


Fig. 3 – Standard Mode 0 block diagram.

Standard MODE 0 Operation (MODE Input = V_{SS})

1. Initialization and Controls

The MASTER RESET (MR) input is pulsed, resetting the Control, Status, and Receiver Holding Registers and setting the SERIAL DATA OUTPUT (SDO) signal high. Timing is generated from the clock inputs, Transmitter Clock (TCLOCK) and Receiver Clock (RCLOCK), at a frequency equal to 16 times the serial data bit rate. When the receiver data input rate and the transmitter data output rate are the same, the TCLOCK and RCLOCK inputs may be connected together. The CONTROL REGISTER LOAD (CRL) input is pulsed to store the control inputs PARITY INHIBIT (PI), EVEN PARITY ENABLE (EPE), STOP BIT SELECT (SBS), and WORD LENGTH SELECTs (WLS1 and WLS2). These inputs may be hardwired to the proper voltage levels (V_{SS} or V_{DD}) instead of being dynamically set and CRL may be hardwired to V_{DD}. The CDP1854 is then ready for transmitter and/or receiver operation.

2. Transmitter Operation

For the transmitter timing diagram refer to Fig. 4. At the beginning of a typical transmitting sequence the Transmitter Holding Register is empty (THRE is HIGH). A character is transferred from the transmitter bus to the Transmitter Holding Register by applying a low pulse to the TRANSMITTER HOLDING REGISTER LOAD ($\overline{THRL}$) input causing THRE to go low. If the Transmitter Shift Register is empty (TSRE is HIGH) and the clock is low, on the next high-to-low transition of the clock the character is loaded into the Transmitter Shift Register preceded by a start bit. Serial data transmission begins ½ clock period later with a start bit and 5-8 data bits followed by the parity bit (if programmed) and stop bit(s). The THRE output signal goes high ½ clock period later on the high-to-low transition of the clock. When THRE goes high, another character can be loaded into the Transmitter Holding Register for transmission beginning with a start bit immediately following the last stop bit of the previous character. This process is repeated until all characters have been transmitted. When transmission is complete, THRE and Transmitter Shift Register Empty (TSRE) will both be high. The format of serial data is shown in Fig. 5. Duration of each serial output data bit is determined by the transmitter clock frequency (f_{CLOCK}) and will be 16/f_{CLOCK}.

3. Receiver Operation

The receive operation begins when a start bit is detected at the SERIAL DATA IN (SDI) input. After the detection of a high-to-low transition on the SDI line, a divide-by-16 counter is enabled and a valid start bit is verified by checking for a low-level input 6½ receiver clock periods later. When a valid start bit has been verified, the following data bits, parity bit (if programmed), and stop bit(s) are shifted into the Receiver Shift Register at clock pulse 6½ in each bit time. If programmed, the parity bit is checked, and receipt of a valid stop bit is verified. On count 6½ of the first stop bit, the received data is loaded into the Receiver Holding Register. If the word length is less than 8 bits, zeros (low output voltage level) are loaded into the unused left-most bits. If DATA AVAILABLE (DA) has not been reset by the time the Receiver Holding Register is loaded, the OVERRUN ERROR (OE) signal is raised. One-half clock period later, the PARITY ERROR (PE) and FRAMING ERROR (FE) signals become valid for the character in the Receiver Holding Register. The DA signal is also raised at this time. The 3-state output drivers for DA, OE, PE and FE are enabled when STATUS FLAG DISCONNECT (SFD) is low. When RECEIVER REGISTER DISCONNECT (RRD) goes low, the receiver bus 3-state output drivers are enabled and data is available at the RECEIVER BUS (R BUS 0-R BUS 7) outputs. Applying a negative pulse to the DATA AVAILABLE RESET ($\overline{DAR}$) resets DA. The preceding sequence of operation is repeated for each serial character received. A receiver timing diagram is shown in Fig. 6.

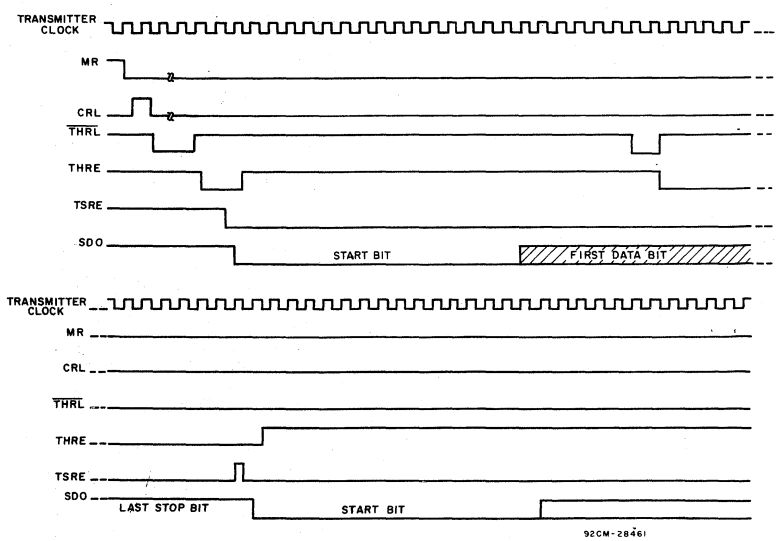


Fig. 4 — Transmitter timing diagram.

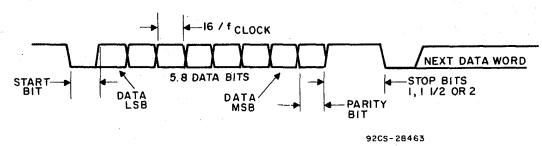


Fig. 5 — Serial data word format.

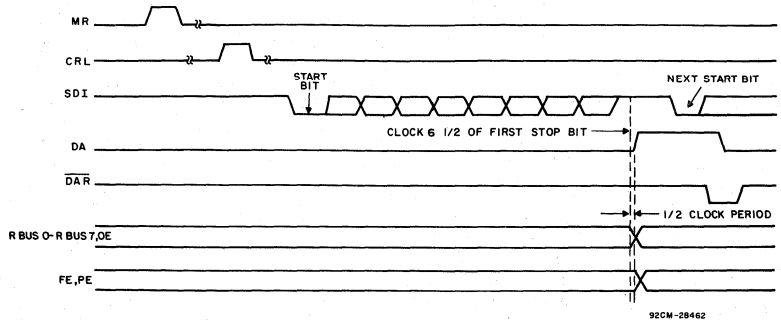


Fig. 6 – Receiver timing diagram.

Signal Definitions – Standard Mode 0

Terminal No.	Signal	Function
1	V_{DD}	Positive supply
2	MODE SELECT (MODE)	A low-level voltage at this input selects Standard Mode 0 Operation.
3	V_{SS}	Ground
4	RECEIVER REGISTER DISCONNECT (RRD)	A high-level voltage applied to this input disconnects the Receiver Holding Register from the Receiver Bus.
5-12	RECEIVER BUS (R BUS 7 - R BUS 0)	Receiver parallel data outputs
13	PARITY ERROR (PE)	A high-level voltage at this output indicates that the received parity does not compare to that programmed by the EVEN PARITY ENABLE (EPE) control. This output is updated each time a character is transferred to the Receiver Holding Register. PE lines from a number of arrays can be bused together since an output disconnect capability is provided by the STATUS FLAG DISCONNECT (SFD) line.
14	FRAMING ERROR (FE)	A high-level voltage at this output indicates that the received character has no valid stop bit, i.e., the bit following the parity bit (if programmed) is not a high-level voltage. This output is updated each time a character is transferred to the Receiver Holding Register. FE lines from a number of arrays can be bused together since an output disconnect capability is provided by the STATUS FLAG DISCONNECT (SFD) line.
15	OVERRUN ERROR (OE)	A high-level voltage at this output indicates that the DATA AVAILABLE (DA) flag was not reset before the next character was transferred to the Receiver Holding Register. OE lines from a number of arrays can be bused together since an output disconnect capability is provided by the STATUS FLAG DISCONNECT (SFD) line.
16	STATUS FLAG DISCONNECT (SFD)	A high-level voltage applied to this input disables the 3-state output drivers for PE, FE, OE, DA, and THRE, allowing these status outputs to be bus connected.
17	RECEIVER CLOCK (RCLOCK)	Clock input with a frequency 16 times the desired receiver shift rate.
18	DATA AVAILABLE RESET ($\overline{DAR}$)	A low-level voltage applied to this input resets the DA flip-flop.

19	DATA AVAILABLE (DA)	A high-level voltage at this output indicates that an entire character has been received and transferred to the Receiver Holding Register.
20	SERIAL DATA IN (SDI)	Serial data received at this input enters the receiver shift register at a point determined by the character length. A high-level voltage must be present when data is not being received.
21	MASTER RESET (MR)	A high-level voltage at this input resets the Receiver Holding Register, Control Register, and Status Register, and sets the serial data output high.
22	TRANSMITTER HOLDING REGISTER EMPTY (THRE)	A high-level voltage at this output indicates that the Transmitter Holding Register has transferred its contents to the Transmitter Shift Register and may be reloaded with a new character.
23	TRANSMITTER HOLDING REGISTER LOAD ($\overline{\text{THRL}}$)	A low-level voltage applied to this input enters the character on the bus into the Transmitter Holding Register. Data is latched on the trailing edge of this signal.
24	TRANSMITTER SHIFT REGISTER EMPTY (TSRE)	A high-level voltage at this output indicates that the Transmitter Shift Register has completed serial transmission of a full character including stop bit(s). It remains at this level until the start of transmission of the next character.
25	SERIAL DATA OUTPUT (SDO)	The contents of the Transmitter Shift Register (start bit, data bits, parity bit, and stop bit(s)) are serially shifted out on this output. When no character is being transmitted, a high-level is maintained. Start of transmission is defined as the transition of the start bit from a high-level to a low-level output voltage.
26-33	TRANSMITTER BUS (T BUS 0 - T BUS 7)	Transmitter parallel data inputs
34	CONTROL REGISTER LOAD (CRL)	A high-level voltage at this input loads the Control Register with the control bits (PI, EPE, SBS, WLS1, WLS2). This line may be strobed or hardwired to a high-level input voltage.
35	PARITY INHIBIT (PI)	A high-level voltage at this input inhibits the parity generation and verification circuits and will clamp the PE output low. If parity is inhibited the stop bit(s) will immediately follow the last data bit on transmission.
36	STOP BIT SELECT (SBS)	This input selects the number of stop bits to be transmitted after the parity bit. A high-level selects two stop bits, a low-level selects one stop bit. Selection of two stop bits with five data bits programmed selects 1.5 stop bits.
37	WORD LENGTH SELECT 2 (WLS2)	These two inputs select the character length (exclusive of parity) as follows:
38	WORD LENGTH SELECT 1 (WLS1)	**WLS2 / WLS1 / Word Length** Low / Low / 5 Bits Low / High / 6 Bits High / Low / 7 Bits High / High / 8 Bits
39	EVEN PARITY ENABLE (EPE)	A high-level voltage at this input selects even parity to be generated by the transmitter and checked by the receiver. A low-level input selects odd parity.
40	TRANSMITTER CLOCK (TCLOCK)	Clock input with a frequency 16 times the desired transmitter shift rate.

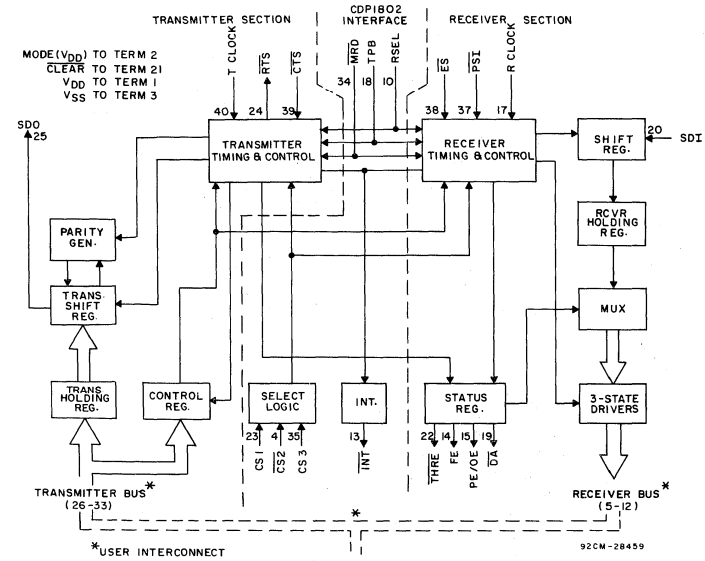


Fig. 7 – MODE 1 block diagram (CDP1802 compatible).

CDP1802 Compatible MODE 1 Operation (MODE Input = V_{DD})

1. Initialization and Controls

In the CDP1802 compatible mode, the CDP-1854 is configured to receive commands and send status via the microprocessor data bus. The register connected to the transmitter bus or the receiver bus is determined by the $\overline{MRD}$ and RSEL inputs as follows:

RSEL	$\overline{MRD}$	Function
Low	Low	Load Transmitter Holding Register from Transmitter Bus
Low	High	Read Receiver Holding Register from Receiver Bus
High	Low	Load Control Register from Transmitter Bus
High	High	Read Status Register from Receiver Bus

In this mode the CDP1854 is compatible with a bidirectional bus system. The receiver and transmitter buses are connected to the bus. CDP1802 I/O control output signals can be connected directly to the CDP1854 inputs as shown in Fig. 8. The $\overline{CLEAR}$ input is pulsed, resetting the Control, Status, and Receiver Holding Registers and setting SERIAL DATA OUT (SDO) high. The Control Register is loaded from the Transmitter Bus in order to determine the operating configuration for the UART. Data is transferred from the Transmitter Bus inputs to the Control Register during TPB when the UART is selected (CS1 · $\overline{CS2}$ · CS3) and the Control Register is designated (RSEL = H, $\overline{MRD}$ = L). The CDP1854 also has a Status Register which can be read onto the Receiver Bus (R BUS 0-R BUS 7) in order to determine the status of the UART. Some of these status bits are also available at separate terminals as indicated in Fig. 10.

2. Transmitter Operation

Before beginning to transmit, the TRANSMIT REQUEST (TR) bit in the Control Register (see bit assignment, page 10) must be set. This setting is done by executing the same operation used to load the Control Register except that the TR bit must be set (TR=1) in the byte transmitted via the bus. When TR has been set, a TRANSMITTER HOLDING REGISTER EMPTY (THRE) interrupt will occur, signalling the microprocessor that the Transmitter Holding Register is empty and may be loaded. Setting TR also causes assertion of a low-level on the REQUEST TO SEND ($\overline{RTS}$) output to the peripheral. The Transmitter Holding Register is loaded from the bus by TPB during execution of an output instruction. The CDP1854 is selected by CS1 · $\overline{CS2}$ · CS3 = 1, and the Holding Register is selected by RSEL = low and $\overline{MRD}$ = low. When the $\overline{CLEAR\ TO\ SEND}$ ($\overline{CTS}$) input, which can be connected to a peripheral device output, goes low, the Transmitter Shift Register will be loaded from the Transmitter Holding Register and data transmission will begin. If $\overline{CTS}$ is always low, the Transmitter Shift Register will be loaded on the first high-to-low edge of the clock which occurs at least ½ clock period after the trailing edge of TPB and transmission of a start bit will occur ½ clock period later (see Fig. 4). Parity (if programmed) and stop bit(s) will be transmitted following the last data bit.

One transmitter clock period after the Transmitter Shift Register is loaded from the Transmitter Holding Register, the $\overline{THRE}$ signal will go low and an interrupt will occur ($\overline{INT}$ goes low). The next character to be transmitted can then be loaded into the Transmitter Holding Register for transmission with its start bit immediately following the last stop bit of the previous character. This cycle can be repeated until the last character is transmitted, at which time a final THRE · TSRE interrupt will occur. This interrupt signals the microprocessor that TR can be turned off. This is done by reloading the original control byte in the Control Register with the TR bit = 0, thus terminating the $\overline{REQUEST\ TO\ SEND}$ ($\overline{RTS}$) signal.

SERIAL DATA OUT (SDO) can be held low by setting the BREAK bit in the Control Register (see Fig. 9). SDO is held low until the BREAK bit is reset.

3. Receiver Operation

The receive operation begins when a start bit is detected at the SERIAL DATA IN (SDI) input. After detection of the first high-to-low transition on the SDI line, a valid start bit is verified by checking for a low-level input 6½ receiver clock periods later. When a valid start bit has been verified, the following data bits, parity bit (if programmed) and stop bit(s) are shifted into the Receiver Shift Register by clock pulse 6½ in each bit time. The parity bit (if programmed) is checked and receipt of a valid stop bit is verified. On count 6½ of the first stop bit, the received data is loaded into the Receiver Holding Register. If the word length is less than 8 bits, zeros (low output level) are loaded into the unused left-most bits. If DATA AVAILABLE ($\overline{DA}$) has not been reset by the time the Receiver Holding Register is loaded, the OVERRUN ERROR (OE) status bit is set. One half clock period later, the PARITY ERROR (PE) and FRAMING ERROR (FE) status bits become valid for the character in the Receiver Holding Register. At this time, the Data Available status bit is also set and the $\overline{DATA\ AVAILABLE}$ ($\overline{DA}$) and $\overline{INTERRUPT}$ ($\overline{INT}$) outputs go low, signalling the microprocessor that a received character is ready. The microprocessor responds by executing an input instruction. The UART's 3-state bus drivers are enabled when the UART is selected (CS1 · $\overline{CS2}$ · CS3 = 1) and $\overline{MRD}$ = high. Status can be read when RSEL = high. Data is read when RSEL = low. When reading data, TPB latches data in the microprocessor and resets $\overline{DATA\ AVAILABLE}$ ($\overline{DA}$) in the UART. The preceding sequence is repeated for each serial character which is received from the peripheral.

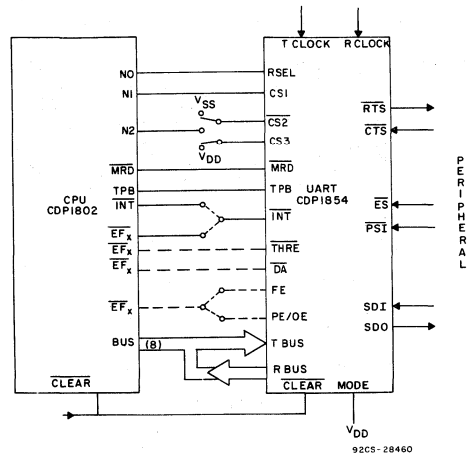


Fig. 8 – CDP1802/CDP1854 connection diagram.

Bit	7	6	5	4	3	2	1	0
Signal	TR	BREAK	IE	WLS2	WLS1	SBS	EPE	PI

Control Register Bit Assignment

Bit	Signal	Function
0	PARITY INHIBIT (PI)	When set high parity generation and verification are inhibited and the PE Status bit is held low. If parity is inhibited the stop bit(s) will immediately follow the last data bit on transmission, and EPE is ignored.
1	EVEN PARITY ENABLE (EPE)	When set high, even parity is generated by the transmitter and checked by the receiver. When low, odd parity is selected.
2	STOP BIT SELECT (SBS)	See table below.
3	WORD LENGTH SELECT 1 (WLS1)	See table below.
4	WORD LENGTH SELECT 2 (WLS2)	See table below.

Bit 4 WLS2	Bit 3 WLS1	Bit 2 SBS	Function
0	0	0	5 data bits, 1 stop bit
0	0	1	5 data bits, 1.5 stop bits
0	1	0	6 data bits, 1 stop bit
0	1	1	6 data bits, 2 stop bits
1	0	0	7 data bits, 1 stop bit
1	0	1	7 data bits, 2 stop bits
1	1	0	8 data bits, 1 stop bit
1	1	1	8 data bits, 2 stop bits

5	INTERRUPT ENABLE (IE)	When set high THRE, DA, THRE • TSRE, $\overline{CTS}$, and PSI interrupts are enabled (see Interrupt Conditions table, Fig. 11).
6	TRANSMIT BREAK (BREAK)	Holds SDO spacing (low) when set.
7	TRANSMIT REQUEST (TR)	When set high, $\overline{RTS}$ is set low and data transfer through the transmitter is initiated by the initial THRE interrupt. (When loading the Control Register from the bus, this (TR) bit inhibits changing of other control flip-flops.)

Fig. 9 – Control Register bit assignment.

Peripheral Interface

In addition to serial data in and out, four signals are provided for communication with a peripheral. The REQUEST TO SEND (RTS) output signal alerts the peripheral to get ready to receive data. The CLEAR TO SEND (CTS) input signal is the response, signalling that the peripheral is ready. The EXTERNAL STATUS (ES) input latches a peripheral status level, and the PERIPHERAL STATUS INTERRUPT (PSI) input senses a status edge (high-to-low) and also generates an interrupt. For example, the modem DATA CARRIER DETECT line could be connected to the PSI input on the UART in order to signal the microprocessor that transmission failed because of loss of the carrier on the communications line. The PSI and ES bits are stored in the Status Register (see Fig. 10).

Bit	7	6	5	4	3	2	1	0
Signal	THRE	TSRE	PSI	ES	FE	PE	OE	DA
Also Available at Terminal	22*	–	–	–	14	15	15	19*

* Polarity reversed at output terminal.

Status Register Bit Assignment Table

Bit	Signal	Function
0	DATA AVAILABLE (DA)	When set high, this bit indicates that an entire character has been received and transferred to the Receiver Holding Register. This signal is also available at Term.19 but with its polarity reversed.
1	OVERRUN ERROR (OE)	When set high, this bit indicates that the Data Available bit was not reset before the next character was transferred to the Receiver Holding Register. This signal OR'ed with PE is output at Term.15.
2	PARITY ERROR (PE)	When set high, this bit indicates that the received parity bit does not compare to that programmed by the EVEN PARITY ENABLE (EPE) control. This bit is updated each time a character is transferred to the Receiver Holding Register. This signal OR'ed with OE is output at Term.15.
3	FRAMING ERROR (FE)	When set high, this bit indicates that the received character has no valid stop bit, i.e., the bit following the parity bit (if programmed) is not a high-level voltage. This bit is updated each time a character is transferred to the Receiver Holding Register. This signal is also available at Term.14.
4	EXTERNAL STATUS (ES)	This bit is set high by a low-level input at Term.38 (ES).
5	PERIPHERAL STATUS INTERRUPT (PSI)	This bit is set high by a high-to-low voltage transition at Term.37 (PSI). The INTERRUPT output (Term.13) is also asserted (INT = low) when this bit is set.
6	TRANSMITTER SHIFT REGISTER EMPTY (TSRE)	When set high, this bit indicates that the Transmitter Shift Register has completed serial transmission of a full character including stop bit(s). It remains set until the start of transmission of the next character.
7	TRANSMITTER HOLDING REGISTER EMPTY (THRE)	When set high, this bit indicates that the Transmitter Holding Register has transferred its contents to the Transmitter Shift Register and may be reloaded with a new character. Setting this bit also resets the THRE output (Term.22) low and causes an INTERRUPT (INT = low).

Fig. 10 – Status Register bit assignment.

SET* ($\overline{INT}$ = LOW)	RESET ($\overline{INT}$ = HIGH)	
CAUSE	CONDITION	TIME
DA (Receipt of data)	Read of data	TPB leading edge
THRE▲ (Ability to reload)	Read of status or write of character	TPB leading edge
THRE • TSRE (Transmitter done)	Read of status or write of character	TPB leading edge
$\overline{PSI}$ (Negative edge)	Read of status	TPB trailing edge
$\overline{CTS}$ (Positive edge when $\overline{THRE \cdot TSRE}$)	Read of status	TPB leading edge

* Interrupts will occur only after the IE bit in the Control Register (see Fig. 9) has been set.

▲ THRE will cause an interrupt only after the TR bit in the Control Register (see Fig. 9) has been set.

Fig. 11 – Interrupt conditions.

Signal Definitions – CDP1802 Compatible Mode 1

Terminal No.	Signal	Function
1	V_{DD}	Positive supply
2	MODE SELECT (MODE)	A high-level voltage at this input selects CDP1802 Mode operation.
3	V_{SS}	Ground
4	$\overline{CHIP\ SELECT\ 2}$ ($\overline{CS2}$)	A low-level voltage at this input together with CS1 and CS3 selects the CDP1854 UART.
5-12	RECEIVER BUS (R BUS 7 - R BUS 0)	Receiver parallel data outputs (may be externally connected to corresponding transmitter bus terminals).
13	$\overline{INTERRUPT}$ ($\overline{INT}$)	A low-level voltage at this output indicates the presence of one or more of the interrupt conditions listed in Fig. 11.
14	FRAMING ERROR (FE)	A high-level voltage at this output indicates that the received character has no valid stop bit, i.e., the bit following the parity bit (if programmed) is not a high-level voltage. This output is updated each time a character is transferred to the Receiver Holding Register.
15	PARITY ERROR or OVERRUN ERROR (PE/OE)	A high-level voltage at this output indicates that either the PE or OE bit in the Status Register has been set (see Status Register Bit Assignment, Fig. 10).
16	REGISTER SELECT (RSEL)	This input is used to choose either the Control/Status Registers (high input) or the transmitter/receiver data registers (low input) according to the truth table on page 8.
17	RECEIVER CLOCK (RCLOCK)	Clock input with a frequency 16 times the desired receiver shift rate.
18	TPB	A positive input pulse used as a data load or reset strobe.
19	$\overline{DATA\ AVAILABLE}$ ($\overline{DA}$)	A low-level voltage at this output indicates that an entire character has been received and transferred to the Receiver Holding Register.
20	SERIAL DATA IN (SDI)	Serial data received on this input line enters the Receiver Shift Register at a point determined by the character length. A high-level input voltage must be present when data is not being received.

21	$\overline{\text{CLEAR}}$ ($\overline{\text{CLEAR}}$)	A low-level voltage at this input resets the Receiver Holding Register, Control Register, and Status Register, and sets SERIAL DATA OUT (SDO) high.
22	$\overline{\text{TRANSMITTER HOLDING REGISTER EMPTY}}$ ($\overline{\text{THRE}}$)	A low-level voltage at this output indicates that the Transmitter Holding Register has transferred its contents to the Transmitter Shift Register and may be reloaded with a new character.
23	CHIP SELECT 1 (CS1)	A high-level voltage at this input together with $\overline{\text{CS2}}$ and CS3 selects the UART.
24	$\overline{\text{REQUEST TO SEND}}$ ($\overline{\text{RTS}}$)	This output signal tells the peripheral to get ready to receive data. $\overline{\text{CLEAR TO SEND}}$ ($\overline{\text{CTS}}$) is the response from the peripheral. $\overline{\text{RTS}}$ is set to a low-level voltage when data is latched in the Transmitter Holding Register and reset high when both the Transmitter Holding Register and Transmitter Shift Register are empty and TR is low.
25	SERIAL DATA OUTPUT (SDO)	The contents of the Transmitter Shift Register (start bit, data bits, parity bit, and stop bit(s) are serially shifted out on this output. When no character is being transmitted, a high level is maintained. Start of transmission is defined as the transition of the start bit from a high-level to a low-level output voltage.
26-33	TRANSMITTER BUS (T BUS 0 - T BUS 7)	Transmitter parallel data inputs. These may be externally connected to corresponding Receiver bus terminals.
34	$\overline{\text{MRD}}$	A low-level voltage at this input gates data from the bus to the Transmitter Holding Register or the Control Register as chosen by register select. A high-level voltage gates data from the Receiver Holding Register or the Status Register, as chosen by register select, to the bus.
35	CHIP SELECT 3 (CS3)	With high-level voltage at this input together with CS1 and $\overline{\text{CS2}}$ selects the UART.
36	No Connection	
37	$\overline{\text{PERIPHERAL STATUS INTERRUPT}}$ (PSI)	A high-to-low transition on this input line sets a bit in the Status Register and causes an INTERRUPT (INT = low).
38	$\overline{\text{EXTERNAL STATUS}}$ ($\overline{\text{ES}}$)	A low-level voltage at this input sets a bit in the Status Register.
39	$\overline{\text{CLEAR TO SEND}}$ ($\overline{\text{CTS}}$)	When this input from peripheral is high, transfer of a character to the Transmitter Shift Register and shifting of serial data out is inhibited.
40	TRANSMITTER CLOCK (TCLOCK)	Clock input with a frequency 16 times the desired transmitter shift rate.

Preliminary Data

4-Bit Bus Buffers/Separators

The RCA-CDP1856D, CDP1856CD, CDP-1857D, and CDP1857CD are 4-bit COS/MOS non-inverting bus separators designed for use in CDP1800-series microprocessor systems. They can be controlled directly by the CDP1802 microprocessor without the use of additional components.

The CDP1856 is designed for use as a bus buffer or separator between the CDP1802 data bus and memories. The CDP1857 is designed for use as a bus buffer or separator between the CDP1802 data bus and I/O devices. Both types provide a chip-select (CS) input signal which, when high (1), enables the bus-separator three-state output drivers. The direction of data flow, when enabled, is controlled by the $\overline{MRD}$ input signal.

In the CDP1856, when the $\overline{MRD}$ signal = 0 (low), it enables the three-state bus drivers (DB0 – DB3) and outputs data from the DATA-IN terminals to the data bus. When $\overline{MRD}$ = 1 (high), it disables the three-state bus drivers and enables the three-state data output drivers (DO0-DO3), thus transferring data from the data bus to the DATA-OUT terminals.

In the CDP1857, when $\overline{MRD}$ = 1, it enables the three-state bus drivers (DB0-DB3) and transfers data from the DATA-IN lines onto the data bus. When MRD = 0, it disables the three-state bus drivers (DB0-DB3) and enables the three-state data output drivers (DO0-DO3), thus transferring data from the data bus to the DATA-OUT terminals.

The CDP1856 or CDP1857 can be used as a bi-directional bus buffer by connecting the corresponding DI and DO terminals (Fig.2).

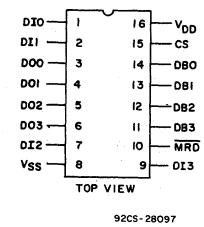
The $\overline{MRD}$ output signal from the CDP1802 microprocessor has the correct polarity to control the CDP1856 when this device is used as a memory data bus buffer/separator, or the CDP1857 when it is used as an I/O bus buffer/separator. Therefore, the CDP1802 $\overline{MRD}$ signal can be connected directly to the $\overline{MRD}$ input of either device. See Function Tables 1 and 2 in Fig.3 for use of the CDP1856 as a memory data bus buffer/separator and CDP1857 as an I/O bus buffer/separator.

The CDP1856D and CDP1857D are functionally identical to the CDP1856CD and CDP1857CD, respectively. The CDP1856D and CDP1857D have a recommended operating-voltage range of 3 to 12 volts, and the CDP1856CD and CDP1857CD have a recommended operating-voltage range of 4 to 6 volts.

The CDP1856D, CDP1856CD, CDP1857D and CDP1857CD are supplied in 16-lead hermetic, dual-in-line ceramic packages.

Features:

- **Static Silicon-Gate CMOS circuitry – CD4000-series compatible**
- **Compatible with CDP1800-series microprocessors at maximum speed**
- **Provides easy connection of memory and I/O devices to CDP1802 microprocessor data bus.**
- **Single voltage supply**
- **Full military-temperature range (–55°C to +125°C)**
- **Low quiescent and operating power**
- **Non-inverting fully buffered data transfer**



Terminal Assignment

OPERATING CONDITIONS at T_A = 25°C Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITIONS	LIMITS				UNITS
	V_{DD} (V)	CDP1856D CDP1857D		CDP1856CD CDP1857CD		
		Min.	Max.	Min.	Max.	
Supply Voltage Range (At T_A = Full Package-Temperature Range)	–	3	12	4	6	V
Recommended Input Voltage Range	–	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	TEST CONDITIONS		LIMITS		UNITS
			CDP1856D CDP1857D	CDP1856CD CDP1857CD	
	V_O (V)	V_{DD} (V)	Typical Values	Typical Values	
Dynamic: t_r,t_f=10 ns, C_L=100 pF					
Propagation Delay Time: $\overline{MRD}$ or CS to DO, t_{ED}		5	150	150	ns
		10	75	–	
$\overline{MRD}$ or CS to DB, t_{EB}		5	150	150	ns
		10	75	–	
DI to DB, t_{IB}		5	100	100	ns
		10	50	–	
DB to DO, t_{BD}		5	100	100	ns
		10	50	–	

MAXIMUM RATINGS,
Absolute-Maximum Values

Storage-Temperature Range (T_{stg}) . . . . . –65 to +150°C

Operating-Temperature Range (T_A) . . . . . –55 to +125°C

DC Supply-Voltage Range (V_{DD})
(All voltage values referenced to V_{SS} terminal)
CDP1856D, CDP1857D . . . –0.5 to +15 V
CDP1856CD, CDP1857CD . . –0.5 to +7 V

Power Dissipation Per Package (P_D):
For T_A = –55 to +100°C . . . . . 500 mW
For T_A = +100 to +125°C . . . . . Derate linearly to 200 mW

Device Dissipation Per Output Transistor:
For T_A = –55°C to +125°C 100 mW

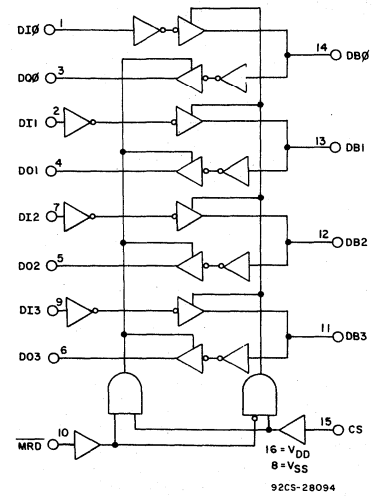
Input Voltage Range, All Inputs . . . . . –0.5 to V_{DD} +0.5 V

Lead Temperature (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

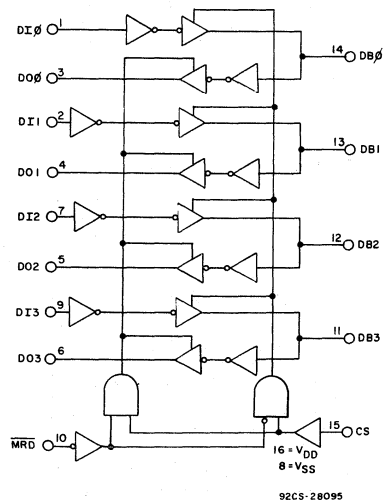
CDP1856D, CDP1856CD, CDP1857D, CD1857CD

ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$

CHARACTERISTIC	TEST CONDITIONS			LIMITS		UNITS
				CDP1856D CDP1857D	CDP1856CD CDP1857CD	
		V_O (V)	V_{DD} (V)	Typical Values	Typical Values	
Static						
Quiescent Device Current, I_L		–	5	50	100	μA
		–	10	100	–	
		–	15	500	–	
Output Voltage: Low-Level, V_{OL}		–	5-10	0.01	0.01	V
High-Level, V_{OH}		–	5	4.99	4.99	
		–	10	9.99	–	
Noise Margin: V_{NML}	Any Input	0.5	5	1	1	V
		1	10	1.5	–	
V_{NMH}	Any Input	4.5	5	1	1	
		9	10	1.5	–	
Output Drive Current: N-Channel (Sink), I_{DN}	Any Output	0.4	5	1.8	1.8	mA
		0.5	10	3.6	–	
P-Channel (Source), I_{DP}	Any Output	4.6	5	–1.6	–1.6	
		9.5	10	–3.6	–	
Data Output Off-Resistance, R_O(Off)	CS Low	–	5-10	5	5	MΩ
Input Leakage, I_{IL}, I_{IH}	Any Input	–	5-10	1	1	μA



CDP1856 – Functional Diagram



CDP1857 – Functional Diagram

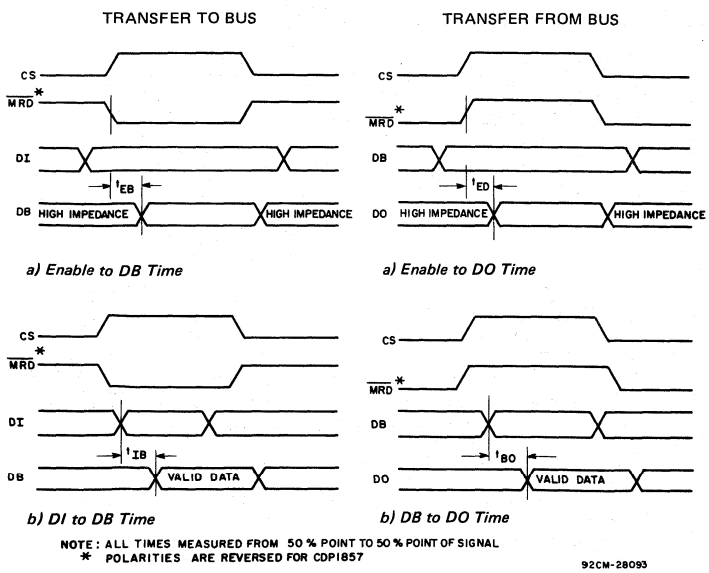


Fig. 1 – Timing Diagrams for CDP1856.

TYPICAL APPLICATIONS

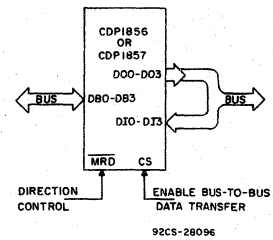
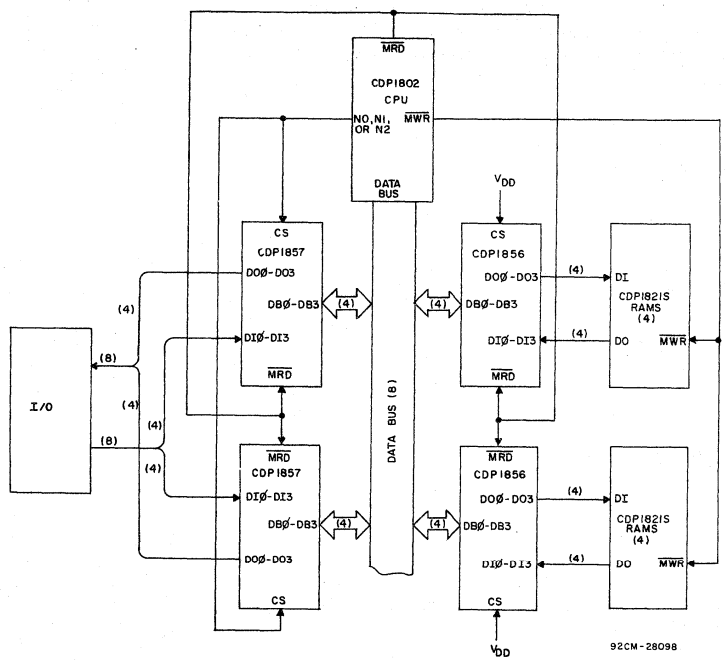


Fig. 2 – CDP1856, CDP1857 Bidirectional Bus Buffer Operation.



CDP1857 FUNCTION TABLE
For I/O Bus Separator Operation

CS	$\overline{MRD}$	DATA BUS OUT DB0 – DB3	DATA OUT DO0 – DO3
0	X	HIGH IMPEDANCE	HIGH IMPEDANCE
1	0	HIGH IMPEDANCE	DATA BUS
1	1	DATA IN	HIGH IMPEDANCE

CDP1856 FUNCTION TABLE
For Memory Data Bus Separator Operation

CS	$\overline{MRD}$	DATA BUS OUT DB0 – DB3	DATA OUT DO0 – DO3
0	X	HIGH IMPEDANCE	HIGH IMPEDANCE
1	0	DATA IN	HIGH IMPEDANCE
1	1	HIGH IMPEDANCE	DATA BUS

Fig. 3 – CDP1856 and CDP1857 Bus Separator Operation.

CDP1858D, CD1858CD, CDP1859D, CDP1859CD

4-Bit Latch With Decode

Preliminary Data

RCA-CDP1858D, CDP1858CD, CDP1859D, and CDP1859CD are 4-bit latch decode circuits designed for use in CDP1800 series microprocessor systems. These devices have been specifically designed for use as memory-system decoders and interface directly with the CDP1802 microprocessor multiplexed address bus at maximum clock frequency.

The CDP1858D and CDP1859D are functionally identical to the CDP1858CD and CDP1859CD, respectively. The CDP1858D and CDP1859D have a recommended operating-voltage range of 3 to 12 volts, and the CDP1858CD and CDP1859CD have a recommended operating-voltage range of 4 to 6 volts.

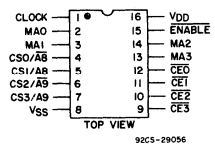
The CDP1858 interfaces the CDP1802 address bus and up to 32 CDP1822S 256 x 4 RAM's to provide a 4k byte RAM system. No additional components are required. The CDP1858 generates the chip selects required by the CDP1822S RAM. The chip select outputs are a function of the address bits connected to inputs MA0 through MA3.

The MA0 – MA3 address bits are latched at the trailing edge of TPA (generated by the CDP1802). When ENABLE = 1 (V_{DD}), the CS outputs = 0 (V_{SS}), and the CE outputs = 1. When ENABLE = 0, the outputs are enabled and correspond to the binary decode of the inputs. The ENABLE input can be used for memory system expansion.

The CDP1858 is also compatible with non-multiplexed address bus microprocessors. By connecting the CLOCK input to 1 (V_{DD}), the latches are in the data following mode and the decoded outputs can be used in general-purpose memory-system applications.

Features:

- **Compatible with CDP1800-series microprocessors at maximum speed**
- **Static Silicon-Gate CMOS circuitry – CD4000-series compatible**
- **Provides easy connection of memory devices to CDP1802 microprocessor**
- **Single voltage supply**
- **Full military-temperature range (–55°C to +125°C)**
- **Low quiescent and operating power**
- **Non-inverting fully buffered data transfer**



TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE (V_{DD})
(All voltage values referenced to V_{SS} terminal):
- CDP1858D, CDP1859D . . . . . –0.5 to +15 V
- CDP1858CD, CDP1859CD . . . . . –0.5 to +7 V

POWER DISSIPATION PER PACKAGE (P_D):
- FOR T_A = –55 to +100°C . . . . . 500 mW
- FOR T_A = +100 to +125°C . . . . . Derate linearly to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
- FOR T_A = –55°C to +125°C . . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
OPERATING-TEMPERATURE RANGE (T_A) . . . . . –55 to +125°C
STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
- At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . 265°C

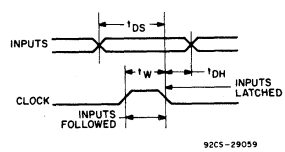
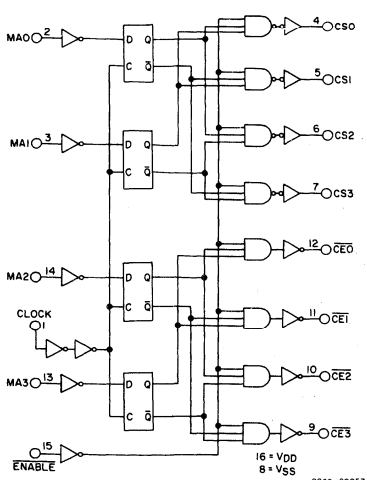
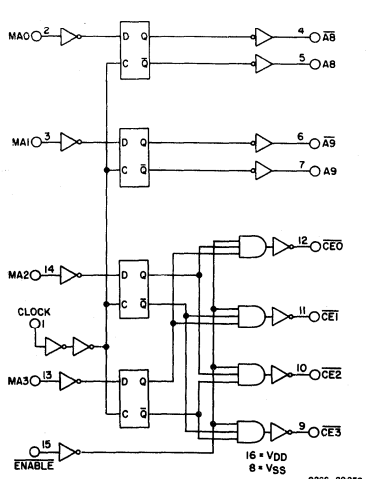


Fig. 1 – CDP1858, CDP1859 timing diagram.



CDP1858 – Functional Diagram



CDP1859 – Functional Diagram

The CDP1859 interfaces the CDP1802 address bus and up to 32 CDP1821S 1024 x 1 RAM's to provide a 4k byte RAM system. The CDP1859 generates the chip selects required by the CDP1821S RAM. The chip select outputs are a function of the address bits connected to inputs MA2 and MA3. The address bits connected to inputs MA0 and MA1 are latched by the trailing edge of TPA (generated by the CDP1802) to provide the two additional address lines required by the CDP1821S when used in a CDP1802-based system. When ENABLE = 1, the CE outputs are 1's; when ENABLE = 0, and CE outputs are enabled and correspond to the binary decode of the MA2 and MA3 inputs. ENABLE does not affect the latching or state of outputs A8, $\overline{A8}$, A9, or $\overline{A9}$.

The CDP1858D, CDP1858CD, CDP1859D, and CDP1858CD are supplied in hermetic 16-lead dual-in-line ceramic packages.

CDP1858 DECODE TRUTH TABLE

$\overline{ENABLE}$	DATA INPUTS		CE0	CS1	CS2	CS3	$\overline{CE0}$	$\overline{CE1}$	$\overline{CE2}$	$\overline{CE3}$
	MA1	MA0								
0	0	0	1	0	0	0	NOT AFFECTED BY MA1, MA0			
0	0	1	0	1	0	0				
0	1	0	0	0	1	0				
0	1	1	0	0	0	1				
	MA3	MA2								
0	0	0	NOT AFFECTED BY MA3, MA2				0	1	1	1
0	0	1					1	0	1	1
0	1	0					1	1	0	1
0	1	1					1	1	1	0
1	X	X	0	0	0	0	1	1	1	1

X = MA3, MA2, MA1, MA0 DON'T CARE

CDP1859 DECODE TRUTH TABLE

$\overline{ENABLE}$	DATA INPUTS		A8	A9	$\overline{A8}$	$\overline{A9}$	$\overline{CE0}$	$\overline{CE1}$	$\overline{CE2}$	$\overline{CE3}$
	MA1	MA0								
0	0	0	0	0	1	1	NOT AFFECTED BY MA1, MA0			
0	0	1	0	1	1	0				
0	1	0	1	0	0	1				
0	1	1	1	1	0	0				
	MA3	MA2								
0	0	0	NOT AFFECTED BY MA3, MA2				0	1	1	1
0	0	1					1	0	1	1
0	1	0					1	1	0	1
0	1	1					1	1	1	0
1	X	X	NOT AFFECTED BY $\overline{ENABLE}$				1	1	1	1

X = MA3, MA2, MA1, MA0 DON'T CARE

RECOMMENDED CONDITIONS at T_A = 25°C Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITIONS	LIMITS				UNITS
	V_{DD} (V)	CDP1858D CDP1859D		CDP1858CD CDP1859CD		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (At T_A = Full Package-Temperature Range)	–	3	12	4	6	V
Recommended Input Voltage Range	–	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
CLOCK Pulse Width, t_W		Typical		Typical		ns
	5	150		150		
	10	75		–		
Data Setup Time, t_{DS}	5	100		100		ns
	10	50		–		
Data Hold Time, t_{DH}	5	25		25		ns
	10	10		–		

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	TEST CONDITIONS		TYPICAL VALUES		UNITS
	V_O (V)	V_{DD} (V)	CDP1858D CDP1859D	CDP1858CD CDP1859CD	
Quiescent Device Current, I_L (Max.)	–	5	50	100	μA
	–	10	100	–	
	–	15	500	–	
Output Drive Current: (Min.)	0.4	5	1.6	1.6	mA
N-Channel (Sink), I_DN	0.5	10	3.6	–	
P-Channel (Source), I_DP	4.6	5	−1.6	−1.6	
	9.5	10	−3.6	–	

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, t_r, t_f = 10 ns, C_L = 100 pF

CHARACTERISTIC	TEST CONDITIONS		TYPICAL VALUES		UNITS
		V_{DD}	CDP1858D	CDP1858CD	
Propagation Delay Time: CLOCK (Low-to-High) to Any Output	$\overline{ENABLE}$ = 0	5	220	220	ns
		10	110	–	
$\overline{ENABLE}$ (High-to-Low) to Any Output	CLOCK = 1	5	170	170	ns
		10	85	–	
$\overline{ENABLE}$ (Low-to-High) to Any Output	CLOCK = 1	5	170	170	ns
		10	85	–	
MA0, MA1 to CE0,CS1, CS2, or CS3	CLOCK = 1, $\overline{ENABLE}$ = 0	5	200	200	ns
		10	90	–	
MA2, MA3 to $\overline{CE0}$, $\overline{CE1}$, $\overline{CE2}$, or $\overline{CE3}$	CLOCK = 1, $\overline{ENABLE}$ = 0	5	200	200	ns
		10	90	–	
			CDP1859D	CDP1859CD	
Propagation Delay Time: CLOCK (Low-to-High) to A8, A9, $\overline{A8}$, or $\overline{A9}$		5	200	200	ns
		10	100	–	
CLOCK (Low-to-High) to $\overline{CE0}$, $\overline{CE1}$, $\overline{CE2}$, or $\overline{CE3}$	$\overline{ENABLE}$ = 0	5	220	220	ns
		10	110	–	
$\overline{ENABLE}$ (High-to-Low) to $\overline{CE0}$, $\overline{CE1}$, $\overline{CE2}$, or $\overline{CE3}$	CLOCK = X	5	170	170	ns
		10	85	–	
$\overline{ENABLE}$ (Low-to-High) to $\overline{CE0}$, $\overline{CE1}$, $\overline{CE2}$, or $\overline{CE3}$	CLOCK = X	5	170	170	ns
		10	85	–	
MA0, MA1 to A8, A9, $\overline{A8}$, or $\overline{A9}$	CLOCK = X	5	150	150	ns
		10	75	–	
MA2, MA3 to $\overline{CE0}$, $\overline{CE1}$, $\overline{CE2}$, or $\overline{CE3}$	CLOCK = 1, $\overline{ENABLE}$ = 0	5	200	200	ns
		10	90	–	

X = Don't care

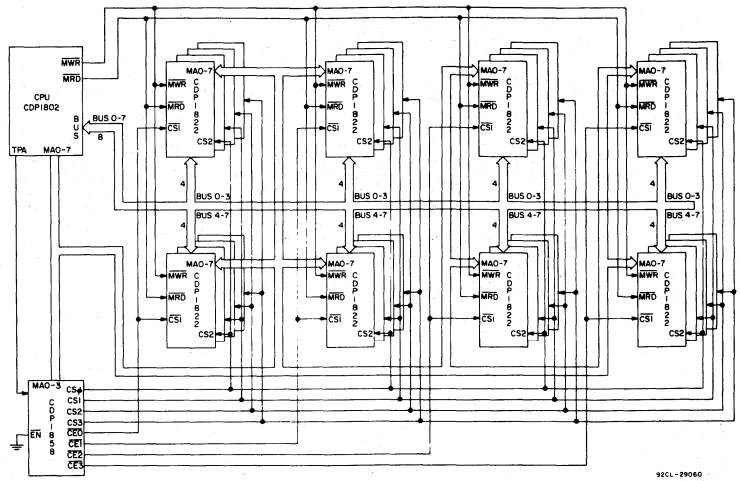


Fig. 2 – 4K byte RAM system using the CDP1858 and CDP1822.

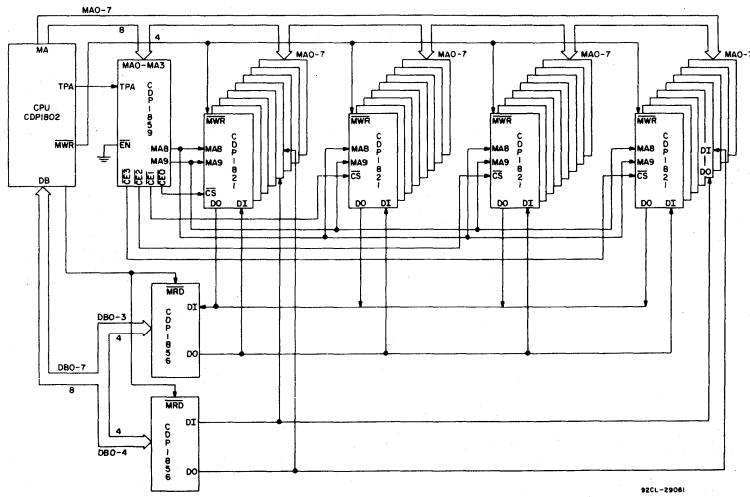


Fig. 3 – 4K byte RAM system using the CDP1859, CDP1856, and CDP1821.

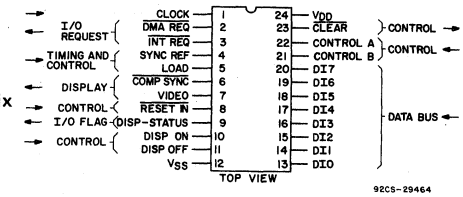
CDP1861CD

Preliminary Data

Video Display Controller

Features:

- Static silicon-gate CMOS circuitry
- Interfaces directly with CDP1802 microprocessor
- Supports bit-mapped video display for graphic flexibility
- Generates composite horizontal and vertical sync
- Programmable vertical resolution for matrix display of up to 64 x 128 segments
- Real-time interrupt generator
- Clear input
- External display control
- Single voltage supply (4 - 6 volts)
- Low quiescent and operating power
- Full military operating temperature range (–55 to +125°C)



TERMINAL ASSIGNMENT

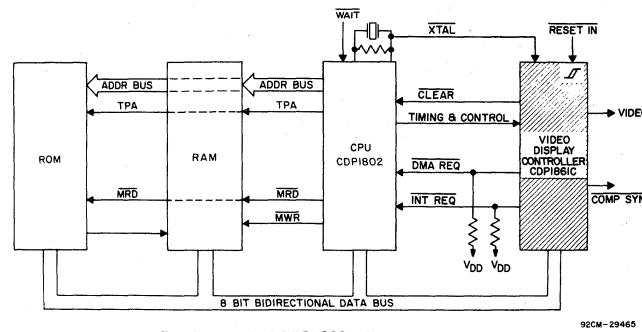


Fig. 1 – Typical CDP1802 microprocessor system.

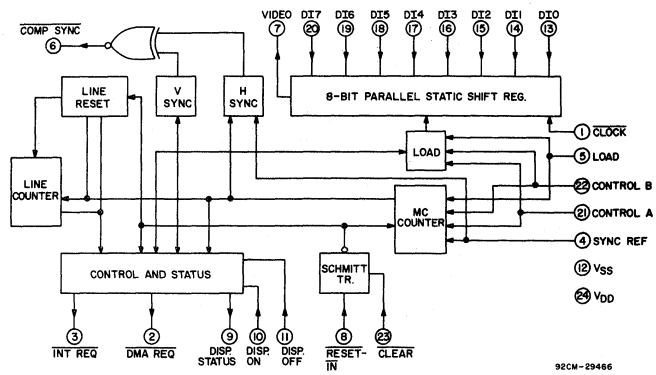


Fig. 2 – CDP1861C block diagram.

The CDP1861C is a video display controller designed for use in CDP1800-series microprocessor systems. It is compatible with the CDP1802 microprocessor and will interface directly with the CDP1802 as shown in the system diagram (Fig. 1).

The CDP1861C utilizes many of the features of the CDP1802 to simplify control and minimize the need for external components. The DMA feature of the CDP1802 may be used for direct data transfers from memory to the CDP1861C. The INTERRUPT input and the I/O command lines may be used to perform the necessary handshaking between the CDP-1802 and the CDP1861C. Timing may be simplified by operating the microprocessor at a clock frequency of 1.76064-MHz (the standard color frequency of 3.58 MHz, divided by 2, may also be used in some applications). The clock and the CDP1802 timing signals (TPA and TPB) may then be used to set the interface timing as shown in the system diagram. In general, the clock frequency equals the number of fields per second (60), times the number of lines per field (262), times the number of machine cycles per line (14), times the number of bits per byte (8). In DMA operation, each machine cycle is a memory access.

Flexibility in vertical resolution may be obtained by synchronizing the CDP1861C with the CDP1802, and employing direct program control over the DMA process in real time. The actual video display takes place during a "window" of 4.6 milliseconds out of each 16.7-millisecond TV field. Throughout each such display window, a CDP1802 interrupt program may be used to manipulate the DMA pointer, re-issuing a given line of the display several times to save memory storage at the expense of reduced vertical resolution.

The CDP1861C generates composite vertical and horizontal sync plus luminance signals which can be combined externally to create an NTSC compatible composite video signal. This composite vertical and horizontal sync output signal ($\overline{\text{COMP SYNC}}$) is generated from the sync reference (SYNC REF) and LOAD inputs. Vertical sync is derived from horizontal sync by dividing the horizontal sync frequency by 262. The composite sync signal generates timing for a non-interlace video display of 262 lines per field.

The CDP1861C generates an interrupt request ($\overline{\text{INT REQ}}$) once per field, 60 lines after the trailing edge of vertical sync and two lines before the raster has reached a "display window" (see Fig. 5). This request alerts the CDP1802 (or other control system) to prepare for DMA (direct memory access) activity. The CDP1861C DISP STATUS output goes low during the 4 lines before the display window, and again during the last 4 lines of the window. This signal may be used to give early warning of the display window and to release the control system from monitoring the DMA activity.

Beginning in the third machine cycle of each line of the display window, and lasting for 8 cycles, the CDP1861C asserts the $\overline{\text{DMA REQ}}$ output to request a sequence of eight 8-bit bytes, which are then used to generate the $\overline{\text{VIDEO}}$ signal. Then, when control signals A and B are low and high respectively, each assertion of the LOAD input causes the CDP-1861C to read a byte from the BUS lines, and immediately to shift it out on the $\overline{\text{VIDEO}}$ output, high-order bit first. A DMA pointer defines an area of memory which is accessed by the CDP1861C to provide a bit-mapped display.

The display on (DISP ON) and display off (DISP OFF) inputs set and reset an internal control flip-flop in the CDP1861C. When this flip-flop is set, $\overline{\text{DMA REQ}}$ and $\overline{\text{INT REQ}}$ are enabled; when reset, they are disabled.

The reset input ($\overline{\text{RESET IN}}$) is a Schmitt trigger input that resets the CDP1861C. The $\overline{\text{CLEAR}}$ output is a conditioned output pulse which can be used to reset the external system.

The CDP1861C is supplied in a 24-lead dual-in-line ceramic package.

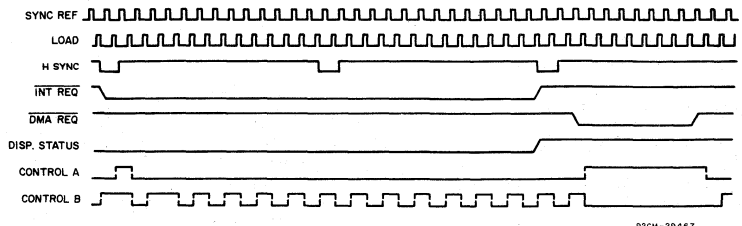


Fig. 3 – Horizontal sync timing diagram.

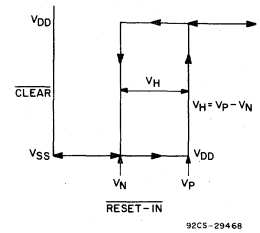


Fig. 4 – Reset transfer characteristics.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE (V_{DD})
(All voltage values referenced to V_{SS} terminal) ..... –0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... –0.5 to V_{DD} +0.5 V
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = –55 to +100°C ..... 500 mW
For T_A = +100 to +125°C ..... Derate Linearly to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = –55°C to +125°C ..... 100 mW
STORAGE-TEMPERATURE RANGE (T_{stg}) ..... –65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A) ..... –55 to +125°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	TYPICAL VALUES	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	–	4 - 6	V
Input Voltage Range	–	V_{SS} – V_{DD}	V
Input Signal Rise or Fall Time	5	5	μs
Clock Input Frequency, f_{CL}	5	0 - 2.5	MHz

ELECTRICAL CHARACTERISTICS AT T_A = 25°C

CHARACTERISTIC		CONDITIONS V_O (V)	CONDITIONS V_{DD} (V)	TYPICAL VALUES	UNITS
Maximum Quiescent Device Current, I_L		–	5	500	μA
Minimum Output Drive Current:					
Video or Sync	N-Channel (Sink), I_{DN}	0.4	5	1.2	mA
	P-Channel (Source), I_{DP}	4.5	5	1	
Reset Out or Flag	N-Channel (Sink), I_{DN}	0.4	5	–0.4	mA
	P-Channel (Source), I_{DP}	4.5	5	0.4	
I/O Requests;	N-Channel (Sink), I_{DN}	0.4	5	–0.2	mA
Reset-In:					
Positive Trigger Threshold, V_P		–	5	2.5	V
Negative Trigger Threshold, V_N		–	5	1.7	V
Hysteresis Voltage, V_H		–	5	0.8	V

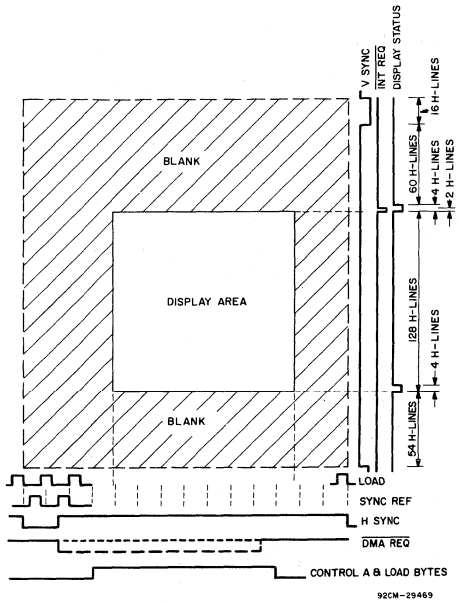


Fig. 5 – Spatial diagram of one video display field (not to scale).

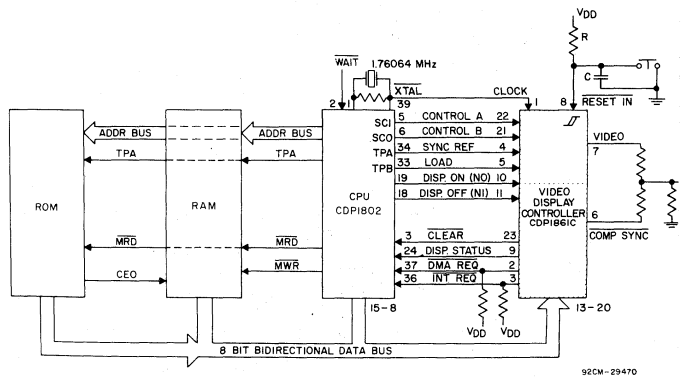


Fig. 6 – Typical CDP1802/CDP1861C video display system.

Application Information (CDP1861C directly controlled by the CDP1802 microprocessor)

Figure 6 shows a simple graphic display system using the CDP1802 and the CDP1861C. The CDP1861C uses both the INTERRUPT and direct memory access (DMA) output channel of the microprocessor for display refresh. The microprocessor specifies the area of memory displayed via the interrupt routines, and the DMA output channel is the mechanism which transfers the data from memory to the CDP1861C via the 8-bit data bus. The data are then shifted out one bit at a time at the clock frequency to generate the video ($\overline{\text{VIDEO}}$) signal.

The composite sync ($\overline{\text{COMP SYNC}}$) signal creates a 262-line-per-field, 60-field-per-second non-interlace video picture. The non-interlaced picture frame for this display consists of two even fields of 262 horizontal lines each. This format differs slightly from the National Television Standard (NTSC) which has a 525-line interlaced picture frame of one odd field and one even field. The vertical sync pulse generated at $\overline{\text{COMP SYNC}}$ of the CDP1861C has no equalizing pulses but is serrated to maintain horizontal synchronization during the vertical blanking time. The VIDEO and $\overline{\text{COMP SYNC}}$ pulses are resistively coupled to create the composite video, which can be supplied directly to a video monitor, a modified TV receiver, or an FCC approved rf modulator.

A clock source of 3.58 MHz, the NTSC color frequency, if divided by 2, may be used for some applications in place of the 1.76-MHz crystal shown in Fig. 6. Deviations from the NTSC frequencies are as follows:

NTSC		Clock Frequencies (MHz)		
		1.76064	1.764000	3.579545/2
Line Freq.	15750	15720	15750	15980
Field Freq.	60	60	60.11	60.99

The user should determine which choice of frequencies provides an optimal cost/performance trade-off for his application. Generally, video CRT's are more sensitive to line frequency accuracy than to field frequency accuracy.

The display is a bit map of memory. Each bit in the display memory corresponds to one spot on the video screen. Logical 1 (V_{DD}) bits in memory correspond to white or lighted spots in the display. The highest resolution that may be produced without any hardware modifications is 128 vertical by 64 horizontal segments. This resolution requires 1024 bytes of memory for the display. The upper left-most spot that can be displayed on the video screen is the most significant bit of the first byte in the display refresh memory buffer. The starting location of the display buffer is initialized in the INTERRUPT routine and may be anywhere in addressable memory (ROM, RAM, or both). The lower right-most spot that can be displayed is the least significant bit of the last byte of the display bit map. For each of the 128 horizontal display lines, 8 bytes of memory are sequentially accessed and displayed from left to right on the video screen. Adjacent illuminated spots appear contiguous both in the horizontal and in the vertical directions.

All display manipulations are accomplished by changing the data within the display buffer or by changing display buffers.

To control the CDP1861C as shown in Fig. 6, the CDP1802 must be in synchronization with the CDP1861C during the display window. Exactly six machine cycles must be executed beyond the eight DMA cycles during each line, and an even number of cycles (262 x 14) must be executed from the start of one display window to the start of the next. These requirements insure that the DMA bursts will not be delayed one cycle waiting for an instruction to finish—this delay would cause jitter on the screen. These requirements can be accomplished in two steps: 1) the main program must not execute any 3-cycle instructions (i.e., SKIPS, LONG BRANCHES, and NOP), and 2) the interrupt routine, including the interrupt cycle itself, must employ an even number of cycles, and must be synchronized with the DMA bursts. There must be 29 cycles between the INTERRUPT cycle (S3) and the first burst of eight DMA cycles. This timing is accomplished by executing an early 3-cycle instruction to compensate for the INTERRUPT cycle. Furthermore, exactly three 2-cycle instructions must be executed between each

successive burst. Occasionally these restrictions may be ignored at the expense of jitter on the screen.

For the 128 x 64 display, the CDP1802 software requirement is straightforward. The DISP STATUS/$\overline{EF1}$ line is not required, and EF1 may be used for other purposes. A simple interrupt routine merely resets the DMA pointer, RO, to the beginning of the display buffer area (see Fig. 5)—note the 3-cycle NOP instruction at the beginning which compensates for the 1-cycle interrupt. The first burst of eight DMA cycles occurs just as this routine finishes, as indicated by the bracket following the RETURN instruction (70). Exactly 29 cycles separate the interrupt request cycle and the first DMA burst. The interrupt routine must last at least 28 cycles, because the interrupt request line is held up that long by the CDP1861C.

When less RAM is to be used (less resolution), a more complicated interrupt routine is used. The interrupt routine is protracted for the full duration of the display window, and the six free cycles in each line are used to execute three instructions, which maintain control over the DMA pointer, RO.1. In the simplest cases, each line of 8 bytes is repeated n times to give 128/n vertical resolution. With n = 4, for example, 64 x 32 resolution is obtained. Such an interrupt routine is shown in Fig. 8. The code from the entry at INTERRUPT to DISPLAY is as in the last example. The use of three instructions per line does not leave time to control a loop, so each of four copies of the line corresponds to three instructions in the main loop, starting at DISPLAY STATUS. The DISPLAY STATUS signal, applied to EF1, is used to RO.1 in the last pass through the loop, when RO advances into the next page after each burst.

For other values of n, similar routines can be devised. For n = 2, the 64 x 64 format, the last 4 lines need special treatment (see Fig. 7). Other schemes are possible, resulting in other resolutions which vary on command from the main program, or even resolutions which vary through the display window.

In general, additional functions may be implemented in the routine before returning to the main program. For example, a real-time clock can be maintained by incrementing a counter once on each interrupt, i.e., once per 1/60 second. Another example is vertical "scrolling" of the display, wherein the starting address in a display file is incremented or reincremented at regular intervals.

Signal Definitions

Signal	Term.No.	Definition
$\overline{\text{RESET IN}}$	8	An input signal which, when low (V_{SS}), initializes the counters, inhibits the display, and places all control outputs in the high (V_{DD}) state. The $\overline{\text{RESET IN}}$ terminal is a Schmitt-trigger-type input which permits the use of an external RC network to provide a power-on reset.
$\overline{\text{CLEAR}}$	23	The output of the Schmitt trigger (reset input circuitry) provides high speed transitions that may be used to reset other devices. It may be connected to the $\overline{\text{CLEAR}}$ terminal of the CDP1802 microprocessor.
DISPLAY-ON DISPLAY-OFF	10 11	Positive input signals that control the display. When enabled (DISPLAY-ON = V_{DD}), data transfers, DMA, and interrupt requests are permitted. These operations are inhibited by the low-to-high transition of the DISPLAY-OFF input signal if DISPLAY-ON = V_{SS}. The $\overline{\text{RESET IN}}$ signal also inhibits the display. When inhibited, the internal counters remain operational. Sync and display status signals are generated. Video output becomes low when the register is emptied. Table I indicates the enable/disable conditions.

Table I

STATE	SIGNAL		
	$\overline{\text{RESET-IN}}$	DISPLAY-ON	DISPLAY-OFF
RESET	L	L	X
INVALID	L	H	X
TV ENABLE	H	H	X
TV DISABLE	H	L	⌐

The DISPLAY-ON and DISPLAY-OFF signals may be provided by the I/O commands (N bits) of the CDP1802 microprocessor.

CLOCK	1	The input for an externally generated single-phase clock which determines the clock rate for the 8-bit data shift register. Data are shifted on the high-to-low transition of the CLOCK input signal, most significant bit first. A low level ("0") is shifted into the least significant bit. The CLOCK signal may be derived directly from the CDP1802 microprocessor by connecting the CLOCK terminal of the CDP1861C to the XTAL terminal of the CDP1802.
SYNC REFERENCE LOAD	4 5	Positive timing pulses each occurring once for every 8 clock pulses. The SYNC REFERENCE signal precedes the LOAD signal. The SYNC REFERENCE signal is used as the clock for the horizontal line counter. The LOAD signal is used as a strobe for gating the output of the counter and for loading data into the data register. They are normally connected to the TPA and TPB terminals of the CDP1802 microprocessor.
$\overline{\text{COMP SYNC}}$	6	Negative (high going low) output signal resulting from the exclusive "OR" of the output of the horizontal and vertical counters. $\overline{\text{COMP SYNC}}$ can be combined with the $\overline{\text{VIDEO}}$ output to form a composite video signal. The $\overline{\text{COMP SYNC}}$ output frequency and pulse duration are determined by the SYNC REFERENCE and LOAD input signals. A horizontal sync pulse is initiated by the trailing edge of the LOAD input signal following the thirteenth or fourteenth SYNC REFERENCE input, as determined by the status of the CONTROL A and CONTROL B input signals, and is terminated on the leading edge of the subsequent second count of the SYNC REFERENCE input.

Signal Definitions (Cont'd)

Signal	Term.No.	Definition
		Vertical timing is generated coincident with the 262 horizontal timing pulse and is present for six horizontal clock cycles. Idealized timing is illustrated in Figs. 3 and 5.
$\overline{\text{INTERRUPT REQUEST}}$	3	A low (V_{SS}) output signal two horizontal cycles prior to the display, as shown in Figs. 3 and 5. This signal is the output of the "open drain" of an n-channel transistor and requires an external pull-up resistor to V_{DD}. The $\overline{\text{INTERRUPT REQUEST}}$ output signal is normally connected to the INTERRUPT input terminal of the CDP1802 microprocessor. In a CDP1802-based system 29 machine cycles occur from initiation of an $\overline{\text{INTERRUPT REQUEST}}$ until the $\overline{\text{DMA REQUEST}}$.
DISPLAY STATUS	9	A low (V_{SS}) output signal which occurs for a period of four horizontal cycles prior to the beginning and end of the 128-line display window, as illustrated in Figs. 3 and 5. The signal can be used by the program software routines to indicate the boundaries of the display area. It is normally connected to a CDP1802 FLAG input terminal.
$\overline{\text{DMA REQUEST}}$	2	A low output (V_{SS}) that requests an 8-bit data transfer. The output signal is from the "open drain" of an n-channel transistor and requires an external pull-up resistor to V_{DD}. Depending upon the status of the CONTROL A and CONTROL B input signals at horizontal sync time, DMA requests are initiated on the leading edge of the second SYNC REFERENCE input signal following the horizontal sync output. This feature is necessary in order to reference the data requests to the program's ability to respond to them, insuring that data will always be initiated at the same point on the display. The system should respond to a $\overline{\text{DMA REQUEST}}$ by setting CONTROL B high (V_{DD}), and CONTROL A low (V_{SS}) permitting data transfer. Data will be loaded on the subsequent 8 LOAD input signals. $\overline{\text{DMA REQUEST}}$ will be terminated on the ninth sync pulse, at which time CONTROL B should be set low (V_{SS}) prior to the next LOAD command. Timing is illustrated in Figs. 3 and 5. The $\overline{\text{DMA REQUEST}}$ output signal may be connected to the DMA IN terminal of the CDP1802 microprocessor, which responds as discussed above.
CONTROL A CONTROL B	22 21	Input signals used to synchronize the operation of the CDP1861C with its controller. They should be initiated prior to the SYNC REFERENCE input and terminate after the LOAD input pulse. The CONTROL signals are sampled at two different times: 1) During the horizontal sync output when the SYNC REFERENCE input is present, the CDP1861C expects to see CONTROL A = 1 (V_{DD}), and CONTROL B = 0 (V_{SS}). Any other combination will result in the skipping of one of the normal 14 cycles per line. This feature allows the CDP1802 to force initial instruction fetch/execute sync with the CDP1861C, and assures sync in case it is later lost for any reason. 2) In the 8 cycles following the CDP1861C $\overline{\text{DMA REQUEST}}$ assertion, the CDP1861C expects to see CONTROL A = 0, and CONTROL B = 1. Any other combination will prevent the CDP1861C from loading data from the bus. These signals may be connected to the STATE CODE outputs of the CDP1802 microprocessor; CONTROL A to SC0 and CONTROL B to SC1.

Signal Definitions (Cont'd)

Signal	Term.No.	Definition
DI7 - DI0	13-20	Input signals to the data register. Data are loaded during the high-to-low transition of the CLOCK only when LOAD = V_{DD} and the CDP1861C is enabled. DISPLAY-ON = 1 (V_{DD}), CONTROL A = 0 (V_{SS}), and CONTROL B = 1 (V_{DD}). The data input signals are normally connected to the 8-bit microprocessor data bus.
VIDEO	7	Output from the most significant bit of the data register. It is used to determine the luminance level and may be combined externally with the $\overline{\text{COMP SYNC}}$ output signal to form a composite video signal.

Machine Code	Assembly Language		Comments
72	INTRET:	LDXA	. . RESTORE D
70		RET	. . RETURN
C4	INT :	NOP	. . 3 CYC.INSTR.FOR PGM.SYNC
22		DEC R2	. . R2 IS STACK PTR
78		SAV	. . T → STACK
22		DEC R2	
52		STR R2	. . D → STACK
F8__B0		A.1(DISMEM) → RO.1	. . DISMEM IS START ADDR
F8__A0		A.0(DISMEM) → RO.0	. . OF DISPLAY MEMORY
C4, C4		NOP; NOP	. . NOPS FOR PGM SYNC
E2		SEX2	
80]	DISP :	GLO RO	. . NEW LINE
E2		SEX2	. . NOP
20		DEC RO	. . RESTORES RO.1 IF PASS PG
A0]		PLO RO	. . REPEATS SAME LINE
E2		SEX2	. . NOP
3C__		BN1 DISP	. . LOOP 60 TIMES
80]	DISEF :	GLO RO	. . LAST 4 VIDEO LINES
E2		SEX2	. . NOP
20 A0]		DEC RO; PLO RO	
E2		SEX2	. . NOP
34__		B1 DISEF	
30__		BR INTRET	. . END OF DISPLAY

Fig. 7 – Interrupt routine for 64 x 64 format (2 pgs mem).

Machine Code	Assembly Language		Comments
72	INTRET:	LDXA	. . RESTORE D
70		RET	. . RETURN
C4	INT :	NOP	. . 3 CYC. INSTR. USED . . FOR PGM. SYNC
22		DEC R2	. . R2 IS STACK PTR
78		SAV	. . T → STACK
22		DEC R2	
52		STR R2	. . D → STACK
F8__B0		A.1(DISMEM) → RO.1	. . LOAD RO WITH
F8__A0		A.0(DISMEM) → RO.0	. . START.ADDR.OF DISP.MEM
C4, C4		NOP; NOP	. . NOPS USED FOR SYNC
E2	DISP :	SEX2	
80]		GLO RO	. . LINE START ADDR. → D
E2		SEX2	. . NOP
20		DEC RO	. . RESET RO.1 IF PASS PG
A0]		PLO RO	. . LINE START ADDR. → RO.0
E2		SEX2	. . NOP
20		DEC RO	. . RESET RO.1 IF PASS PG
A0]		PLO RO	. . LINE START ADDR. → RO.0
E2		SEX2	. . NOP
20		DEC RO	. . RESET RO.1 IF PASS PG
A0		PLO RO	. . REPEATS SAME LINE
3C__		BN1 DISP	. . LOOPS 32 TIMES
30__		BR INTRET	. . END OF DISPLAY

Fig. 8 – Interrupt routine for 64 x 32 format (1 pg mem).

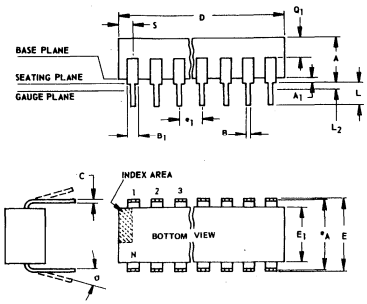
Machine Code	Assembly Language		Comments
72	INTRET:	LDXA	. . RESTORE D
70]		RET	. . RETURN
C4	INT :	NOP	. . ENTRY POINT
22		DEC R2	. . R2 = STACK PTR
78		SAV	. . T → STACK
22		DEC R2	
52		STR R2	. . D → STACK
E2, E2		SEX R2; SEX R2	. . NOP
F8__B0		A.1(DISMEM) → RO.1	. . LOAD RO WITH
F8__A0		A.0(DISMEM) → RO.0	. . START ADDR OF DISP.MEM.
30__		BR INTRET	. . OR INSERT OTHER COMMENT

Fig. 9 – Interrupt routine for 64 x 128 (4 pgs mem).

Dimensional Outlines

Dimensional Outlines

Ceramic Dual-In-Line Packages



NOTES:

Refer to JEDEC Publication No. 95 for Rules for Dimensioning Axial Lead Product Outlines.

1. When this device is supplied solder dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).
2. When base of body is to be attached to heat sink, terminal lead standoffs are not required and $A_1 = 0$. When $A_1 = 0$, the leads emerge from the body with the B_1 dimension and reduce to the B dimension above the seating plane.
3. e_1 and e_A apply in zone L_2 when unit is installed. Leads within 0.005 " (0.127 mm) radius of True Position (TP) at gauge plane with maximum material condition.
4. Applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

(D) Suffix
JEDEC MO-001-AD 14-Lead Welded-Seal

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.160		3.05	4.06
A_1	0.020	0.065		0.51	1.65
B	0.014	0.020		0.356	0.508
B_1	0.050	0.065		1.27	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.770		18.93	19.55
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	14		5	14	
N_1	0		6	0	
Q_1	0.050	0.085		1.27	2.15
S	0.065	0.090		1.66	2.28

92SS-4411R2

(D) Suffix
JEDEC MO-001-AE 16-Lead Welded-Seal

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.160		3.05	4.06
A_1	0.020	0.065		0.51	1.65
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.785		18.93	19.93
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	16		5	16	
N_1	0		6	0	
Q_1	0.050	0.085		1.27	2.15
S	0.015	0.060		0.39	1.52

92SS-4286R5

(D) Suffix
JEDEC MO-015-AG
24-Lead Welded-Seal

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.090	0.200		2.29	5.08
A_1	0.020	0.070	2	0.51	1.78
B	0.015	0.020		0.381	0.508
B_1	0.045	0.055		1.143	1.397
C	0.008	0.012	1	0.204	0.304
D	1.15	1.22		29.21	30.98
E	0.600	0.625		15.24	15.87
E_1	0.480	0.520		12.20	13.20
e_1	0.100 TP		3	2.54 TP	
e_A	0.600 TP		3	15.24 TP	
L	0.100	0.180		2.54	4.57
L_2	0.000	0.030	3	0.00	0.76
α	0°	15°	4	0°	15°
N	24		5	24	
N_1	0		6	0	
Q_1	0.020	0.080		0.51	2.03
S	0.020	0.060		0.51	1.52

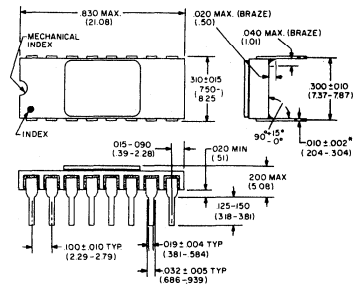
92CS-19948R2

(D) Suffix
JEDEC MO-015-AH
28-Lead Welded-Seal

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	.090	.200	2.29	5.0	2
A_1	.000	.070	0	1.77	
B	.015	.020	.381	.508	
B_1	.015	.055	.39	1.39	
C	.008	.012	.204	.304	
D	1.380	1.420	35.06	36.06	
E	.600	.625	15.24	15.87	
E_1	.485	.515	12.32	13.08	
e_1	.100 TP		2.54 TP		3
e_A	.600 TP		15.24 TP		3
L	.100	.200	2.6	5.0	
L_2	.000	.030	0	.76	
α	0	15	0°	15°	4
N	28		28		5
N_1	0		0		6
Q_1	.020	.070	.51	1.77	
S	.040	.070	1.02	1.77	
See Note	1				

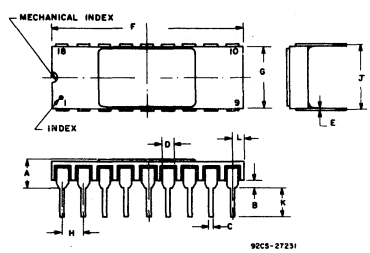
92CM-20250R1

(D) Suffix
16-Lead Side-Brazed



92CS-21219

(D) Suffix
18-Lead Side-Brazed



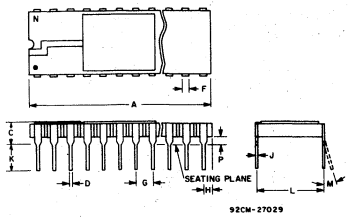
92CS-27231

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	–	0.200	–	5.08	
B	0.020	0.045	0.51	1.14	
C	0.015	0.021	0.381	0.533	
D	0.54		1.37		
E	0.008	0.012	0.204	0.304	1
F	0.890	0.915	22.61	23.24	
G	0.280	0.300	7.12	7.62	
H	0.100		2.54		2
J	0.300		7.62		2, 3
K	0.125	0.150	3.18	3.81	
L	0.035	0.065	0.89	1.65	

NOTES:

1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).
2. Leads within 0.005" (0.13 mm) radius of true position at maximum material condition.
3. Lead spacing (center to center) when formed parallel.

Ceramic Dual-In-Line Packages (Cont'd)



NOTES

1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. WHEN THIS DEVICE IS SUPPLIED SOLDER-DIPPED, THE MAXIMUM LEAD THICKNESS (NARROW PORTION) WILL NOT EXCEED 0.013" (0.33 mm).

(D) Suffix
22-Lead Side-Brazed

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	27.05	27.94	1.065	1.100
C	2.16	3.68	0.085	0.145
D	0.43	0.56	0.017	0.023
F	1.02 REF.		0.040 REF.	
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	3.18	4.45	0.125	0.175
L	9.65	10.67	0.380	0.420
M	–	7°	–	7°
P	0.64	1.27	0.025	0.050

(D) Suffix
40-Lead Side-Brazed

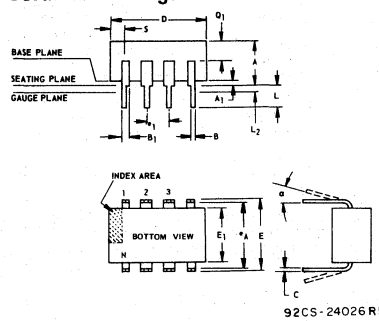
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	50.30	51.30	1.980	2.020
C	2.42	3.93	0.095	0.155
D	0.43	0.56	0.017	0.023
F	1.27 REF.		0.050 REF.	
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	3.18	4.45	0.125	0.175
L	14.74	15.74	0.580	0.620
M	–	7°	–	7°
P	0.64	1.27	0.025	0.050
N	40		40	

(D) Suffix
28-Lead Side-Brazed

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	35.06	36.06	1.380	1.420
C	2.16	3.68	0.085	0.145
D	0.43	0.56	0.017	0.023
F	1.27 REF.		0.050 REF.	
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	3.18	4.45	0.125	0.175
L	14.74	15.74	0.580	0.620
M	–	7°	–	7°
P	0.64	1.27	0.025	0.050
N	28		28	

92CM-26419

Dual-In-Line Plastic and Frit-Seal Ceramic Packages



NOTES:
Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.

1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

(E) Suffix
8-Lead Plastic (Mini-Dip)

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.508	1.27
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.889	1.65
C	0.008	0.012	1	0.203	0.304
D	0.370	0.400		9.40	10.16
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.762
α	0°	15°	4	0°	15°
N	8		5	8	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.015	0.060		0.381	1.52

Dual-In-Line Plastic and Frit-Seal Ceramic Packages (Cont'd)

(E) and (F) Suffixes
JEDEC MO-001-AB
14-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B_1	0.050	0.065		1.27	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.770		18.93	19.55
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	14		5	14	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.065	0.090		1.66	2.28

92SS-4296R3

(E) and (F) Suffixes
JEDEC MO-001-AC
16-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.785		18.93	19.93
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	16		5	16	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.015	0.060		0.39	1.52

92CM-15967R4

(E) and (F) Suffixes
JEDEC MO-015-AA 24-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.250		3.10	6.30
A_1	0.020	0.070	2	0.51	1.77
B	0.016	0.020		0.407	0.508
B_1	0.028	0.070		0.72	1.77
C	0.008	0.012	1	0.204	0.304
D	1.20	1.29		30.48	32.76
E	0.600	0.625		15.24	15.87
E_1	0.515	0.580		13.09	14.73
e_1	0.100 TP		3	2.54 TP	
e_A	0.600 TP		3	15.24 TP	
L	0.100	0.200		2.54	5.00
L_2	0.000	0.030	3	0.00	0.76
α	0°	15°	4	0°	15°
N	24		5	24	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.040	0.100		1.02	2.54

Dimensional Outlines (Cont'd)

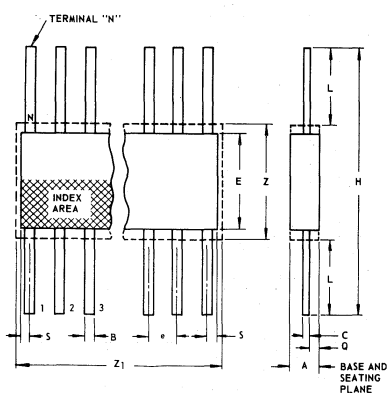
Dual-In-Line Plastic and Frit-Seal Ceramic Packages (Cont'd)

(F) Suffix
JEDEC MO-001-AG
16-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.165	0.210		4.20	5.33
A_1	0.015	0.045		0.381	1.14
B	0.015	0.020		0.381	0.508
B_1	0.045	0.070	7	1.15	1.77
C	0.009	*0.011		0.229	0.279
D	0.750	0.795		19.05	20.19
E	0.295	0.325		7.50	8.25
E_1	0.245	0.300		6.23	7.62
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.120	0.160		3.05	4.06
L_2	0.000	0.030		0.000	0.76
α	2°	15°	4	2°	15°
N	16		5	16	
N_1	0		6	0	
Q_1	0.050	0.080		1.27	2.03
S	0.010	0.060		0.254	1.52

92CM-22284

Ceramic Flat Packs



NOTES:
1. Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.
2. Leads within .005" (.12 mm) radius of True Position (TP) at maximum material condition.
3. N is the maximum quantity of lead positions.
4. Z and Z_1 determine a zone within which all body and lead irregularities lie.

Ceramic Flat Packs (Cont'd)

(K) Suffix
JEDEC MO-004-AF 14-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.008	0.100		0.21	2.54
B	0.015	0.019	1	0.381	0.482
C	0.003	0.006	1	0.077	0.152
e	0.050 TP		2	1.27 TP	
E	0.200	0.300		5.1	7.6
H	0.600	1.000		15.3	25.4
L	0.150	0.350		3.9	8.8
N	14		3	14	
Q	0.005	0.050		0.13	1.27
S	0.000	0.050		0.00	1.27
Z	0.300		4	7.62	
Z_1	0.400		4	10.16	

92SS-4300R3

(K) Suffix
JEDEC MO-004-AG 16-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.008	0.100		0.21	2.54
B	0.015	0.019	1	0.381	0.482
C	0.003	0.006	1	0.077	0.152
e	0.050 TP		2	1.27 TP	
E	0.200	0.300		5.1	7.6
H	0.600	1.000		15.3	25.4
L	0.150	0.350		3.9	8.8
N	16		3	16	
Q	0.005	0.050		0.13	1.27
S	0.000	0.025		0.00	0.63
Z	0.300		4	7.62	
Z_1	0.400		4	10.16	

92CS-17271R3

(K) Suffix
24-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.075	0.120		1.91	3.04
B	0.018	0.022	1	0.458	0.558
C	0.004	0.007	1	0.102	0.177
e	0.050 TP		2	1.27 TP	
E	0.600	0.700		15.24	17.78
H	1.150	1.350		29.21	34.29
L	0.225	0.325		5.72	8.25
N	24		3	24	
Q	0.035	0.070		0.89	1.77
S	0.060	0.110	1	1.53	2.79
Z	0.700		4	17.78	
Z_1	0.750		4	19.05	

92CS-19949R2

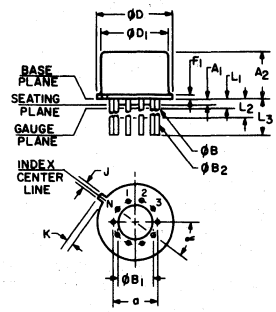
(K) Suffix
28-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.075	0.120		1.91	3.04
B	0.018	0.022	1	0.458	0.558
C	0.004	0.007	1	0.102	0.177
e	0.050 TP		2	1.27 TP	
E	0.600	0.700		15.24	17.78
H	1.150	1.350		29.21	34.29
L	0.225	0.325		5.72	8.25
N	28		3	28	
Q	0.035	0.070		0.89	1.77
S	0	0.060	1	0	1.53
Z	0.700		4	17.78	
Z_1	0.750		4	19.05	

92CS-20972

(T) Suffix TO-5 Style

(T) Suffix
JEDEC MO-006-AG 12-Lead TO-5 Style
(CD4062A Only)



92CS-19774

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
a	0.230		2	5.84 TP	
A_1	0	0		0	0
A_2	0.165	0.185		4.19	4.70
øB	0.016	0.019	3	0.407	0.482
$øB_1$	0	0		0	0
$øB_2$	0.016	0.021	3	0.407	0.533
øD	0.335	0.370		8.51	9.39
$øD_1$	0.305	0.335		7.75	8.50
F_1	0.020	0.040		0.51	1.01
j	0.028	0.034		0.712	0.863
k	0.029	0.045	4	0.74	1.14
L_1	0.000	0.050	3	0.00	1.27
L_2	0.250	0.500	3	6.4	12.7
L_3	0.500	0.562	3	12.7	14.27
α	30° TP			30° TP	
N	12		6	12	
N_1	1		5	1	

NOTES:
1. Refer to Rules for Dimensioning Axial Lead Product Outlines.
2. Leads at gauge plane within 0.007" (0.178 mm) radius of True Position (TP) at maximum material condition.
3. øB applies between L_1 and L_2. $øB_2$ applies between L_2 and 0.500" (12.70 mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.500" (12.70 mm).
4. Measure from Max. øD.
5. N_1 is the quantity of allowable missing leads.
6. N is the maximum quantity of lead positions.

Application Notes

The RCA COS/MOS Phase-Locked-Loop A Versatile Building Block for Micro-Power Digital and Analog Applications

INTRODUCTION

Phase-locked-loops (PLL's), especially in monolithic form, are finding significantly increased usage in signal-processing and digital systems. FM demodulation, FSK demodulation, tone decoding, frequency multiplication, signal conditioning, clock synchronization, and frequency synthesis are some of the many applications of a PLL. The PLL described in this Note is the COS/MOS CD4046A, which consumes only 600 microwatts of power at 10 kHz, a reduction in power consumption of 160 times when compared to the 100 milliwatts required by similar monolithic bipolar PLL's. This power reduction has particular significance for portable battery-operated equipment. This Note discusses the basic fundamentals of phase-locked-loops, and presents a detailed technical description of the COS/MOS PLL as well as some of its applications.

REVIEW OF PLL FUNDAMENTALS

The basic phase-locked-loop system is shown in Fig. 1; it consists of three parts: phase comparator, low-pass filter, and voltage-controlled oscillator (VCO); all are connected to form a closed-loop frequency-feedback system.

With no signal input applied to the PLL system, the error voltage at the output of the phase comparator is zero. The voltage, Vd(t), from the low-pass filter is also zero, which causes the VCO to operate at a set frequency, fo, called the center frequency. When an input signal is applied to the PLL, the phase comparator compares the phase and frequency of the signal input with the VCO frequency and generates an error voltage proportional to the phase and frequency

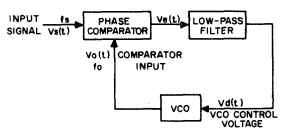


Fig. 1— Block diagram of PLL.

difference of the input signal and the VCO. The error voltage, Ve(t), is filtered and applied to the control input of the VCO; Vd(t) varies in a direction that reduces the frequency difference between the VCO and signal-input frequency. When the input frequency is sufficiently close to the VCO frequency, the closed-loop nature of the PLL forces the VCO to *lock* in frequency with the signal input; i.e., when the PLL is in lock, the VCO frequency is identical to the signal input except for a finite phase difference. The range of frequencies over which the PLL can maintain this locked condition is defined as the *lock range* of the system. The lock range is always larger than the band of frequencies over which the PLL can acquire a locked condition with the signal input. This latter band of frequencies is defined as the *capture range* of the PLL system.

TECHNICAL DESCRIPTION OF COS/MOS PLL

Fig. 2 shows a block diagram of the COS/MOS CD4046A, which has been implemented on a single monolithic integrated circuit. The PLL structure consists of a low-power, linear, voltage-controlled oscillator (VCO), and two different phase comparators having a common signal-input amplifier and a common comparator input. A 5.2-volt zener is provided for supply regulation if necessary. The VCO can be connected either directly or through frequency dividers to the comparator input of the phase comparators. The low-pass filter is implemented through external parts because of the radical configuration changes from application to application and because some of the components are non-integrable. The CD4046A is supplied in a 16-lead, dual-in-line, ceramic package (CD4046AD); a 16-lead, dual-in-line, plastic package (CD4046AE); or a 16-lead flat-pack (CD4046AK). It is also available in chip form (CD4046AH).

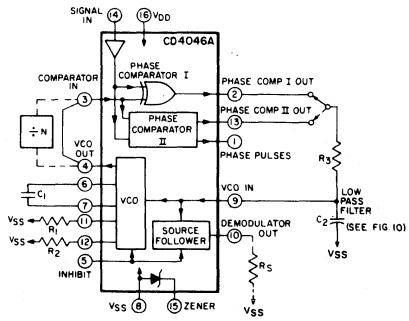


Fig. 2— COS/MOS PLL block diagram.

Phase Comparators

Most PLL systems utilize a balanced mixer composed of well-controlled analog amplifiers for the phase-comparator section. Analog amplifiers with well-controlled gain characteristics cannot easily be realized using COS/MOS technology. Hence, the COS/MOS design shown in Fig. 3 employs digital-type phase comparators. Both phase comparators are driven by a common-input amplifier configuration composed of a bias stage and four inverting-amplifier stages. The phase-comparator signal input (terminal 14) can be direct-coupled provided the signal swing is within COS/MOS logic levels [logic $0 \leq 30\%$ (VDD-VSS), logic $1 \geq 70\%$ (VDD-VSS)]. For smaller input signal swings, the signal must be capacitively coupled to the self-biasing amplifier at the signal input to insure an over-driven digital signal into the phase comparators.

Phase-comparator I is an exclusive-OR network; it operates analagously to an over-driven balanced mixer. To maximize the lock range, the signal and comparator input frequencies must have 50-percent duty cycle. With no signal or noise on the signal input, this phase comparator has

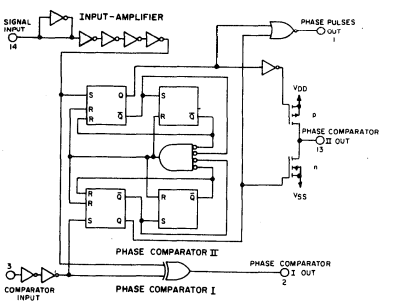


Fig. 3— Schematic of COS/MOS PLL phase-comparator section.

an average output voltage equal to VDD/2. The low-pass filter connected to the output of phase-comparator I supplies the averaged voltage to the VCO input, and causes the VCO to oscillate at the center frequency (f_o). With phase-comparator I, the range of frequencies over which the PLL can acquire lock (capture range) is dependent on the low-pass-filter characteristics, and can be made as large as the lock range. Phase-comparator I enables a PLL system to remain in lock in spite of high amounts of noise in the input signal.

One characteristic of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the VCO center-frequency. A second characteristic is that the phase angle between the signal and the comparator input varies between 0° and 180°, and is 90° at the center frequency. Fig. 4 shows the typical, triangular, phase-to-output, response characteristic of phase-comparator I. Typical waveforms for a COS/MOS phase-locked-loop employing phase-comparator I in locked condition of f_o is shown in Fig. 5.

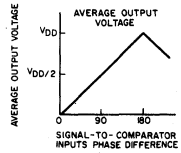


Fig. 4— Phase-comparator I characteristics at low-pass filter output.

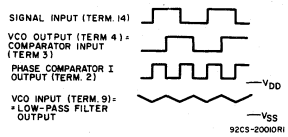


Fig. 5— Typical waveforms for COS/MOS phase-locked loop employing phase-comparator I in locked condition of f_o.

Phase-comparator II is an edge-controlled digital memory network. It consists of four flip-flop stages, control gating, and a three-state output circuit comprising p and n drivers having a common output node as shown in Fig. 3. When the p-MOS or n-MOS drivers are ON, they pull the output up to V_{DD} or down to V_{SS}, respectively. This type of phase comparator acts only on the positive edges of the signal- and comparator-input signals. The duty cycles of the signal and comparator inputs are not important since positive transitions control the PLL system utilizing this type of comparator. If the signal-input frequency is higher than the comparator-input frequency, the p-MOS output driver is maintained ON continuously. If the signal-input frequency is lower than the comparator-input frequency, the n-MOS output driver is maintained ON continuously. If the signal- and comparator-input frequencies are the same, but the signal input lags the comparator input in phase, the n-MOS output driver is maintained ON for a time corresponding to the phase difference. If the signal- and comparator-input frequencies are the same, but the signal input leads the comparator input in phase, the p-MOS output driver is maintained ON for time corresponding to the phase difference. Subsequently, the capacitor voltage of the low-pass filter connected to this type of phase comparator is adjusted until the signal and comparator input are equal in both phase and frequency. At this stable operating point, both p- and n-MOS output drivers remain OFF, and thus the phase-comparator output becomes an open circuit and holds the voltage on the capacitor of the low-pass filter constant. Moreover, the signal at the "phase pulses" output is at a high level, and can be used for indicating a locked condition. Thus, for phase-comparator II, no phase difference exists between signal and comparator input over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both the p- and n-MOS output drivers are OFF for most of the signal-input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase-comparator II. Fig. 6 shows typical waveforms for a COS/MOS PLL employing phase-comparator II in a locked condition.

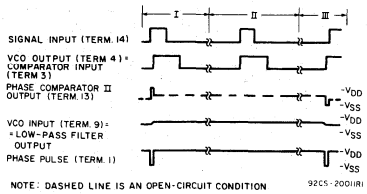


Fig. 6 – Typical waveforms for COS/MOS phase-locked loop employing phase-comparator II in locked condition.

Fig. 7 shows the state diagram for phase-comparator II; each circle represents a state of the comparator. The number at the top inside each circle represents the state of the comparator, while the logic state of the signal and comparator inputs, represented by a 0 or a 1, are given by the left and right numbers, respectively, at the bottom of each circle. The transitions from one state to another result from either a logic change on the signal input (I) or the comparator input (C). A positive transition and a negative transition are shown by an arrow pointing up or down, respectively. The state diagram assumes that only one transition on either the signal input or the comparator input occurs at any instant. States 3, 5, 9, and 11 represent the condition at the output of phase-comparator II when the p-MOS driver is ON, while states 2, 4, 10, and 12 determine the condition when the n-MOS driver is ON. States 1, 6, 7, and 8 represent the condition when the output of phase-comparator II is in its high impedance state; i.e., both p- and n-devices are OFF, and the phase-pulses output (terminal 1) is high. The condition at the phase-pulses output for all other states is low.

As an example of how one may use the state diagram shown in Fig. 7, consider the operation of phase-comparator II in the locked condition shown in Fig. 6. The waveforms shown in Fig. 6 are broken up into three sections: section I corresponds to the condition in which the signal input leads the comparator input in phase, while section II corresponds to a finite phase difference. Section III depicts the condition when the comparator input leads the signal input in phase. These three sections all correspond to a locked condition for the COS/MOS PLL; i.e., both signal- and comparator-input signals are of the same frequency but differ slightly in phase. Assume that both the signal inputs begin in the 0 state, and that phase-comparator II is initially in its high-impedance output condition (state 1), as shown in Figs. 7 and 6, respectively. The signal input makes a positive transition

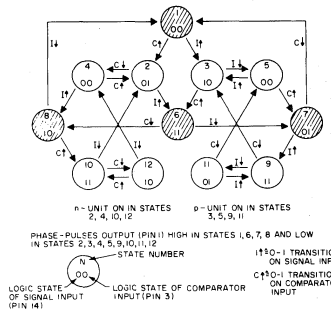


Fig. 7– State diagram of phase-comparator II.

first, which brings phase-comparator II to state 3. State 3 corresponds to the condition of the comparator in which the signal input is a 1, the comparator input is a 0, and the output p-device is ON. The comparator input goes high next, while the signal input is high, thus bringing the comparator to state 6, a high-impedance output condition. The signal input goes to zero next, while the comparator input is high, which corresponds to state 7. The comparator input goes low next, bringing phase-comparator II back to state 1. As shown for section I, the p-device stays on for a time corresponding to the phase difference between the signal input and the comparator input. Starting in state 1 at the beginning of section III, the comparator input goes high first, while the signal input is low, bringing the comparator to state 2. Following the example given for section I, the comparator proceeds from state 2 to states 6 and 8 and then back to 1. The output of phase-comparator II for section III corresponds to the n-device being on for a time corresponding to the phase difference between the signal and comparator inputs.

The state diagram of phase-comparator II completely describes all modes of operation of the comparator for any input condition in a phase-locked-loop.

Voltage-Controlled Oscillator

Fig. 8 shows the schematic diagram of the voltage-controlled oscillator (VCO). To assure low system-power dissipation, it is desirable that the low-pass filter consume little power. For example, in an RC filter, this requirement dictates that a high-value R and a low-value C be utilized. The VCO input must not, however, load down or modify the characteristics of the low-pass filter. Since the VCO design shown utilizes an n-MOS input configuration having practically infinite input resistance, a great degree of freedom is allowed in selection of the low-pass filter components.

The VCO circuit shown in Fig. 8 operates as follows: when the inhibit input is low, P_3 is turned full ON, effectively connecting the sources of P_1 and P_2 to V_{DD}; and gates 1 and 2 are permitted to function as NOR-gate flip-flops. N1 together with external-resistor R1 form a source-follower configuration. As long as the resistance of R1 is at least an order of magnitude greater than ON resistance of N_1 (greater than 10 kilohms), the current through R1 is linearly dependent on the VCO input voltage. This current flows through P_1, which, together with P2, forms a current-mirror network. External resistor R2 adds an additional constant current through P1; this current offsets the VCO operating frequency for VCO input signals of 0 volts. In the current-mirror network, the current of P2 is effectively equal to the current through P1 independent of the drain voltage at P2. (This condition is true provided P2 is maintained in saturation; in the circuit shown, P_2 is saturated under all possible operating conditions and modes). The set/reset flip-flop composed of gates 1 and 2 turns ON either P4 and N3, or P5 and N2. One side of the external capacitor C1 is, therefore, held at ground, while the other side is charged by the constant current supplied by P2. As soon as C1 charges to the point at which the transfer point of inverters 1 or 5 is reached, the flip-flop changes state. The

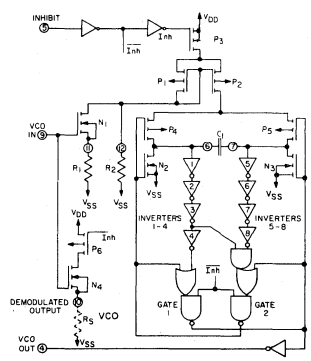


Fig. 8– Schematic of COS/MOS VCO section.

charged side of the capacitor is now pulled to ground. The other side of the capacitor goes negative, and discharges rapidly through the drain diode of the OFF n-device. Subsequently, a new half-cycle starts. Since inverters 1 and 5 have the same transfer points, the VCO has a 50-percent duty-cycle. Inverters 1 through 4 and 5 through 8 serve several purposes: (1) they shape the slow-input ramp from capacitor C1 to a fast waveform at the flip-flop input stage, (2) they maintain low power dissipation through the use of high-impedance devices at inverters 1 and 5 (slow-input wave-forms), and (3) they provide four inverter delays before removal of the set/reset flip-flop triggering pulse to assure proper toggling action.

In order not to load the low-pass filter, a source-follower ouput of the VCO input voltage is provided (demodulated output). If this output is used, a load resistor (Rs) of 10 kilohms or more should be connected from this terminal to ground. If unused, this terminal should be left open. A logic 0 on the inhibit input enables the VCO and the source follower, while a logic 1 turns off both to minimize stand-by power consumption.

Performance Summary of COS/MOS PLL

The maximum ratings for the CD4046A COS/MOS PLL, as well as its general operating-performance characteristics are outlined in Table I. The VCO and comparator characteristics are shown in Tables II and III, respectively. Table IV summarizes some useful formulas as a guide for approximating the values of external components for the CD4046A in a phase-locked-loop system. When using Table IV, one should keep in mind that frequency values are in kilohertz, resistance values are in kilohms, and capacitance values are in microfarads. The selected external components must be within the following ranges:

$$10\ K\Omega \leqslant R_1, R_2, R_s \leqslant 1\ M\Omega$$
$$C_1 \geqslant 100\ pF \text{ at } V_{DD} \geqslant 5\ V$$
$$C_1 \geqslant 50\ pF \text{ at } V_{DD} \geqslant 10\ V$$

In addition to the given design information, refer to Fig. 9 for R_1, R_2, and C_1 component selections. The use of Table IV in designing a COS/MOS PLL system for some familiar applications is discussed below.

APPLICATIONS OF THE COS/MOS PLL

The COS/MOS phase-locked-loop is a versatile building block suitable for a wide variety of applications, such as FM demodulators, frequency synthesizers, split-phase data synchronization and decoding, and phase-locked-loop lock detection.

FM Demodulation

When a phase-locked-loop is locked on an FM signal, the voltage-controlled oscillator (VCO) tracks the instantaneous frequency of that signal. The VCO input voltage, which is the filtered error voltage from the phase detector, corresponds to the demodulated output. Fig. 11 shows the connections for the COS/MOS CD4046A PLL as an FM demodulator. For this example, an FM signal consisting of a 10-kilohertz carrier frequency was modulated by a 400-Hz audio signal. The total FM signal amplitude is 500 millivolts, therefore the signal must be ac coupled to the signal input (terminal 14).

Table I– Maximum ratings and general operating characteristics

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage Temperature Range	−65°C to +150	°C
Operating Temperature Range:		
Ceramic Package Types	−55°C to +125	°C
Plastic Package Types	−40°C to +85	°C
DC Supply Voltage Range ($V_{DD} - V_{SS}$)	−0.5 V to +15	V
Device Dissipation (Per Pkg.)	200	mW
All Inputs	$V_{SS} \leqslant V_I \leqslant V_{DD}$	
Recommended DC Supply Voltage ($V_{DD} - V_{SS}$)	5 to 15	V
Recommended Input Voltage Swing	V_{DD} to V_{SS}	

General Characteristics (Typical Values at $V_{DD} - V_{SS}$ = 10 V and T_A = 25°C)

Operating Supply Voltage ($V_{DD} - V_{SS}$)	5 to 15	V
Operating Supply Current		
Inhibit = "0" @ C_1 = 0.0001 μF R_1 = 1 MΩ	f_0 = 10 kHz, V_{DD} = 5 V	70 μW
	f_0 = 10 kHz, V_{DD} = 10 V	600 μW
Inhibit = "1"		25 μA

Table II– VCO electrical characteristics

VCO Characteristics (Typical Values at $V_{DD} - V_{SS}$ = 10 V and T_A = 25°C)

Maximum Frequency	1.2 MHz
Temperature Stability	600 ppm/°C
Linearity ($V_{VCO\ in}$ = 5 V ± 2.5 V)	1%
Center Frequency	Programmable with R_1 and C_1
Frequency Range	Programmable with R_1, R_2, and C_1
Input Resistance	$10^{12}\ \Omega$
Output Voltage	10 V_{p-p}
Duty Cycle	50%
Rise & Fall Times	50 ns
Output Current Capability	
"1" Drive @ V_O = 9.5 V	−1.8 mA
"0" Sink @ V_O = 0.5 V	2.6 mA
Demodulated Output:	
Offset Voltage ($V_{VCO\ in} - V_{DEMOD\ out}$) @ 1 mA	1.5 V

Table III – Comparator electrical characteristics

Comparator Characteristics (Typical Values at $V_{DD} - V_{SS}$ = 10 V and T_A = 25°C)

Signal Input:	
Input Impedance	400 KΩ
Input Sensitivity:	
ac coupled	400 mV
dc coupled	"0" ≤ 30% ($V_{DD} - V_{SS}$) "1" ≥ 70% ($V_{DD} - V_{SS}$)
Comparator Input Levels (term. 3)	"0" ≤ 30% ($V_{DD} - V_{SS}$) "1" ≥ 70% ($V_{DD} - V_{SS}$)
Output Current Capability	
Comparator I (term. 2) and Comparator II (term. 13):	
"1" Drive @ V_O = 9.5 V	−1.8 mA
"0" Sink @ V_O = 0.5 V	2.6 mA
Comparator II Phase Pulses (term. 1):	
"1" Drive @ V_O = 9.5 V	−0.5 mA
"0" Sink @ V_O = 0.5 V	1.4 mA

Phase-comparator I is used for this application because a PLL system with a center frequency equal to the FM carrier frequency is needed. Phase comparator I lends itself to this application also because of its high signal-input-noise-rejection characteristics.

The formulas shown in Table IV for phase-comparator I with $R_2 = \infty$ are used in the following considerations. The center frequency of the VCO is designed to be equal to the carrier frequency, 10 kHz. The value of capacitor C_1, 500 pF, was found by assuming an R_1 = 100 KΩ for a supply voltage V_{DD} = 5 volts.

These values determined the center frequency:

$$f_0 = 10\ \text{kHz}$$

The PLL was set for a capture-range of

$$f_c \approx \pm\frac{1}{2\pi}\ \frac{2\pi f1}{R_3C_2} = \pm 0.4\ \text{kHz}$$

to allow for the deviation of the carrier frequency due to the audio signal. The components shown in Fig. 10 for the low-pass filter (R_3 = 100 kΩ, C_2 = 0.1 μF) determine the above capture frequency.

The total current drain at a supply voltage of 5 volts for this FM-demodulator application is 132 microamperes for a 4 dB S/N-ratio on the signal input, and 90 microamperes for a 10dB S/N ratio. The power consumption decreases because the signal-input amplifier goes into saturation at higher input levels.

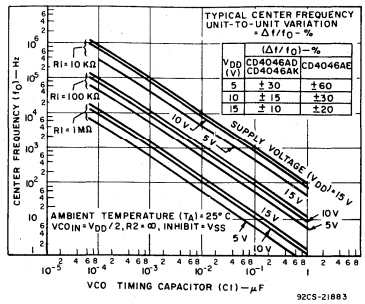


Fig. 9(a)– Typical center frequency vs. C_1 for R_1 = 10 KΩ, 100 KΩ, and 1 MΩ.

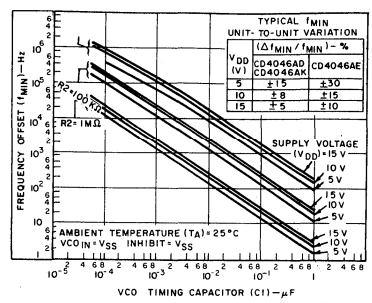


Fig. 9(b)– Typical frequency offset vs. C_1 for R_2 = 10 KΩ, 100 KΩ, and 1 MΩ.

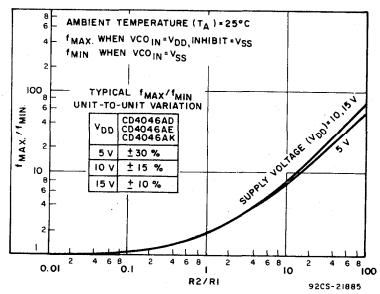
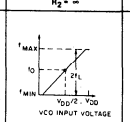
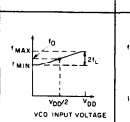
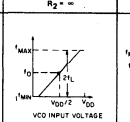
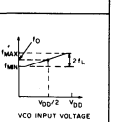
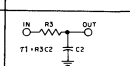
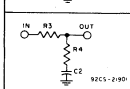


Fig. 9(c)– Typical f_{max}/f_{min} vs. R_2/R_1.

CHARACTERISTICS	USING PHASE COMPARATOR I		USING PHASE COMPARATOR II	
	VCO WITHOUT OFFSET $R_2 = \infty$	VCO WITH OFFSET	VCO WITHOUT OFFSET $R_2 = \infty$	VCO WITH OFFSET
VCO Frequency				
For No Signal Input	VCO in PLL system will adjust to center frequency, f_0		VCO in PLL system will adjust to lowest operating frequency, f_{min}	
Frequency Lock Range, $2f_L$	$2f_L$ = full VCO frequency range $2f_L = f_{max} - f_{min}$			
Frequency Capture Range, $2f_C$	 (1),(2) $2f_C \approx \frac{1}{\pi}\sqrt{\frac{2\pi f_L}{f1}}$		$f_C = f_L$	
Loop Filter Component Selection	 For $2f_C$, see Ref. (2)			
Phase Angle between Signal and Comparator	90° at center frequency (f_0), approximating 0° and 180° at ends of lock range ($2f_L$)		Always 0° in lock	
Locks on Harmonics of Center Frequency	Yes		No	
Signal Input Noise Rejection	High		Low	
VCO Component Selection	– Given: f_0 – Use f_0 with Fig.9a to determine R1 and C1	– Given: f_0 and f_L – Calculate f_{min} from the equation $f_{min} = f_0 - f_L$ – Use f_{min} with Fig.9b to determine R2 and C1 – Calculate $\frac{f_{max}}{f_{min}}$ from the equation $\frac{f_{max}}{f_{min}} = \frac{f_0 + f_L}{f_{min} - f_L}$ – Use $\frac{f_{max}}{f_{min}}$ with Fig.5c to determine ratio R2/R1 to obtain R1	– Given: f_{max} – Calculate f_0 from the equation $f_0 = \frac{f_{max}}{2}$ – Use f_0 with Fig.9a to determine R1 and C1	– Given: f_{min} & f_{max} – Use f_{min} with Fig.5b to determine R2 and C1 – Calculate $\frac{f_{max}}{f_{min}}$ – Use $\frac{f_{max}}{f_{min}}$ with Fig.9c to determine ratio R2/R1 to obtain R1

For further information, see
(1) F. Gardner, "Phase-Lock Techniques" John Wiley and Sons, New York, 1966
(2) G. S. Moschytz, "Miniaturized RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.

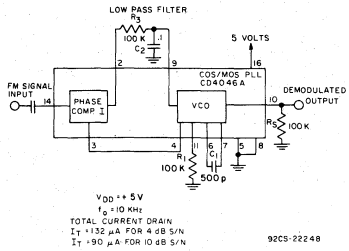


Fig. 10– FM demodulator.

Fig. 11 shows the performance of the FM/demodulator circuit of Fig. 10 at a 4 dB S/N-ratio. The demodulated output is taken off the VCO-input source follower using a resistor Rs (R_S = 100 kΩ).The demodulation gain for this circuit is 250 mV/kHz.

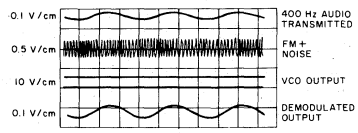


Fig. 11– Voltage waveforms of FM demodulator.

Frequency Synthesizer

The PLL system can function as a frequency-selective frequency multiplier by inserting a frequency divider into the feedback loop between the VCO output and the comparator input. Fig. 12 shows a COS/MOS low-frequency synthesizer with a programmable divider consisting of three decades. N, the frequency-divider modulus, can vary from 3 to 999 in steps of 1. When the PLL system is in lock, the signal and comparator inputs are at the same frequency and

$$f = N \times 1\ kHz$$

Therefore, the frequency range of this synthesizer is 3 to 999 kHz in 1-kHz increments, which is programmable by the switch position of the Divide-by-N counter.

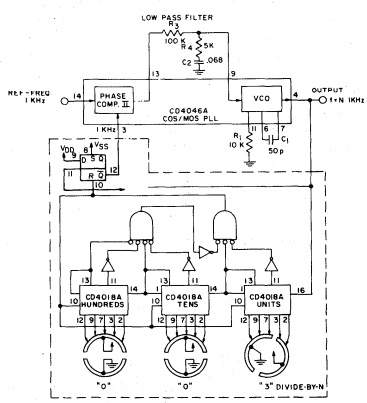


Fig. 12– Low-frequency synthesizer with three-decade programmable divider.

Phase-comparator II is used for this application because it will not lock on harmonics of the signal-input reference frequency (phase-comparator I does lock on harmonics). Since the duty cycle of the output of the Divide-by-N frequency divider is not 50 percent, phase-comparator II lends itself directly to this application.

Using the formulas for phase-comparator II shown in Table IV, the VCO is set up to cover a range of 0 to 1.1 MHz. The low-pass filter for this application is a two-pole, lag-lead filter which enables faster locking for step changes in frequency. Fig. 13 shows the waveforms during switching between output frequencies of 3 and 903 kHz. The figure shows that the transient going towards 3 kHz on the VCO control voltage is overdamped, while the transient to 903 kHz is underdamped. This condition could be improved by changing the value of R_3 in the low-pass filter by means of adjustment of the switch-position hundreds in the Divide-by-N counter.

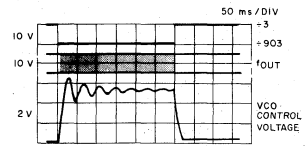


Fig. 13– Frequency-synthesizer waveforms.

Split-Phase Data Synchronization and Decoding

Fig.14 shows another application of COS/MOS PLL, split-phase data synchronization and decoding. A split-phase data signal consists of a series of binary digits that occur at a periodic rate, as shown in waveform A in Fig. 14, The weight of each bit, 0 or 1, is random, but the duration of each bit, and therefore the periodic bit-rate, is essentially constant. To detect and process the incoming signal, it is necessary to have a clock that is synchronous with the data-bit rate. This clock signal must be derived from the incoming data signal. Phase-lock techniques can be utilized to recover the clock and the data. Timing information is contained in the data transitions, which can be positive or negative in direction, but both polarities have the same meaning for timing recovery. The phase of the signal determines the binary bit weight. A binary 0 or 1 is a positive or negative transition, respectively, during a bit interval in split-phase data signals.

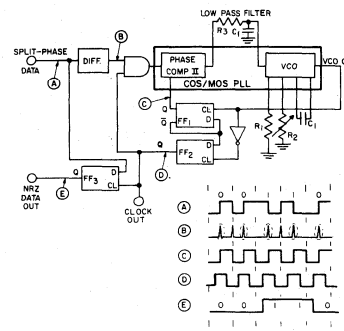


Fig. 14– Split-phase data synchronization and decoding.

As shown in Fig. 14, the split-phase data-input (A) is first differentiated to mark the locations of the data transitions. The differentiated signal, (B), which is twice the bit rate, is gated into the COS/MOS PLL. Phase-comparator II in the PLL is used because of its insensitivity to duty cycle on both the signal and comparator inputs. The VCO output is fed into the clock input of FF1 which divides the VCO frequency by two. During the ON intervals, the PLL tracks the differentiated signal (B); during the OFF intervals the PLL remembers the last frequency present and still provides a clock output. The VCO output is inverted and fed into the clock input of FF2 whose data input is the inverted output of FF1. FF2 provides the necessary phase shift in signal (C) to obtain signal (D), the recovered clock signal from the split-phase data transmission. The output of FF3, (E), is the recovered binary information from the phase information contained in the split-phase data. Initial synchronization of this PLL system is accomplished by a string of alternating 0's and 1's that precede the data transmission.

Phase-Locked-Loop Lock Detection

In some applications that utilize a PLL, it is sometimes necessary to have an output indication of when the PLL is in lock. One of the **simplest forms** of lock-condition indicator is a binary signal. For example, a 1 or a 0 output from a lock-detection circuit would correspond to a locked or unlocked condition, respectively. This signal could, in turn, activate circuitry utilizing a locked PLL signal. This detection could also be used in frequency-shift-keyed (FSK) data transmissions in which digital information is transmitted by switching the input frequency between either of two discrete input frequencies, one corresponding to a digital 1 and the other to a digital 0.

Fig. 15 shows a lock-detection scheme for the COS/MOS PLL. The signal input is switched between two discrete frequencies of 20 kHz and 10 kHz. The PLL system uses

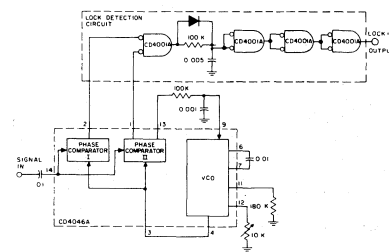


Fig. 15– Lock-detection circuit.

phase-comparator II; the VCO bandwidth is set up for an f_{min} of 9.5 kHz and an f_{max} of 10.5 kHz. Therefore, the PLL locks and unlocks on the 10-kHz and 20-kHz signals, respectively. When the PLL is in lock, the output of phase-comparator I is low except for some very short pulses that result from the inherent phase difference between the signal and comparator inputs; the phase-pulses output (terminal 1) is high except for some very small pulses resulting from the same phase difference. This low condition of phase comparator I is detected by the lock-detection circuit shown in Fig. 15. Fig. 16 shows the performance of this circuit when the input signal is switched between 20 and 10 kHz. It can be seen that after about five input cycles the lock detection signal goes high.

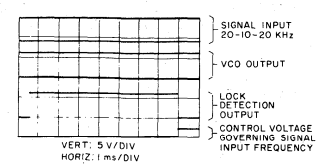


Fig. 16– Lock-detection-circuit waveforms.

Using the CD4047A in COS/MOS Timing Applications

by J. Paradise

Many applications exist today for COS/MOS multivibrators– both oscillators and one-shots–in analog and digital circuits. The requirements for these applications vary widely in such parameters as voltage range, temperature stability, power dissipation, drive capability, and external-component cost. No design is optimum for all of the above considerations. However, the RCA-CD4047A Monostable/Astable Multivibrator fulfills the needs of most applications in this timing area. It can function as either an oscillator or one-shot with many additional features, and will meet the power dissipation, stability, and speed requirements of most COS/MOS systems.

This Note compares some simpler types of oscillator circuits with the CD4047A in both theoretical and actual performance, and provides application information on the CD4047A which should prove useful to COS/MOS circuit and system designers.

COS/MOS DISCRETE RC OSCILLATOR

The simplest type of RC-oscillator is shown in Fig. 1. It consists of two inverters (which may be taken from standard

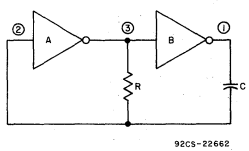


Fig. 1 – Simplest COS/MOS RC oscillator.

RCA COS/MOS parts, i.e., CD4007A, CD4001A, CD4011A, etc.) and a single resistor and capacitor. The operating waveforms for this circuit are shown in Fig. 2.

The circuit operates as follows: depending on the output levels of inverters A and B, at any instant C will be charging or discharging through R. When the waveform at point (2) in the circuit passes through the transfer voltage of inverter A, this inverter will switch and cause inverter B to switch. Subsequently, the waveform at point (2) would be exponentially

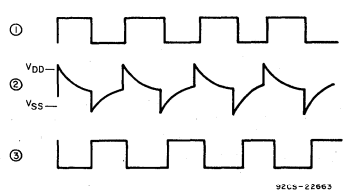


Fig. 2 – RC-oscillator operating waveforms.

increasing or decreasing with discontinuities equal in magnitude to V_{DD} during the instant of switching. However, since point (2) is protected by a standard input-protection circuit common to COS/MOS devices, the waveform is clamped at one diode voltage drop above V_{DD} and below V_{SS}. (Refer to waveforms in Figs. 2 and A1). The calculations for the period of this multivibrator circuit are shown in Appendix A; the final equation for the period T is

$$T = -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_D)^2} \qquad (1)$$

where V_{TR} is the switching or transfer point of the inverter, and V_D is the diode forward voltage drop.

Equation (1) shows that the period of the multivibrator, T, is sensitive to changes in V_{DD}, as illustrated by the graph of time period, T, vs transfer voltage as a function of V_{DD} in Fig. 3. In addition to the strong dependence of actual time period on the V_{DD} chosen, the graph also illustrates that, for a given V_{DD}, a full transfer voltage spread of 30 to 70 per cent of V_{DD} (unit-to-unit worst-case variations) yields a change in time period of about 10 per cent from the nominal 50-per-cent transfer-voltage percentage values.

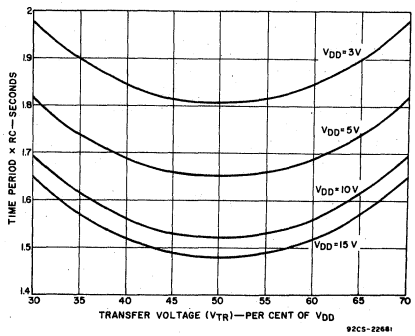


Fig. 3 – Discrete RC-oscillator time period as a function of transfer voltage.

The above analysis is valid only at low frequencies (i.e., less than 50 kHz). As the multivibrator frequency approaches this value, other considerations must be taken into account:

1. The input protection circuit has a V_{DD} diode with a finite resistance and capacitance; the diode will discharge at the rate associated with this small time constant.
2. In the negative direction, there is a diode as well as a series protection resistor (1 to 3 kilohms); the time constant of this diode is even longer than that of the V_{DD} diode.
3. The propagation delay of the inverters used is added to the time period during each charge and discharge cycle. Since the delay is a function of V_{DD}, small changes in V_{DD} at high frequencies will cause the time period to vary.
4. There is a finite output impedance associated with the inverter which is in series with the external timing resistor. Since this output impedance also changes with V_{DD}, at high frequencies where the external resistor becomes small, the multivibrator stability decreases with small variations in V_{DD}.

The negative features of the input protection circuit can be partially compensated for by the addition of a resistor, R_S, in series with the input protection circuit, as shown in Fig. 4. Although the input inverter A is still clamped at one diode drop above V_{DD} or one diode drop below V_{SS}, the waveform at point (4) is allowed to swing well above V_{DD} and below V_{SS}. The larger swing reduces the dependency of transfer-voltage variations upon stability; the variable characteristics of the input protection circuit and their effect upon stability are greatly reduced. An analysis of this circuit is presented in

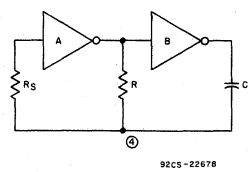


Fig. 4 – RC-oscillator with the addition of R_S

Appendix B; the equation for the period, T, for this circuit is shown in Eq. 2.

When $K = \frac{R_s}{R}$, T is:

$$\left\{ \begin{array}{l} T = -RC \ln \dfrac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_D)^2} \\ \\ -\dfrac{(K\ \ )}{(K+1)} RC \ln \dfrac{K\,[V_{DD} + V_D]}{K\,[V_{DD} + V_{TR}] + [V_{TR} - V_D]} \\ \\ -\dfrac{(K\ \ )}{(K+1)} RC \ln \dfrac{K\,[V_{DD} + V_D]}{K\,[2\,V_{DD} - V_{TR}] + [V_{DD} - V_{TR} - V_D]} \end{array} \right\} \qquad (2)$$

In this form it is easy to see that when K approaches zero, the circuit and associated waveforms are equivalent to those of Fig. A-1. On the other hand, as K approaches infinity, the variation in period as a function of V_{DD} is reduced to zero. This result is shown in Fig. 5, where period as a function of transfer voltage is plotted for different value of V_{DD} and K, and Fig. 6, which shows period as a function of K for different values of V_{DD}. Variation in period with transfer voltage is also reduced as K increases. This variation decreases from 10 per cent for K = 0 to about 5 per cent as K gets large.

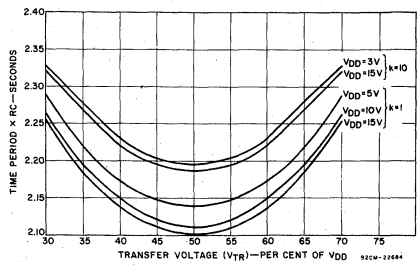


Fig. 5 – Discrete RC-oscillator time period as a function of transfer voltage.

There are some obvious limitations in the value of R_S that can be used. Besides the disadvantages in this circuit if R is to

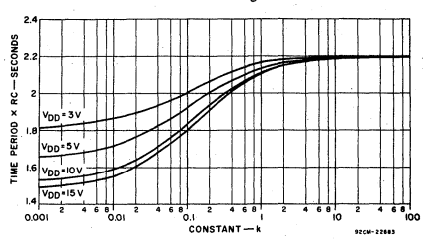


Fig. 6 – Discrete RC-oscillator time period as a function of constant, k.

be made adjustable, the user must be careful with component layout, if R_S is made very large, to take advantage of the improvement in stability. A time constant and phase shift is produced by R_S and stray wiring and breadboard capacitance, see Fig. 7. This shift creates a switching delay in the circuit which changes the time period and, in addition, may cause spurious oscillations and glitches in the multivibrator circuit. A reasonable value for K would be anywhere from 2 to 10, with maximum and minimum values for R_S determined by the above considerations.

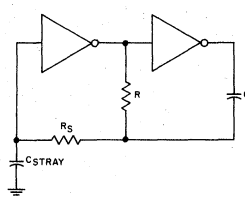


Fig. 7 – RC-oscillator circuit with stray capacitance.

COS/MOS INTEGRATED RC OSCILLATORS

The RCA-CD4047A is an integrated RC oscillator that eliminates most of the disadvantages of the discrete circuits previously discussed. The primary reason for this improved performance is the special input-protection circuit which allows the capacitor charging waveform to swing above V_{DD} and below V_{SS} without the need for an external resistor. This circuit, shown in Fig. 8, has the same time period and stability as the circuit in Fig. 4 for the case where the value of R_S is infinite. However, a resistor is eliminated, as well as the disadvantages of a time constant caused by the resistor.

There are two additional reasons for expected improvement with the CD4047A. First, the transfer-voltage point of the input inverter, A, is tested between 33 and 67 per cent of V_{DD} instead of between 30 and 70 per cent; this narrower test range improves stability by reducing unit-to-unit variations. In addition, large buffers are used for inverters D and E; this practice

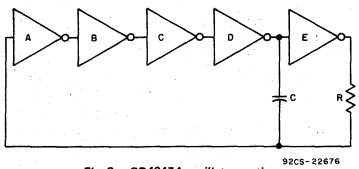


Fig. 8 – CD4047A oscillator section

reduces the effect of changes of device output impedance with period stability. A derivation of period, T, for this circuit is presented in the Appendix C; the final equation for T becomes:

$$T = -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_{TR})(2V_{DD} - V_{TR})} \quad (3)$$

Figure 9 shows a graph of stability as a function of transfer voltage based on this equation.

The graph of Fig. 9 shows a maximum variation of 5 per cent between minimum (2.197 RC) and maximum (2.307 RC) time periods. A value of 2.25 RC yields a ± 2.5 per-cent variation. Typical values of period variations at high frequencies and temperature extremes are included in the published data for the CD4047A.[1]

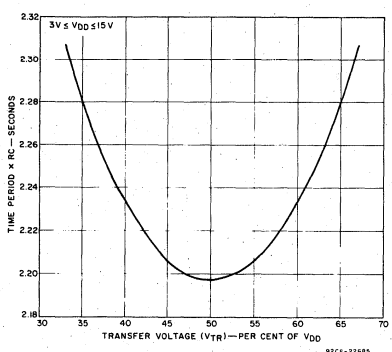


Fig. 9 – CD4047 time period as a function of transfer voltage.

An additional advantage of the CD4047A is a reduction in power dissipation as compared to the discrete multivibrators discussed previously. Inverter A in Fig. 8 is designed with high-impedance components that limit power dissipation during the time that the inverter operates in the middle of its transfer region. Four additional inverters are used to gradually shift from a very-high-impedance inverter at the input to a very-low-impedance driver in series with the external timing resistor. Calculations for power dissipation and a comparison of P_{diss} for the CD4047A and a discrete oscillator are presented in Appendix D; the result is

$$P_{diss} = 2CV^2 f \quad (4)$$

This equation specifies the power dissipated in the external components only. At low frequencies, where most of the power will be dissipated in R, power can be minimized by using a small value of C, since the formula shows the power is a function of C and not R.

Additional power is consumed in the CD4047A chip as a function of frequency. Fig. 10 shows curves for theoretical minimum power dissipation, actual CD4047A oscillator-power dissipation, and discrete oscillator-power dissipation as a function of frequency.

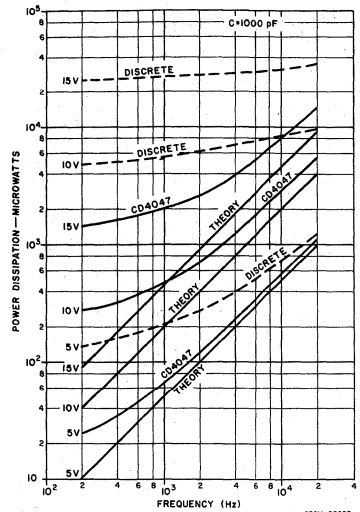


Fig. 10 – Comparison of P_{diss} for discrete oscillator and CD4047 with theory.

CMOS DISCRETE ONE-SHOTS

Fig. 11 illustrates one of several simple monostable circuits which can be employed in non-critical timing circuits.[2] The

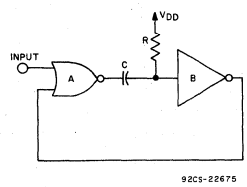


Fig. 11 – COS/MOS monostable circuit.

circuit pulse width is dependent upon the transfer voltage of inverter B as time constant RC charges to V_{DD} from V_{SS}. The pulse width is defined as

$$T = -RC \ln \frac{(V_{DD} - V_{TR})}{(V_{DD})} \quad (5)$$

Fig. 12 shows the variation in pulse width as a function of transfer voltage for this device.

There are several alternatives to the circuit shown in Fig. 12.[2] These alternatives have the advantage of greater stability, but at the expense of two time constants required in circuit and, in some cases, the addition of a diode.

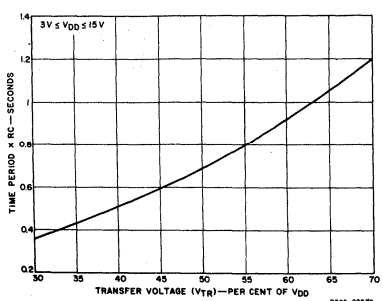


Fig. 12 – Simple one-shot time period as a function of transfer voltage.

COS/MOS INTEGRATED ONE-SHOTS

The CD4047A, when used in the monostable mode, again has several advantages over discrete designs. A high degree of accuracy can be achieved with one time constant, and power dissipation is lower than with discrete designs. Fig. 13 shows that many functions can be achieved with the CD4047A, including leading and trailing-edge triggering, and retriggering.

The pulse width, T_M, is expressed below: its derivation is given in Appendix E.

$$T_M = -RC \ln \frac{(V_{TR})(V_{DD}) - V_{TR})}{(2V_{DD})(2V_{DD} - V_{TR})} \quad (6)$$

Fig. 14 is a graph of pulse width versus transfer voltage based on the above equation.

The equations for monostable-mode power dissipation are also derived in Appendix E. For a repetitive output on the CD4047A, power dissipation can be expressed by the following equation:

$$P_{diss} = \frac{2.875\, CV_{DD}^2}{T_M} \times (\text{duty cycle}) \quad (7)$$

USING THE CD4047A – SPECIAL CONSIDERATIONS

A number of circuit considerations are explained below which will aid the user of the CD4047A.

A clamping circuit is provided on the chip to reduce the recovery time (tr) that would normally exist in other monostable circuits; see Figs. 15 and 16. Fig. 17 shows a plot of monostable-pulse-width stability as a function of duty cycle for specific R and C external components. Note that there is no appreciable change in pulse width until the duty cycle approaches 100 per cent. A disadvantage to the clamping circuit is that it introduces additional capacitance at the RC common node (Fig. 16), which may be noticeable for short pulse widths in the monostable mode only. Some diffusion capacitance present at the base of the n-p-n transistor is used to quickly charge C to V_{DD} after the one-shot cycle has terminated. This capacitance is multiplied by the beta of the transistor, and is in parallel with the external C during the time interval that the transistor is on ($V_{DD} - V_{BE} < t < V_{BE}$). Thus, when values of C less than 1000 picofarads are used, the actual width will be longer than that predicted by the formula. Fig. 18 is a graph of actual, typical pulse widths as a function of external C used under these conditions. Note that the minimum values of C used in the graph are the smallest that can be used in the CD4047A to assure proper operation of the circuit.

The waveform in Fig. 15 shows that two positive transitions are encountered by the control circuitry in the CD4047A. These transitions are necessary to make the output flip-flop at pin 10 toggle properly to produce the single pulse needed in monostable operation. However, at pin 13, the waveform of Fig. 19 results; the pulse width of the spike is equivalent to the propagation delay of the circuit. This spike will normally prevent the user from using pin 13 in the monostable mode. In the astable mode, however, pin 13 can be used whenever a 50-per-cent duty cycle and higher drive capability are not required. The advantage to the use of pin 13 under these conditions is that the frequency of the waveform at pin 13 is twice that of pin 10 for the same external timing components.

When the CD4047A is used in the retrigger mode, the retrigger input is connected directly to the set input of FF4, as shown in Fig. 13. This connection means that the output at pin 10 will be high during the time that a high level is present on pin 12. Thus, if normal one-shot operation is required at any time that the circuit is in the retrigger mode, the input pulse should be shorter than the expected pulse at the output. Note that in the retrigger mode the output pulse width is not referenced to the last positive-going edge produced at the input because of the asynchronous nature of the circuit. The output actually terminates when two internal-oscillator leading edges have been received by FF4, after the high level present on pin 12 has been removed. The output width variation will then be between one and two time constants referenced to the trailing edge of the input at pin 12, see Fig. 20.

A section on timing-component limitations is presented in the CD4047A data sheet.[1] It should be emphasized that it is desirable to use a small value of capacitance wherever possible.

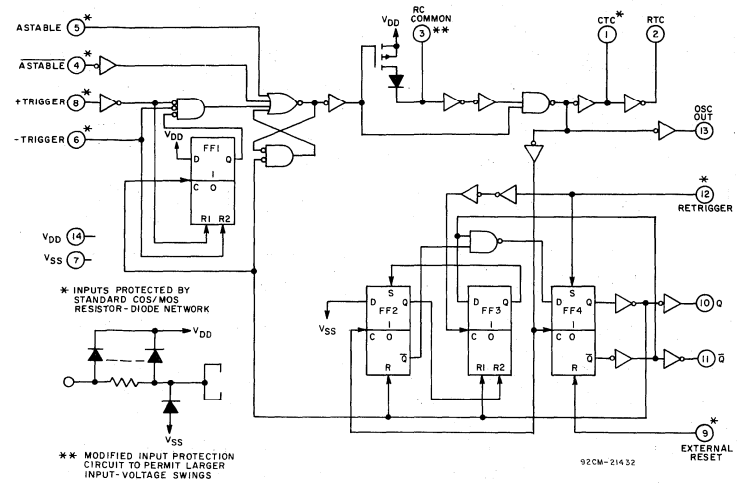


Fig. 13 – CD4047A logic diagram.

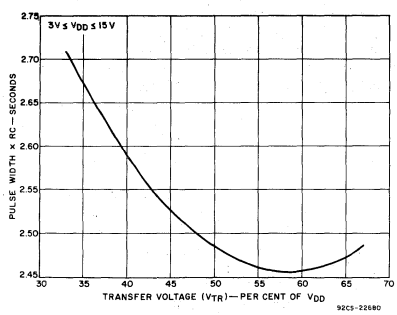


Fig. 14 – CD4047A one-shot pulse width as a function of transfer voltage.

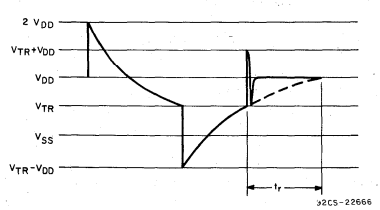


Fig. 15 – CD4047A one-shot RC waveform.

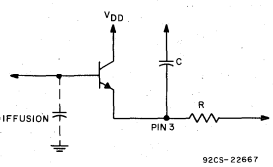


Fig. 16 – CD4047A clamping circuit.

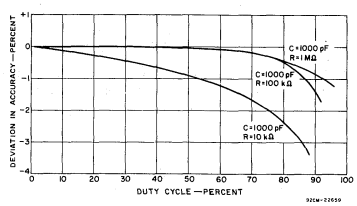


Fig. 17 – CD4047A monostable accuracy as a function of duty cycle.

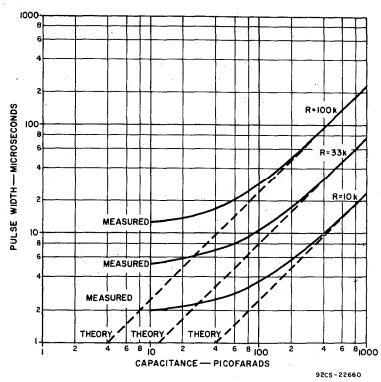


Fig. 18 – CD4047A pulse width as a function of capacitance.

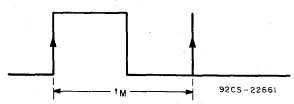


Fig. 19 – CD4047A one-shot output at pin 13.

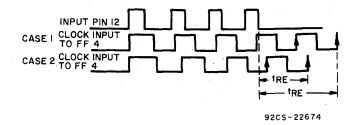


Fig. 20 – CD4047A retrigger-mode waveforms.

The circuit will work well even when the value of R approaches or exceeds 1 megohm. For very low frequencies, where a large value of capacitance is needed, the selection of the capacitor is very important. It must be nonpolarized because there is no reference ground at either of the two pins to which C is connected. The capacitor parallel resistance (i.e., leakage) must also be at least an order of magnitude higher than the external R used. This criterion generally eliminates electrolytic capacitors and those made of materials which could produce greater leakage current than that permitted for proper circuit operation.

Because of the internal circuit construction, there is no guarantee as to what dc level will be present on the output at pin 10 or 11 when power is first turned on. If this condition must be guaranteed, a system-power on pulse input to pin 9 can be made to assure that pin 10 will initially be at a low logic level. The pulse can be generated from one of the circuits shown in Fig. 21.

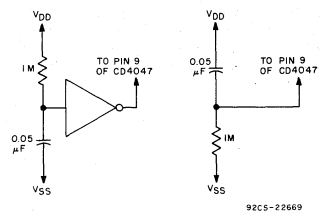


Fig. 21 – CD4047A power-up reset circuits.

Although the CD4047A data sheet calls for a minimum input pulse duration of 200 nanoseconds at 10 volts and 500 nanoseconds at 5 volts, shorter pulses (due to transients, etc.) occur frequently in system applications where the CD4047A is used. Such narrow pulses may not be ignored by the CD4047A, but may instead cause Q to go high permanently or until a reset input occurs. The circuit shown in Fig. 22 eliminates this problem by essentially "lengthening" the trigger pulse by feeding back through R_A and C_A a current pulse when Q goes from 0 to a 1. The particular values shown have been tried and found to work well, even for extremely short input pulses (less than 20 nanoseconds).

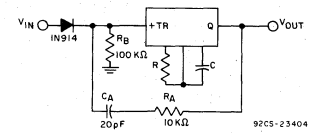


Fig. 22 – Input-pulse stretcher circuit.

APPLICATIONS

NOISE DISCRIMINATOR

Fig. 23 illustrates an application of the CD4047A in a noise-discriminator circuit. Py adjusting the external time constant, a pulse width narrower than that determined by the time constant will be rejected by the circuit. The output pulse will

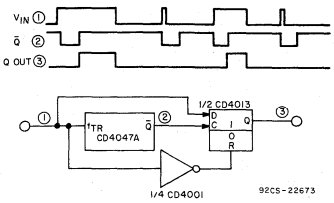


Fig. 23 – Noise-discriminator circuit.

follow the desired input, but the leading edge will be delayed by the selected time constant. Fig. 24 shows typical waveforms with the circuit in operation.

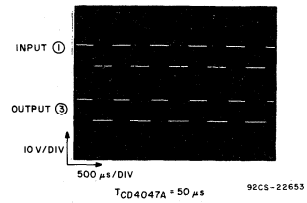


Fig. 24 – Noise-discriminator circuit waveforms.

FREQUENCY DISCRIMINATOR

The CD4047A can be used as a frequency-to-voltage converter, as shown in Fig. 25. A waveform of varying frequency is applied to the +TR input. The one-shot will produce a pulse of constant width for each positive transition on the input. The

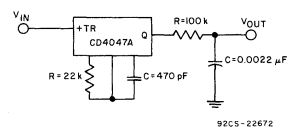


Fig. 25 – Frequency-discriminator circuit.

resultant pulse train is integrated to produce a waveform whose amplitude is proportional to the input frequency. The waveforms of Fig. 26 were taken with the circuit in operation.

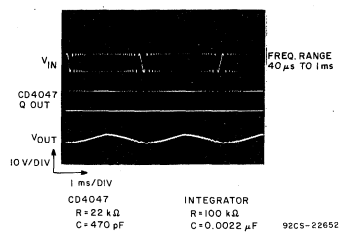


Fig. 26 – Frequency-discriminator-circuit waveforms.

LOW-PASS FILTER

A simple circuit using the CD4047A as a low-pass filter is shown in Fig. 27. The time constant chosen for the multivibrator will determine the upper cutoff frequency for the filter. The circuit essentially compares the input frequency

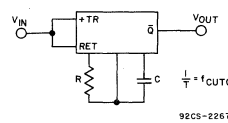


Fig. 27 – Low-pass filter circuit.

with its own reference, and produces an output which follows the input for frequencies less than f_{cutoff}, and a low output for frequencies greater than f_{cutoff}. Figs. 28 and 29 show waveforms with the low-pass filter circuit in operation.

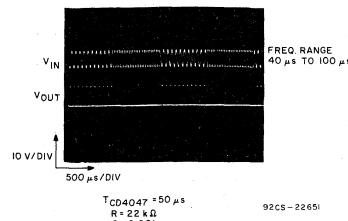


Fig. 28 – Low-pass filter-circuit waveforms.

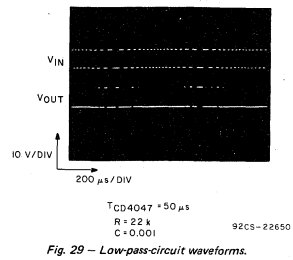


Fig. 29 – Low-pass-circuit waveforms.

BANDPASS FILTER

Two CD4047A low-pass filters can be employed to construct a bandpass filter, as illustrated by the circuit in Fig. 30. The pass band is determined by the time constants of the two filters. If the output of filter No. 2 is delayed by C_1, the CD4013A flip-flop will clock high only when the cutoff frequency of filter No. 2 has been exceeded; this point is illustrated in the timing diagram in Fig. 30. The $\overline{Q}$ output of the CD4013A is gated with the output of filter No. 1 to produce

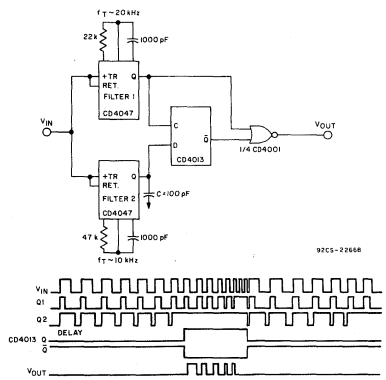


Fig. 30 – Bandpass filter circuit and waveforms.

the desired output. Typical operation of the circuit is shown in Fig. 31, where the input frequency is swept through the pass band.

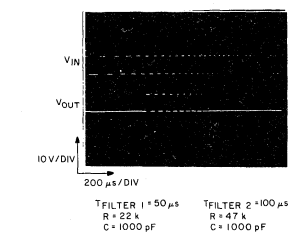


Fig. 31 – Bandpass-filter-circuit waveforms.

ENVELOPE DETECTOR

The CD4047A can be used as an envelope detector by employing it in the retrigger mode, as shown in Fig. 32. The time constant is selected so that the circuit will retrigger at the

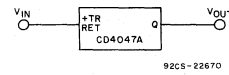


Fig. 32 – Envelope-detector circuit.

frequency of the input pulse burst. A dc level appears at the output for the duration of the input pulse train. Fig. 33 shows waveforms taken with the circuit in operation.

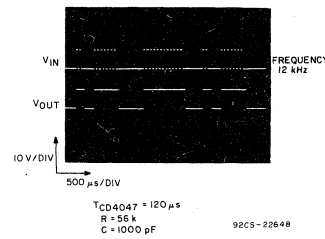


Fig. 33 – Envelope-detector-circuit waveforms.

PULSE GENERATOR

Several CD4047A units can be connected together to produce a general-purpose laboratory pulse generator, as shown in Fig. 34. The circuit shown has variable-frequency and pulse-width control, as well as gating and delayed sync capability. Gating can be controlled from a high- or low-level input. Automatic 50-per-cent duty-cycle capability is included, as normal or inverted output.

CD4047A No. 1 is connected as a gated, astable multivibrator, and, with the RC values shown, can produce overlapping ranges of frequencies from 2 Hz to 1 MHz. For free-running operation, the Gate/Free-Run switch is closed, and the Gate Level switch is placed in the **high-level** position. Standby operation can be achieved with the Gate Level switch in the **low-level** position. When gating, the Gate/Free-Run switch is open, and the Gate Level switch is set to the appropriate position. The gate signal is applied to the Gate In jack.

CD4047A No. 2 is triggered from the gated, astable multivibrator, and produces a narrow sync pulse which can trigger an oscilloscope or generator. The sync pulse is obtained from the Sync Out jack.

If a 50-per-cent duty cycle is desired, the Duty Cycle switch is set in the 50-per-cent position, and the output is obtained from CD4047A No. 1. The Signal Polarity switch determines whether the Q and $\overline{Q}$ output is used.

CD4047A No. 3 produces a variable, delayed (from 1.5 microseconds to 250 milliseconds) output with respect to the sync pulse when the Delay switch is in the IN position. This one-shot is bypassed when the Delay switch is in the OUT position (the inherent delay is approximately 400 nanoseconds).

CD4047A No. 4 is a monostable multivibrator which receives trigger pulses from CD4047A No. 1 or No. 3. It can produce overlapping ranges of pulse widths from 1.5 microseconds to 200 milliseconds with the values shown.

The signal output is buffered with the CD4041A to allow the pulse generator to drive any required load. The circuit shown has the advantages of being compact, battery-powered, and COS/MOS compatible. In addition, it is capable of being run from the same power supply as the device under test to assure that the input levels are the same as V_{DD} when the power-supply voltage is varied.

MISCELLANEOUS APPLICATIONS

The basic properties of good stability in the astable mode, and stable pulse delay and width control in the monostable mode, make the CD4047A a useful building block in many systems, such as PMOS clock generation, audio tone gener-

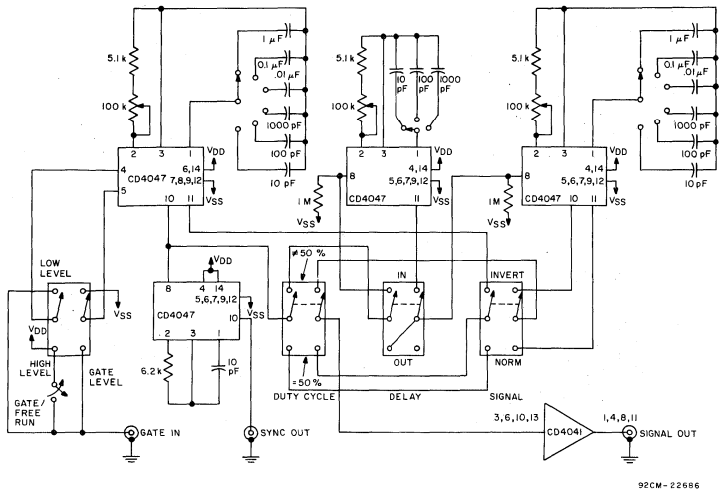


Fig. 34 – Pulse-generator circuit.

ation, semiconductor memory systems, semiconductor memory exercisers, and general-purpose functional-testing systems. This Application Note will serve as a guideline in incorporating the CD4047A in a system design.

REFERENCES

1. **"CD4047A COS/MOS Low-Power Monostable/Astable Multivibrator,"** RCA Data Bulletin, File No. 623
2. **"Astable and Monostable Oscillators Using RCA COS/MOS Digital Integrated Circuits,"** by J. A. Dean and J. P. Rupley, RCA Application Note ICAN-6267

ACKNOWLEDGMENTS

The assistance of R. Vaccarella in the designing of some of the application circuits shown and in obtaining laboratory measurements used in plotting the curves shown in this Note is acknowledged.

Appendix A –
Calculation of the Period of an Astable Multivibrator Using a Single RC Time Constant

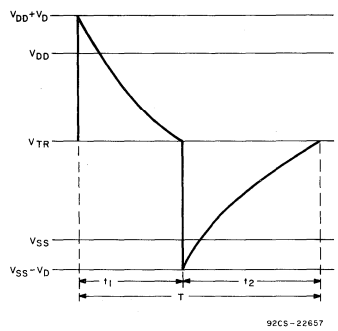


Fig. A-1 – RC oscillator waveform for the circuit of Fig. 1.

In Fig. A-1:

t_1: $V_{TR} = (V_{DD} + V_D)\, e^{-t_1/RC}$

$$t_1 = -RC \ln \frac{V_{TR}}{V_{DD} + V_D}$$

t_2: $V_{DD} - V_{TR} = (V_{DD} + V_D)\, e^{-t_2/RC}$

$$t_2 = RC \ln \frac{V_{DD} - V_{TR}}{V_{DD} + V_D}$$

And the period of an astable multivibrator using a single RC time constant is:

$$T = t_1 + t_2 = -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_D)^2}$$

Appendix B –
Analysis of Circuit Shown in Fig. 4

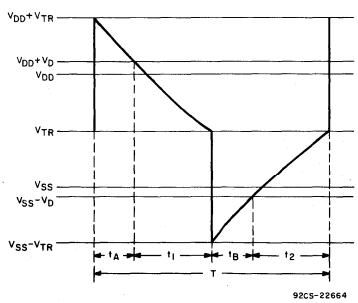


Fig. B-1 – RC waveform for the circuit of Fig. 4.

In Fig. B-1:

t_1: $V_{TR} = (V_{DD} + V_D)\, e^{-t_1/RC}$

$$t_1 = -RC \ln \frac{V_{TR}}{V_{DD} + V_D}$$

t_2: $V_{DD} - V_{TR} = (V_{DD} + V_D)\, e^{-t_2/RC}$

$$t_2 = -RC \ln \frac{V_{DD} - V_{TR}}{V_{DD} + V_D}$$

t_A

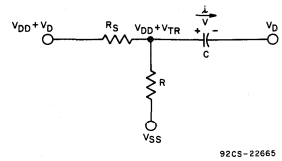


Fig. B-2 – Initial conditions for solving period t_A.

Circuit initial conditions are shown in Fig. B-2. In the figure

$$-C\frac{dv}{dt} = \frac{V + V_{DD}}{R} + \frac{V + V_{DD} - (V_{DD} + V_D)}{R_S} \qquad (B\text{–}1)$$

t_B

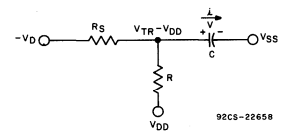


Fig. B-3 – Initial conditions for solving period t_B.

Circuit initial conditions as shown in Fig. B-3. In the figure

$$C\frac{dv}{dt} = \frac{V_{DD} - V}{R} - \frac{V_D + V}{R_S} \qquad (B\text{–}3)$$

Solving Eq. (B-3) for V the final voltage across the capacitor, yields

$$V = C_2 e^{-K_1 t_B} - \frac{K_2}{K_1} \qquad (B\text{–}4)$$

where $C_2 = V_{TR} - V_{DD}$ = initial voltage across capacitor

K_1, K_2 are same values as for above for t_A.

Eq. (B-1) is solved for V; the final voltage across the capacitor is

$$V = C_1 e^{-K_1 t_A} + \frac{K_2}{K_1} \qquad (B\text{–}2)$$

where $C_1 = V_{TR}$ = initial voltage across capacitor

$$K_1 = \frac{R_S + R}{R_S RC}$$

$$K_2 = \frac{V_D R - R_S V_{DD}}{R_S RC}$$

By inserting these values into Eq. (B-2) and setting the final voltage across the capacitor, V, to V_D, t_A becomes

$$t_A = -\left[\frac{R_S RC}{R_S + R}\right] \ln \frac{R_S [V_{DD} + V_D]}{R_S [V_{DD} + V_{TR}] + R [V_{TR} - V_D]}$$

Insertion of these values into Eq. (B-4), with $V = -V_D$ yields

$$t_B = -\left[\frac{R_S RC}{R_S + R}\right] \ln \frac{R_S [V_{DD} + V_D]}{R_S [2 V_{DD} - V_{TR}] + R [V_{DD} - V_{TR} - V_D]}$$

and $T = t_1 + t_2 + t_A + t_B$

The equations for t_A, t_B, and T can be simplified by expressing R_S as a multiple of R. Let $K = \frac{R_S}{R}$ and combining the expressions for t_1 and t_2. The resulting expression for T is

$$T = -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_D)^2}$$

$$-\left(\frac{K}{K+1}\right) RC \ln \frac{K [V_{DD} + V_D]}{K [V_{DD} + V_{TR}] + [V_{TR} - V_D]}$$

$$-\left(\frac{K}{K+1}\right) RC \ln \frac{K [V_{DD} + V_D]}{K [2 V_{DD} - V_{TR}] + [V_{DD} - V_{TR} - V_D]}$$

Appendix C –
Calculation for Period of Astable Multivibrator Using Integrated Techniques

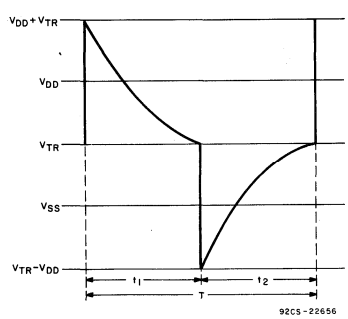


Fig. C-1 – CD4047A RC oscillator waveform.

In Fig. C-1

t_1: $V_{TR} = (V_{DD} + V_{TR}) e^{-t_1/RC}$

$$t_1 = RC \ln \frac{V_{TR}}{V_{DD} + V_{TR}}$$

t_2: $V_{DD} - V_{TR} = (2 V_{DD} - V_{TR}) e^{-t_2/RC}$

$$t_2 = -RC \ln \frac{V_{DD} - V_{TR}}{2 V_{DD} - V_{TR}}$$

And the period of the astable multivibrator using integrated techniques is

$$T = -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_{TR})(2 V_{DD} - V_{TR})}$$

Appendix D –

Power Needed for Charge and Discharge of an External Capacitor During One Cycle

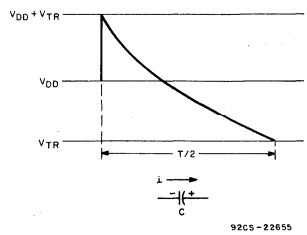


Fig. D-1 – Waveform for calculating power dissipation.

Assume for this calculation that V_{TR} = 50-per-cent V_{DD}, and that T = 2.2 RC. Since charge and discharge cycles are symmetrical, the calculation can be performed by analyzing a discharge cycle only. See Fig. D-1.

$$V = 1.5\,V_{DD}\,e^{-t/RC}$$

$$\frac{dv}{dt} = -\left(\frac{1}{RC}\right)(1.5\,V_{DD})\left(e^{-t/RC}\right)$$

$$P = \frac{1}{(T/2)}\int_0^{T/2} CV\frac{dv}{dt}\,dt$$

$$= \frac{2C}{T}\int_0^{T/2} \left(1.5\,V_{DD}\,e^{-t/RC}\right)\left(\frac{1}{RC}\right)(1.5\,V_{DD})\,e^{-t/RC}\,dt$$

$$= \frac{4.5C}{T}\,\frac{V_{DD}^2}{RC}\int_0^{T/2} e^{-2t/RC}\,dt$$

$$= -\frac{2.25C\,V_{DD}^2}{T}\,e^{-2t/RC}\,\Big|_0^{T/2}$$

Substituting T = 2.2 RC

$$P = -\frac{C}{T}(2.25)\,V_{DD}^2\,[e^{-2.2} - 1] = \frac{2.0\,C}{T}V_{DD}^2$$

$$P = 2\,CV^2f$$

Appendix E –

Equations for Pulse Width T_M of CD4047A in Monostable Mode

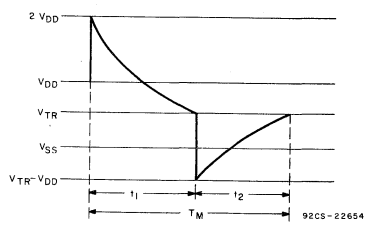


Fig. E-1 – CD4047A RC waveform, monostable mode.

Note that the waveform in Fig. E-1 is not symmetrical because the timing capacitor is initially charged to V_{DD}. In the monostable mode, the circuit goes through one cycle only.

t_1: $V_{TR} = 2\,V_{DD}\,e^{-t_1/RC}$

$$t_1 = -RC\ln\frac{V_{TR}}{2\,V_{DD}}$$

t_2: $V_{DD} - V_{TR} = (2\,V_{DD} - V_{TR})\,e^{-t_2/RC}$

$$t_2 = -RC\ln\frac{V_{DD} - V_{TR}}{2\,V_{DD} - V_{TR}}$$

And the equation for the pulse width, T_M, of a CD4047A in the monostable mode is:

$$T_M = t_1 + t_2 = -RC\ln\frac{(V_{TR})(V_{DD} - V_{TR})}{(2\,V_{DD})(2\,V_{DD} - V_{TR})}$$

Monostable Power Dissipation

To calculate the power dissipation for the circuit in the monostable mode, refer to Fig. E-1. If it is assumed that V_{TR} = 50-per-cent V_{DD}, Fig. 14 shows that T_M = 2.485 RC. t_2 is the same as in the astable calculation, i.e., t_2 = 1.10 RC and $P_{t2} = CV^2f$ for V_{TR} = 50-per-cent V_{DD}. Thus, t_1 in the monostable mode = 2.485 RC – 1.10 RC = 1.385 RC.

$$P = \frac{1}{T_M}\left[\int_0^{t_1} CV\frac{dv}{dt}\,dt + \int_{t_1}^{t_2} CV\frac{dv}{dt}\,dv\right]$$

$$= \frac{1}{T_M}\int_0^{t_1} CV\frac{dv}{dt}\,dt + \frac{1}{T_M}CV^2$$

where $V = 2\,V_{DD}\,e^{-t/RC}$ and

$$\frac{dv}{dt} = -\left(-\frac{1}{RC}\right)(2\,V_{DD})\,e^{-t/RC}$$

$$P_{t1} = \frac{C}{T_M}\int_0^{t_1} \left(2\,V_{dd}\,e^{-t/RC}\right)\left(\frac{1}{RC}\right)(2\,V_{dd}\,e^{-t/RC})\,dt$$

$$= \frac{C}{T_M}\,\frac{4\,V_{dd}^2}{RC}\int_0^{t_1} e^{-2t/RC}\,dt$$

$$= -\frac{C}{T_M}\,2\,V_{dd}^2\,e^{-2t/RC}\,\Big|_0^{t_1}$$

Substituting t_1 = 1.385 RC

$$P_{t1} = -\frac{C}{T_M}\,2\,Vdd^2\,[e^{-2.77} - 1] = \frac{1.875\,C\,Vdd^2}{T_M}$$

$$P = P_{t1} + P_{t2} = (1.875 + 1)\frac{C\,Vdd^2}{T_M} = 2.875\,\frac{C\,Vdd^2}{T_M}$$

For a repetitive output from the CD4047A

$$P = \frac{2.875\,C\,Vdd^2}{T_M} \times \text{duty cycle}$$

Astable and Monostable Oscillators Using RCA COS/MOS Digital Integrated Circuits

by J. A. Dean and J. P. Rupley

COS/MOS integrated logic circuits are being widely used in digital and other applications because of their inherent advantages of high noise immunity, extremely low power dissipation, and tolerance to wide variations in power-supply voltages and operating-temperature ranges. In addition to these features, COS/MOS gates can provide cost and size reductions in multivibrator circuits because their high input impedance makes it possible to obtain large time constants without the use of large capacitors. This Note describes several techniques which may be used to compensate for the normal threshold variation of MOS devices in the design of stable multivibrator circuits for operation at frequencies up to 1 MHz. The circuits shown can be formed by use of COS/MOS Inverters or by use of COS/MOS NAND or NOR gates connected in an inverter configuration. NAND and NOR gates perform the inverter function when all of the gate inputs are tied together. This Note also describes various applications for COS/MOS multivibrator circuits, (i.e., voltage-controlled oscillators, voltage controlled pulse-width circuits, phased-locked voltage controlled oscillators, frequency multipliers, and modulator/demodulator (envelope detectors).

ASTABLE CIRCUITS

Fig. 1(a) shows an astable multivibrator circuit that uses two COS/MOS inverters, and Fig. 1(b) shows the related waveforms. This simple circuit requires only one resistor and one capacitor, and operates in the following manner. When the waveform 1 at the output of inverter B is in a high or "one" state, capacitor C_{tc} becomes charged positive. As a result, the input to inverter A is high and its output is low or "zero".

Resistor R_{tc} is returned to the output of inverter A to provide a path to ground for discharge of capacitor C_{tc}.

As long as the output of A is low, the output of inverter B is high. As capacitor C_{tc} discharges, however, the voltage generated [waveform 2 in Fig. 1(b)] approaches and passes through the transfer voltage point of inverter A. At the instant that this crossover occurs, the output of A becomes high; as a result, the output of B becomes low and the capacitor C_{tc} is charged negative (or low). The resistor R_{tc} connected to the output of A then provides a charge path to a supply voltage. Capacitor C_{tc} begins to charge to this voltage, and again the voltage approaches and passes through the transfer voltage point of inverter A. At that instant, the circuit again changes state (the output of A becomes low and that of B high) and the cycle repeats.

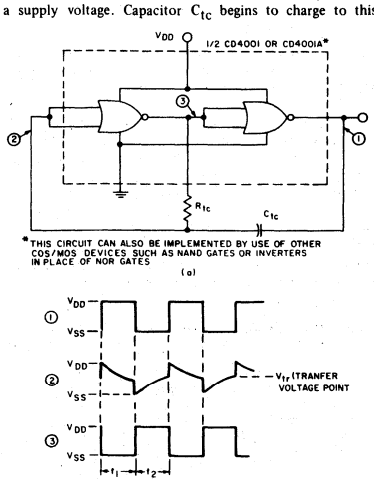


Fig. 1 - Astable multivibrator circuit that uses two COS/MOS inverters: (a) circuit diagram; (b) voltage waveforms.

Because of the input-diode protection circuits included in the COS/MOS IC, shown in Fig. 2, the generated drive waveform is clamped between V_{DD} and V_{SS}. Consequently, the time to complete one cycle is approximately 1.4 times the RC time constant because one time constant is used to control the switching of both states of the multivibrator circuit. Switching occurs when the charge or discharge reaches the transfer voltage level, or when the time period reaches 70.7 per cent of its discharge. As shown in waveform 2 of Fig. 1(b), the transfer voltage point V_{tr} is the same for t_1 and t_2. The time period T for one cycle can be computed as follows:

$$T = t_1 + t_2$$

$$t_1 = -RC \ln \frac{(V_{DD} - V_{tr})}{V_{DD}}$$

$$t_2 = -RC \left[\ln \frac{V_{tr}}{V_{DD}} \right]$$

$$T = -RC \left[\ln \frac{(V_{DD} - V_{tr})}{V_{DD}} + \ln \frac{V_{tr}}{V_{DD}} \right] \quad (1)$$

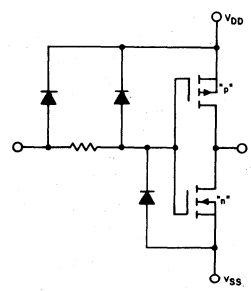


Fig. 2 - Diode protection circuit.

If the time constant is assumed to be 1×10^{-6} second and the transfer voltage V_{tr} is allowed to vary from 33 to 67 per cent of V_{DD}, the period T varies from 1.4 microseconds at a value of V_{tr} equal to half of V_{DD} to 1.5 microseconds at either the 33 or 67 per cent value of V_{DD}. Therefore, the maximum variation in the time period T is only 9 per cent with a ±33-per-cent variation in transfer voltage from unit to unit.

The oscillator can be made independent of supply-voltage variations by use of a resistor in series with the input lead to inverter A, as shown in Fig. 3(a). This resistor R_s should be at least twice as large as the resistor R_{tc} of the time constant to allow the voltage waveform generated at the junction of R_s, R_{tc}, and C_{tc} to rise to $V_{DD} + V_{tr}$. The waveform is still clamped at the input between V_{DD} and V_{SS}, as shown by the waveforms in Fig. 3(b). The use of resistor R_s provides several advantages in the circuit. First, because the RC time constant controls the frequency, the over-all maximum variations in the time period are reduced to less than 5 per cent with variations in transfer voltage, as determined by the following equation:

$$T = -RC \ln \left[\frac{V_{tr}}{(V_{DD} + V_{tr})} + \ln \frac{(V_{DD} - V_{tr})}{2V_{DD} - V_{tr}} \right] \quad (2)$$

The resistor R_s also makes the frequency independent of supply-voltage variations. Table I shows data measured on typical units with and without the resistor.

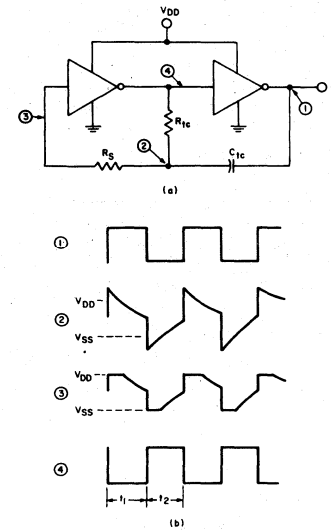


Fig. 3 - Addition of resistor in series with input to one COS/MOS inverter to make oscillator circuit independent of supply-voltage variations: (a) circuit diagram; (b) voltage waveforms.

Fig. 4 shows a typical transfer characteristic as a function of temperature. It can be seen that there is very little change in the characteristic from low to high temperature. Because the oscillator can also tolerate changes in the transfer characteristic without frequency instability, it requires no thermal compensation. The frequency at -55°C is the same as at +125°C. Table II shows data measured on typical units at temperature extremes.

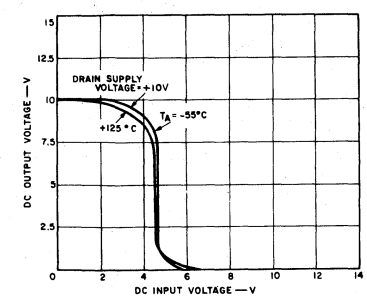


Fig. 4 - Transfer characteristic as a function of temperature.

The astable multivibrator shown in Fig. 1 can be gated on and off by use of a NOR or NAND gate as the first inverter, as shown in Fig. 5.

COMPENSATION FOR 50-PER-CENT DUTY CYCLES

The variation in transfer voltage described above affects the output-pulse duty cycle, as shown in Fig. 6. A true square-wave pulse is obtained only when the transfer voltage

Table I - Frequency variations of astable multivibrator with and without series resistor.

Unit No.	V_{tr} @ V_{DD} = 10V (V)	Period Without Rs - (ms)			Period With Rs - (ms)		
		V_{DD} = 6V	V_{DD} = 10V	V_{DD} = 14V	V_{DD} = 6V	V_{CC} = 10V	V_{CC} = 14V
2	4.77	0.735	0.66	0.645	1.04	1.00	1.02
6	5.78	0.715	0.665	0.63	1.06	1.04	1.03
11	5.58	0.695	0.66	0.625	1.03	1.02	1.03
13	5.00	0.70	0.665	0.64	1 03	1.01	1.02
20	5.56	0.70	0.665	0.64	1.04	1.03	1.03

R_{tc} = 0.4 megohm, C_{tc} = 1000pF, R_s = 0.8 megohm

Table II - Frequency variations of astable multivibrator at temperature extremes.

Unit No.	Period - (ms)					
	V_{DD} = 6V		V_{DD} = 10V		V_{DD} = 14V	
	-55°C	+125°C	-55°C	+125°C	-55°C	+125°C
2	1.04	1.04	1.02	1.01	1.03	1.02
6	1.06	1.07	1.06	1.04	1.04	1.03
11	1.03	1.03	1.04	1.02	1.04	1.01
13	1.02	1.02	1.02	1.02	1.03	1.01
20	1.04	1.03	1.04	1.03	1.04	1.02

R_{tc} = 0.4 megohm, C_{tc} = 1000pF, R_s = 0.8 megohm

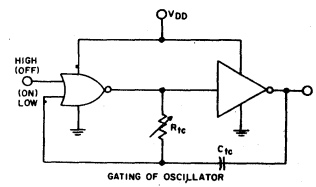


Fig. 5 - Astable multivibrator in which a NOR or NAND gate is used as the first inverter to permit gating of the multivibrator.

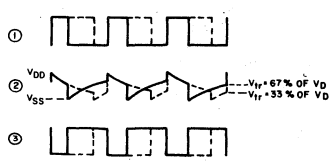


Fig. 6 - Waveforms showning effects of transfer voltage on multivibrator frequency.

occurs at the 50-per-cent point. However, the duty cycle can be controlled if part of the resistance in the RC time constant is shunted out with a diode, as shown in Fig. 7.

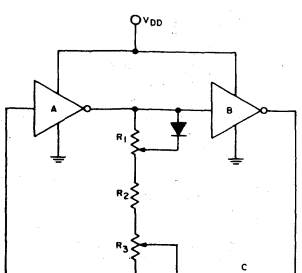


Fig. 7 - Astable multivibrator in which a duty-cycle control is added.

Because adjustment of this diode shunt to obtain a specific pulse duty factor causes the frequency of the circuit to vary, a frequency control R_3 is added to compensate for this variation. It may also be necessary to reverse the diode to obtain the desired duty factor. The frequency of any of the circuits shown can be made variable by use of a potentiometer for resistor R_{tc}.

MONOSTABLE CIRCUITS

Basic Configuration. Fig. 8(a) shows a basic "one-shot" circuit that uses a single RC time constant. This circuit operates well provided it is adjusted to the particular COS/MOS unit used. If no adjustment is made, however, the period T can vary from unit to unit by as much as -40 per cent to +60 per cent if the transfer voltage varies by ±33 per cent, as shown by the waveforms in Fig. 8(b).

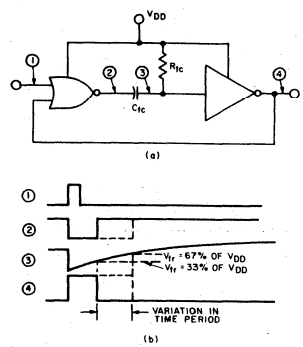


Fig. 8 - Basic one-shot multivibrator circuit: (a) circuit diagram; (b) waveforms.

Compensated Monostable Circuit. Fig. 9 shows a compensated monostable multivibrator type of circuit that can be triggered with a negative-going pulse (V_{DD} to ground). In the quiescent state, the input to inverter A is high and the output low; therefore, the output of inverter B is high. When a negative-going pulse or spike is introduced into the circuit, as

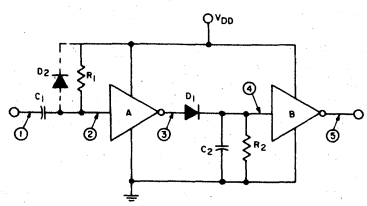


Fig. 9 - Compensated monostable multivibrator circuit.

shown in the waveforms of Fig. 10, capacitor C_1 becomes negatively charged to ground and the output of inverter A becomes high. Capacitor C_2 then charges to V_{DD} through the diode D_1 and inverter A, and the output of inverter B becomes low. As capacitor C_1 discharges negatively, it charges through resistor R_1 to V_{DD} (waveform 2). The output of inverter A remains high until the voltage waveform generated by the charge of C_1 passes through the transfer voltage of inverter A; at that instant its output becomes low. Diode D_1 temporarily prevents the discharge of capacitor C_2, which was charged when inverter A was high (waveform 3). Capacitor C_2 then commences to discharge to ground through resistor R_2 (waveform 4). The output of inverter B remains low until the waveform generated by the discharge of C_2 passes through the transfer voltage point of inverter B; at that point the output returns to its high state (waveform 5).

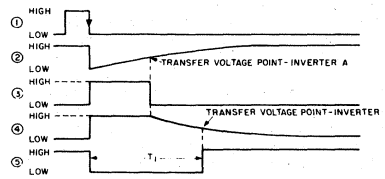


Fig. 10 - Voltage waveforms for monostable multivibrator circuit when a negative-going trigger pulse is applied.

The advantage of using two inverters fabricated on the same chip is that they have similar transfer voltages. When two equal RC time constants are used (R_1C_1 equals R_2C_2), the effects of variations in transfer voltage from device to device are effectively cancelled out, as shown in Fig. 11. By use of Eq.(1) derived for the astable oscillator, it can be shown that the maximum variation in the time period T is less than 9 per cent. The total time for one period T_1 is approximately 1.4 times the R_1C_1 time constant.

Unlike the astable circuit, which shows no variation in frequency over the temperature range from -55°C to +125°C,

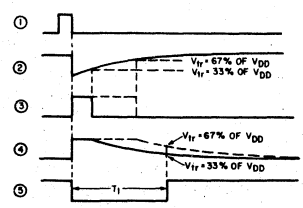


Fig. 11 - Waveforms showing the cancelling effects of transfer-voltage variations of the two COS/MOS inverters when two equal time constants are used.

the monostable multivibrator shows some change in time period. The variation is less than 10 per cent. Table III shows data measured on five units over the temperature range. At 25°C, the variation in the time period T from unit to unit is quite small, usually less than 5 per cent at a V_{DD} of 10 volts.

The output from inverter B can be held in the low or zero state as long as the R_2C_2 time constant is recharged by another triggering pulse before the discharge waveform it generates passes through the transfer voltage of inverter B.

Table III - Frequency variations of monostable multivibrator at three temperatures.

Unit No.	Period @ V_{DD} = 10V - (ms)		
	-55°C	+25°C	+125°C
2	1.06	1.08	1.00
6	1.015	1.03	0.99
11	1.00	1.02	0.98
13	1.01	1.03	0.97
20	1.02	1.02	0.99

$R_1 = R_2 = 1$ megohm, $C_1 = C_2 = 0.001\mu F$

Diode D_2 in Fig. 9 is internal to the COS/MOS circuit. As discussed for the astable oscillator, it is part of the input protection circuit shown in Fig. 2, and serves to clamp the input at V_{DD}.

Figs. 12 and 13 show two variations of the monostable circuit, together with their associated waveforms. The circuit of Fig. 12 triggers on the negative-going excursions of the input pulse, in the same manner as the circuit of Fig. 9. The output pulse is positive-going and is taken from the first inverter. This circuit does not need an external diode. The circuit of Fig. 13 triggers on the positive-going excursion of the input pulse, and then locks back on itself until the RC time constants complete their discharge. The circuits of Figs. 12 and 13 cannot be retriggered until they return to their quiescent states.

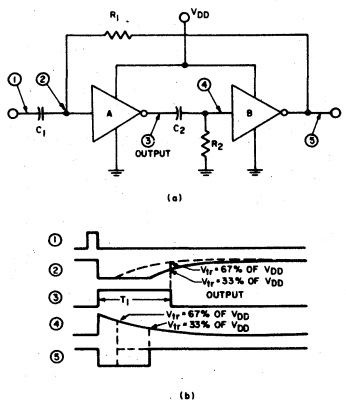


Fig. 12 - Monostable multivibrator that is triggered by a negative-going input pulse: (a) circuit diagram; (b) waveforms.

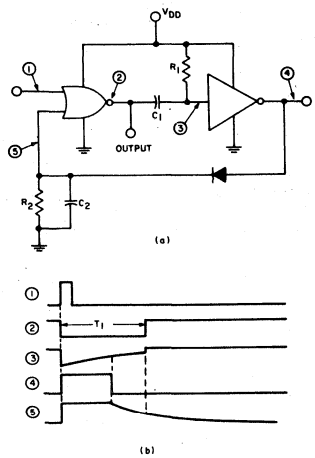


Fig. 13 - Monostable multivibrator that is triggered by a positive-going input pulse: (a) circuit diagram; (b) waveforms.

Low-Power Monostable Circuit. The monostable circuits discussed thus far dissipate some power because one or both of the inverters are on during the charging or discharging of the RC time constants. This power dissipation will be extremely low provided the "one-shot" pulse width is short compared to the over-all cycle time. Fig. 14 shows the current waveform associated with the circuit of Fig. 9. This

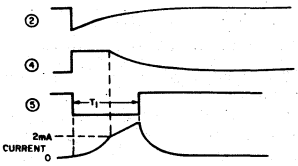


Fig. 14 - Current waveforms for the diode-compensated multivibrator shown in Fig. 9.

waveform is quite wide at the base, and some current flows for approximately twice the time period. Fig. 15(a) shows a circuit using the RCA CD4007 or CD4007A which dissipates much less power than the other circuits shown, but does not have the same stability. This circuit operates as shown by the waveforms in Fig.15(b). In the quiescent state, the p-channel transistor of the first inverter is biased off, while the n-channel transistor (which derives its control from the output of the second inverter) is biased on. Therefore, the output at C is low, and that at D is high. When a negative-going pulse is introduced into the circuit through capacitor C_1, the R_1C_1 time constant becomes negatively charged, and the p-channel device is turned on. Capacitor C_2 then charges to V_{DD}, the output at D becomes low, and the n-channel device of the first inverter is turned off. Capacitor C_1 immediately begins to charge to V_{DD} through R_1 (waveform B). The p-channel transistor remains on, keeping capacitor C_2 charged to V_{DD}, until the waveform generated passes through its threshold voltage level and turns it off. The n-channel transistor of the first inverter is still off because the output of the second inverter (waveform D) is still low. When the p-channel device of the first inverter turns off, capacitor C_2 begins to discharge through resistor R_2 (waveform C) to ground. As it discharges, it passes through the threshold voltage of the second p-channel transistor so that it begins to turn on. The voltage waveform at D then begins to rise, and the n-channel device of the first inverter turns on and provides a second discharge path for the capacitor C_2. As a result, the output waveform changes state from low to high quite rapidly to complete the cycle.

The major advantage of the circuit of Fig. 15 is its low power dissipation. Because the circuit depends on the p-channel

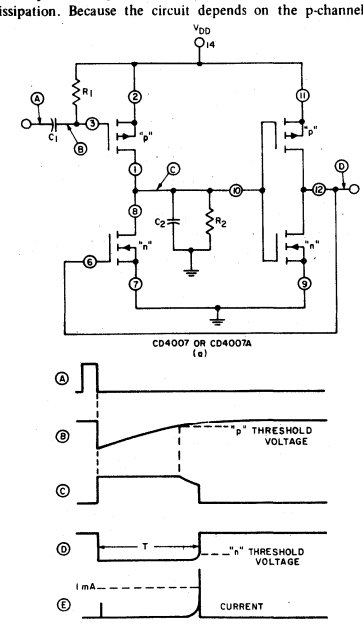


Fig. 15 - Low-power monostable multivibrator: (a) circuit diagram; (b) waveforms.

transistor threshold, the time period T varies from unit to unit or with temperature variations. Some compensation can be provided if the R_2C_2 time constant is made approximately 3 times larger than the R_1C_1 time constant, as shown in Table IV.

Table IV - Frequency variations of monostable multivibrator with temperature when R_2C_2 time constant is increased.

	Period with V_{DD} = 10V - (μs)		
Unit No.	-55°C	+25°C	+125°C
553	1090	1120	1160
554	1060	1090	1120
810	1030	1030	1020
900	1000	1020	990
939	1080	1100	1050

R_1 = 0.35 megohm, C_1 = 0.001μF

R_2 = 1 megohm, C_2 = 0.001μF

R_2C_2 is approximately 3 times the time constant R_1C_1

For minimum current in the circuit of Fig. 15, capacitor C_2 can be removed so that only stray capacitance is present at the input of the second inverter. A comparison of time-period variations under this condition is shown in Table V. Again, the variations from unit to unit are caused by differences in p-channel transistor threshold.

Table V - Frequency variations of monostable multivibrator with temperature when C_2 consists of stray capacitance only.

	Period with V_{DD} = 10V - (μs)		
Unit No.	-55°C	+25°C	+125°C
553	870	940	1020
554	900	970	1050
810	900	1000	1080
900	810	880	960
939	780	850	920

R_1 = 0.62 megohm, C_1 = 0.001 μF

R_2 = 1 megohm, C_2 = strays

Applications

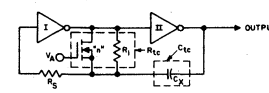
Fig. 16 shows a circuit similar to the circuit in Fig. 3a. C_{tc} is variable (by adjustment of C_X) and R_{tc} is variable (by adjustment of V_A). The value of R_{tc} varies from $\approx$ 1kΩ to 10kΩ. These limits are determined by the parallel combination of R1 (10kΩ) and the n-channel device resistance. This varies from 1kΩ (R_{ON}) to $\approx 10^9\Omega$ (R_{OFF}).

When $V_A = V_{SS}$, the n-channel device is "OFF" and $R_{tc} = R_{OFF}/\!/R1 \approx R1 = 10k\Omega$

because $R_{OFF} \gg R1$.

When $V_A = V_{DD}$, the n-channel device is fully "ON.. and $R_{tc} = R_{ON}/\!/R1 \approx R_{ON} = 1k\Omega$

because $R_{ON} \ll R1$.



NOTE:
INVERTERS AND n-CHANNEL DEVICE ARE AVAILABLE IN A SINGLE COS/MOS PACKAGE
1 - CD4007 OR CD4007A*
TYPICAL VALUES:
R_1 = 10 kΩ C_X = 0.001 - 0.004 μF
R_S = 100 kΩ 0 $\leq V_A \leq V_{DD}$

* USE PROPER SUFFIX TO DENOTE PACKAGE REQUIRED - SEE APPENDIX.

Fig. 16 – Voltage-controlled oscillator.

The oscillator center frequency is varied by adjustment of C_X. Table VI shows a comparison of the period of the output waveform as a function of V_{DD} and V_A.

Table VI - Period of Output as a function of Va and V_{DD} - V.C.O. of Fig. 16.

	Period (μsec)		
V_A	V_{DD} = 5V	V_{DD} = 10V	V_{DD} = 15V
0	120	54	48
5	115	45	41
10	---	32	30
15	---	---	24

Voltage-Controlled Pulse-Width Circuit

Fig. 17a shows a further modification of the circuit of Fig. 3a which modulates the pulse width (by varying V_A) only if R_X is sufficiently high. As an example; if C = 0.0022μF, then $R_X \approx 35k\Omega$. Lower values of R_X cause the frequency to be affected. If $R_X < 10k\Omega$, there is a value of V_A which will cause the oscillator to cut off. Table VII lists values of pulse width (B in Fig. 17b) for various values of V_A and V_{DD}. Fig. 17b shows the output waveform for the circuit described.

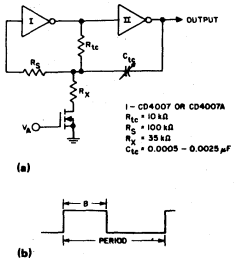


Fig. 17 - (a) V.C. pulse-width circuit; (b) output waveform.

Table VII - Pulse Width as a Function of V_A and V_{DD}.

V_A	Pulse Width (B) μsec		
	V_{DD} = 5V Period-41.5	V_{DD} = 10V Period-35	V_{DD} = 15V Period-33
0	23	19.3	17
5	20	17.7	16.2
10	—	16.2	15.5
15	—	—	14.3
C_{tc} = 0.0015μF			

Phase Locked VCO

The voltage controlled oscillator can be operated as a phase locked oscillator by the application of a frequency controlled voltage to the gate of the n-channel device. Fig. 18 shows the block diagram an FM discriminator using the phase locked VCO. Block A is the same circuit as Fig. 16. The output of the phase comparator is fed to the gate of the n-channel device (V_A). If the two inputs to the phase comparator are different, the change of V_A causes the output frequency of the VCO to change. This change is divided by 2^N and fed back to the phase comparator.

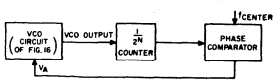


Fig. 18 – VCO used in phase-locked loop.

Frequency Multipliers

Fig. 19a shows a frequency doubler. A 2^N multiplier can be realized by cascading this circuit with N-1 other identical circuits. The leading edge of the input signal is differentiated by R1 and C1, applied to the input No. 1 of the NAND gate, and produces a pulse at the output. The trailing edge of the input pulse, after having been inverted, is differentiated, applied to the input No. 2 of the NAND gate, and produces the second output pulse from the NAND gate. The waveforms for 5 points in the circuit are shown in Fig. 19b.

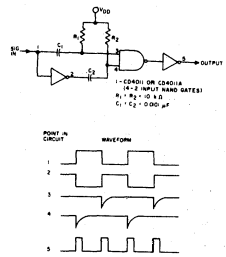


Fig. 19 - (a) Frequency doubler schematic; (b) waveforms.

Modulation/Demodulation (Envelope Detection).

Pulse modulation may be accomplished by use of the circuit shown in Fig. 20a. This circuit is a variation of Fig. 3. The oscillator is gated ON or OFF by the signal input No. 1 to the NAND gate. The waveforms are shown in Fig. 20b.

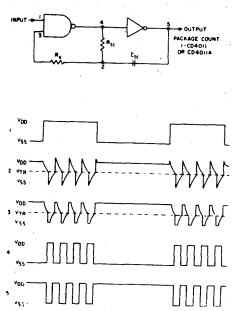


Fig. 20 - (a) Modulator circuit; (b) waveforms.

Demodulation or envelope detection of pulse modulated waves is performed by the circuit shown in Fig. 21a. The carrier burst is inverted (by Inverter A), and its first negative transition at point 2, turns on the diode (D) to provide a charging path for C_{tc} through the n-channel resistance to ground. On the positive transition of the signal (at point 2), the diode is cut off and C_{tc} discharges through R_{tc}. The discharge time constant (R_{tc} C_{tc}) is much greater than the time of the burst duration. Point 3, therefore, never reaches the switch point of inverter B until the burst has ended. The waveforms for 4 points in the circuit are shown in Fig. 21b.

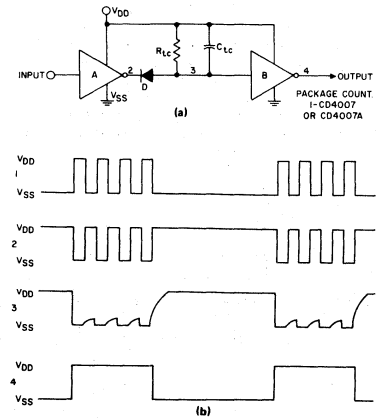


Fig. 21 - (a) Demodulator circuit; (b) waveforms.

Appendix

The RCA COS/MOS product line includes a standard line of devices designed to operate from voltage supplies of 5 to 15V and a low voltage "A" series designed to operate from voltage supplies of 3 to 15V. These devices are available in any of the package types or temperature ranges shown in Table A.

TABLE A

Package			Operating Temperature Range (°C)
Type	Suffix		
	5-15V	3-15V ("A")	
Dual-in-line ceramic	D	D	–55 to +125
Plastic	E	E	–40 to +85
Flat Pack	–	K	–55 to +125

When ordering COS/MOS devices, the appropriate suffix should be affixed to the number of the device required, (i.e., if a low voltage plastic package, four-bit full adder is desired, order CD4008AE). This Note is applicable to both COS/MOS product lines, and all package types mentioned above.

COS/MOS Interfacing Simplified

by D. Blandford and A. Bishop

COS/MOS with its wide range of operating supply voltages, low input current, and low power consumption, interfaces easily with many electronic devices. In addition, COS/MOS circuitry can easily be added to a system and can often be operated from the existing power supply. Examples of practical circuits for a wide variety of interfacing situations are given in this Note; design constraints are included in each case.

Note that the CD4000 Series type numbers are followed by a suffix letter, A or B, which specifies the maximum operating voltage for the device: A, 3 to 15 volts; B, 3 to 18 volts. The outputs of all B-type devices are buffered and have the same output drive current and equal source and sink capabilities. Table I shows some characteristics of B-type devices.

Table I – Output Drive Current—B-Type Devices

Output Drive Current	Symbol	V_{DD} Volt	V_O Volt	BD, BK, BF, BH –55°C Min.	BD, BK, BF, BH +25°C Min.	BD, BK, BF, BH +125°C Min.	BE –40°C Min.	BE +25°C Min.	BE +85°C Min.	BE +25°C Typ.	Units
Sink	I_{DN}	5	0.4	0.5	0.4	0.3	0.45	0.4	0.36	0.8	mA
		10	0.5	1.1	0.9	0.65	1.0	0.9	0.75	1.8	mA
		5	4.6	–0.5	–0.4	–0.3	–0.45	–0.4	–0.36	–0.8	mA
Source	I_{DP}	5	2.5	–2.0	–1.6	–1.15	–1.8	–1.6	–1.3	–3.2	mA
		10	9.5	–1.1	–0.9	–0.65	–1.0	–0.9	–0.75	–1.8	mA

COS/MOS to TTL

In interfacing TTL with COS/MOS with a common power supply of between 4.5 and 5.5 volts, the guaranteed active-pull-up TTL output voltage of 2.4 volts is lower than the minimum COS/MOS input voltage required to guarantee switching, 3.5 volts, Fig. 1. This difference is overcome by the use of an external resistor, R_X in Fig. 2, which is also the resistor to be used for open-collector-output TTL at a V_{DD} of 5 volts. The minimum value of R_X is fixed by the maximum sink current, e.g., 1.6 milliamperes for 74-series TTL, its maximum value by I_{OH}, the off leakage of the output sink transistor. As shown in Table II, the values of R_X between 1.5 and 4.7 kilohms are suitable for all the TTL families under worst-case conditions. The COS/MOS input impedance is essentially "capacitive", which means that many COS/MOS inputs may be driven by a single TTL output. The actual number depends on the frequency of operation.

In the COS/MOS to TTL interface, Fig. 3, the requirement is to sink sufficient current in the low output state at a maximum output voltage of 0.4 volt. Table III gives the current sinking capability of some CD4000-series devices. Note that all B-type devices have the same standard output drive and are capable of sinking two low-power TTL loads, worst case. For the higher power types of TTL, the CD4049A and CD4050A buffers may be used. Table IV shows the minimum and typical fanout for each TTL family. The buffer takes its power from the 5-volt TTL supply and has an additional advantage in that it can accept input voltage swings of 5 to 15 volts from the preceding COS/MOS system.

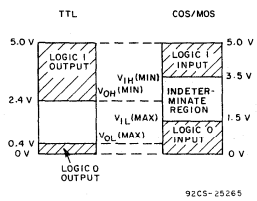


Fig. 1—TTL to COS/MOS voltage levels.

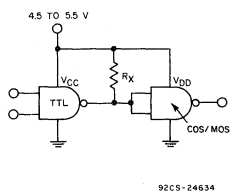


Fig. 2—TTL to COS/MOS interface.

Table II—Values of R_X for TTL—COS/MOS Interface

Characteristic	74	74H	74L	74LS	74S
R_X min. (ohms)	390	270	1.5k	820	270
R_X max. (kilohms)	4.7	4.7	27	12	4.7

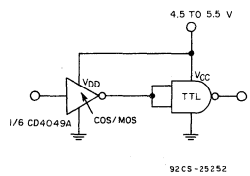


Fig. 3—COS/MOS to TTL interface.

To gain improvements in speed and noise immunity in a system using a COS/MOS supply voltage greater than +5 volts, high-voltage open-collector TTL circuits such as the 7416, 7417 or 7426 may be used, as shown in Fig. 4. The value of the pull-up resistor R_X will depend on the actual value of V_{DD}; at 10 volts, 39 kilohms would be suitable.

COS/MOS to HNIL

The wide operating-voltage range and low power consumption of COS/MOS circuitry enables it to operate from the HNIL power supply. Most CD4000A circuits will drive the HNIL input directly; for example, in Fig. 5, the CD4081B output sinks the required 1.4 milliamperes at an output voltage typically less than 0.5 volt. The HNIL output-voltage levels, 0.8 volt and 10 volts, enable it to interface directly with the COS/MOS input with good noise immunity.

Table IV—Fanout of CD4049A and CD4050A Buffers to TTL

Buffer Fanout	TTL Family 74	74H	74L	74LS	74S
Minimum	1	1	14	7	1
Typical	3	2	28	14	2

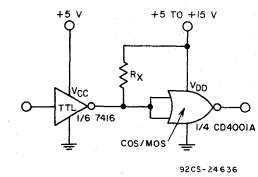


Fig. 4—TTL to COS/MOS at a V_{DD} greater than 5 volts.

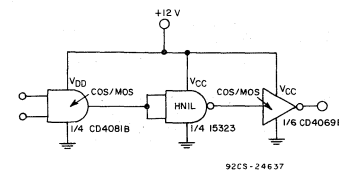


Fig. 5—COS/MOS to HNIL to COS/MOS interface.

COS/MOS to DTL

The COS/MOS to DTL interface requires a buffer, such as the CD4049A shown in Fig. 6, to sink the DTL input current of 1.5 milliamperes at 0.4 volt. Fanout to DTL circuits depends on the sink-current capability of the COS/MOS buffer used. For the CD4049A and CD4050A, typical fanout is 3.

The DTL to COS/MOS interface requires no special consideration because the internal pull-up resistor in DTL circuits and the extremely low input current of COS/MOS circuits ensures a high logic level almost equal to the power-supply voltage.

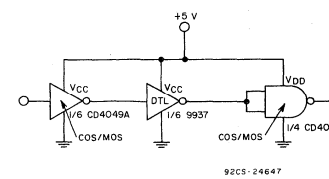


Fig. 6—COS/MOS to DTL to COS/MOS interface.

Table III—Minimum Current-Sinking Capability of COS/MOS Devices

COS/MOS Type	Description	Sink Current (mA at 25°C V_O = 0.4 Volt, V_{DD} = 5 Volt) Ceramic	Plastic
CD4000A	Dual 3-Input NOR Gate Plus Inverter	0.4	0.3
CD4001A	Quad 2-Input NOR Gate	0.4	0.3
CD4002A	Dual 4-Input NOR Gate	0.4	0.3
CD4007A	Dual Complementary Pair Plus Inverter	0.6	0.3
CD4009A/49A	Inverting Hex Buffer	3.0	3.0
CD4010A/50A	Non-Inverting Hex Buffer	3.0	3.0
CD4011A	Quad 2-Input NAND Gate	0.2	0.1
CD4012A	Dual 4-Input NAND Gate	0.1	0.05
CD4041A	Quad True/Complement Buffer	0.4	0.2
CD4031A	64-Stage Static Shift Register	1.3	1.3
CD4048A	Expandable 8-Input Gate	1.6	1.6
CD4XXXB	Any B-Type Device Output	0.4	0.4

COS/MOS to 10k ECL

COS/MOS and 10k ECL are not normally interfaced, but they can be readily by using the 10124 and 10125 devices which are intended for conversion between ECL and TTL. This interface requires that the COS/MOS device be operated at a 5-volt V_{DD}, as shown in Fig. 7. Where greater speed is required of the COS/MOS system, it can be operated with V_{DD} at the ECL ground and V_{SS} at −12 volts. In the latter case, a 1N914 diode clamps the COS/MOS output to V_{EE} as shown in Fig. 8. At supply voltages greater than 6 volts, a COS/MOS buffer should not be used, as over-dissipation will occur in the buffer.

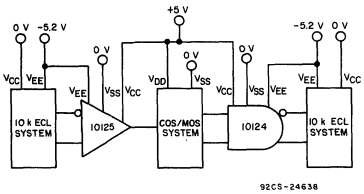


Fig. 7—10k ECL to COS/MOS and COS/MOS to 10k-ECL interface.

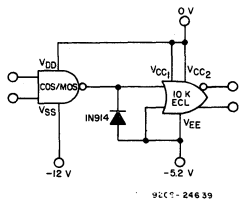


Fig. 8—COS/MOS at 12 volts to 10k-ECL interface.

COS/MOS to NMOS

The increasing use of n-channel MOS memories means that interfaces between COS/MOS and NMOS are now common. In a system of 1k memories, such as the type 2102, which employ peripheral COS/MOS circuitry for address, read/write, chip select and data handling, the COS/MOS circuitry can be supplied from the 5-volt power supply of the memory. Inputs to the memory are then COS/MOS compatible, and direct interface is permitted. The data output requires only a single pull-up resistor, R_X, as shown in Fig. 9, to ensure an acceptable high-state output voltage.

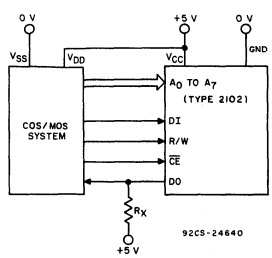


Fig. 9—Direct interface between COS/MOS and a1k memory, type 2102.

A 4k-bit, dynamic, n-channel RAM, such as the 2107A, has +12-volt and −5-volt supplies as well as the +5-volt V_{CC} supply, as shown in Fig. 10. The COS/MOS peripheral circuitry in this system is probably best operated from the +12-volt supply, ensuring good speed characteristics and noise immunity. The 5-volt input signals to the memory are provided by CD4050A buffers powered by the 5-volt V_{CC} supply. The 12-volt-swing chip-enable signal is directly compatible with the 12-volt COS/MOS system. The data output uses a single transistor to generate the required 12-volt logic swing; memories added to provide an increase in word capacity are wire-OR'ed at the data output pin of the memory.

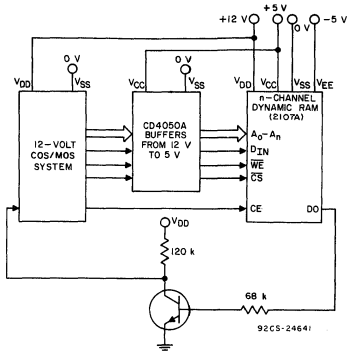


Fig. 10—COS/MOS to n-channel dynamic-RAM interface.

COS/MOS to PMOS

Silicon-gate PMOS static shift registers operating from +5-volt and −12-volt supplies are directly compatible with a COS/MOS system operating from the +5-volt supply with V_{SS} at zero volts. The only additional component required is a clamp diode to V_{SS} on the data output, as shown in Fig. 11, because the unloaded PMOS output voltage will go negative in the low output state.

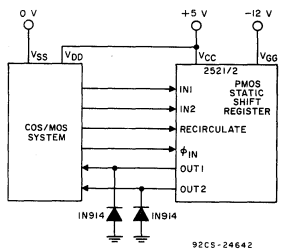


Fig. 11—COS/MOS to PMOS static-shift-register interface.

COS/MOS to Industrial and Power-Control Circuits

Industrial control systems employ greater logic swings than IC logic systems, such as COS/MOS, to achieve high noise immunity and to enable them to operate from readily available high-voltage supplies and to interface with electro-mechanical equipment.

Fig. 12 shows a simple, resistive-divider circuit used to interface a system with a 24-volt logic swing to COS/MOS; the circuit could readily be modified for even higher voltage swings. The capacitor filter enhances the excellent noise immunity of the COS/MOS logic, and the two clamp diodes ensure that the input signal voltage is between V_{DD} and V_{SS}. An alternative circuit using a zener diode is shown in Fig. 13.

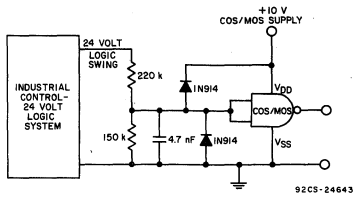


Fig. 12—Industrial control to COS/MOS interface.

A single-transistor level-converter interfaces a COS/MOS device to an industrial control system, as shown in Fig. 14. The transistor is driven directly from the COS/MOS device output (Fig. 23 describes the method of calculating the values of the resistors needed in Fig. 14).

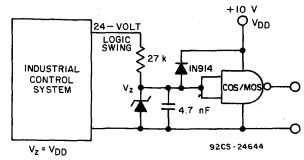


Fig. 13—Zener diode industrial control interface.

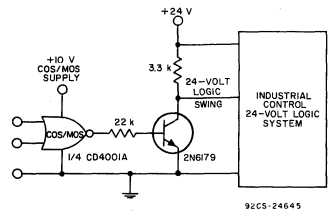


Fig. 14—COS/MOS to industrial-control interface.

The slow pulse edges typically found in an industrial control system can be speeded up in the COS/MOS system by a Schmitt-trigger circuit, the CD4093B, Fig. 15(a). At a V_{DD} of 5 volts, V_H is typically 0.6 volt, Fig. 15(b).

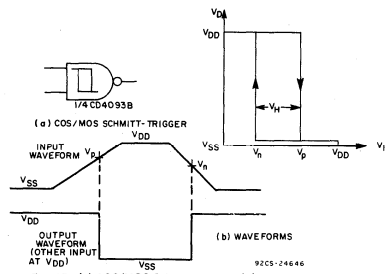


Fig. 15—(a) COS/MOS Schmitt-trigger, (b) typical waveforms for Schmitt-trigger.

A high-power coil, such as the solenoid of a printer hammer, which requires about 1 ampere at 70 volts, may be driven from a COS/MOS system by using a Darlington transistor as shown in Fig. 16. A typical value of V_{BE} for a type 2N6385 transistor is 1.5 volts at a collector current of 1 ampere and a minimum gain of 1000, so that the output source transistor of the CD4073B has to supply 1.5 milli-amperes. The value of resistor R is chosen so that V_{DS} is sufficient to guarantee this output current. Suitable values of R for use with a B-type device are given in Fig. 16 for a V_{DD} of 5, 10, and 15 volts.

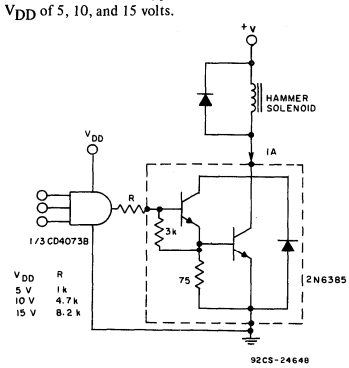


Fig. 16—COS/MOS system driving a printer-hammer solenoid with the aid of a Darlington transistor.

Power-control SCR's and triacs may also be driven directly by COS/MOS outputs. A sensitive-gate SCR, such as the 106B1, may be controlled directly by a COS/MOS gate, such as the CD4069B, and thus be able to control directly 2.5 amperes at reverse voltages up to 600 volts, as shown in Fig. 17.

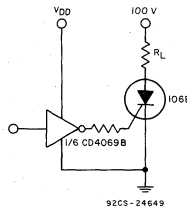


Fig. 17—COS/MOS directly driving a sensitive-gate SCR.

SCR's and triacs with gate currents in the milliampere region may be controlled by a buffer, such as the CD4049A. This buffer could, in turn, be controlled by a COS/MOS system or, as in Fig. 18, by an opto-coupler to provide greater isolation.

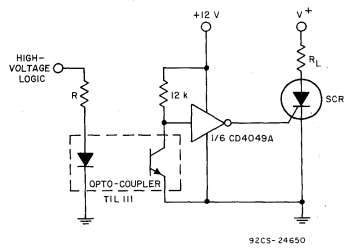


Fig. 18—High-voltage logic to COS/MOS driving an SCR.

In cases where a single-gate output source or sink current proves insufficient, it is possible to parallel the inputs and outputs of gates on the same chip, as in Fig. 19. Gates not on the same chip and buffer circuits should not be operated in parallel as over-dissipation may result.

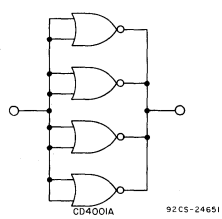


Fig. 19—Paralleling inputs and outputs.

Interfacing Op-Amps to COS/MOS

COS/MOS circuits may be connected directly to the output of an op-amp operating between the normal ±15-volt supply rails, as in Fig. 20, provided clamp diodes to V_{DD} and V_{SS} are used to ensure that the COS/MOS input voltage does not go outside the range V_{SS} to V_{DD}. Resistor R3 limits the op-amp output current should the op-amp output voltage tend toward the negative rail.

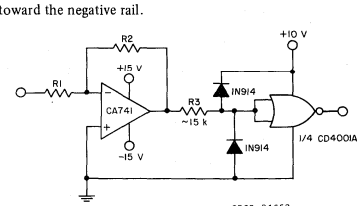


Fig. 20—Split-rail op-amp to COS/MOS interface.

Fig. 21 shows a CA741-type op-amp operated between V_{DD} and V_{SS} with a resistive divider on the non-inverting op-amp input.

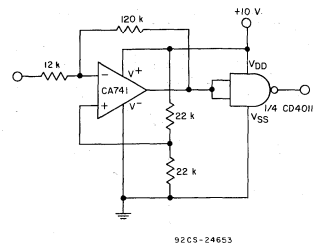


Fig. 21—Interface of op-amp and COS/MOS with common supply rail.

COS/MOS Driving Displays

Digital systems now employ a great variety of digital displays, so that their interface to COS/MOS is a common requirement.

COS/MOS TO LED'S

LED's may be driven directly from a COS/MOS buffer, such as the CD4050A shown in Fig. 22, at a drive current of 15 milliamperes if a power supply of approximately 10 volts is available.

Seven-segment LED displays connected in either common anode or common cathode configurations may be driven at supply voltages as low as +5 volts by the seven-transistor

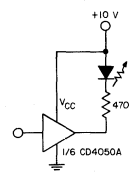


Fig. 22—COS/MOS buffer driving an LED.

arrays CA3081 and CA3082. Fig. 23 shows one of the seven transistors of the CA3081 with an LED load. The figure also shows the method of calculating R_b and R_c. The base drive current available depends on the CD4000A Series device used and the values of V_{DD} and V_{DS}. As shown in Fig. 24, the base drive current increases with both V_{DD} and V_{DS}. Fig. 25 shows one of the seven transistors of the CA3082 driving a common-cathode LED. The method of calculating the value of emitter resistor R_e is also shown in Fig. 25.

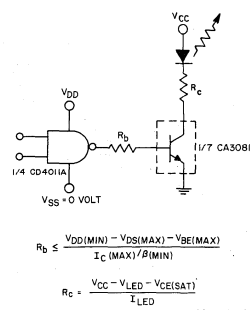


Fig. 23—COS/MOS driving a transistor that has an LED load.

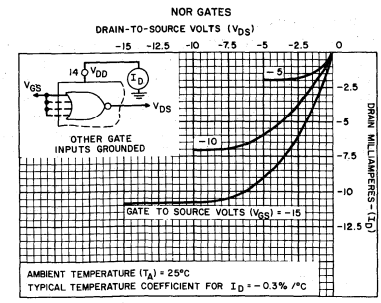


Fig. 24—CD4001A—typical p-channel drain characteristics.

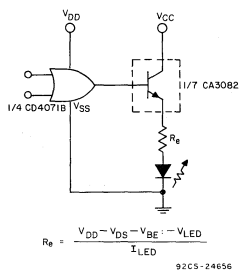


Fig. 25—COS/MOS driving a transistor with a common-cathode-connected LED load.

COS/MOS TO LCD

Seven-segment liquid-crystal displays may be driven directly by COS/MOS circuits CD4054A, CD4055A or CD4056A, as shown in Fig. 26. These circuits contain the internal level-shifting circuitry needed to convert the typically 5-volt input logic-level swing to the 30-volt peak ac signal required to drive the dynamic-scattering LCD.

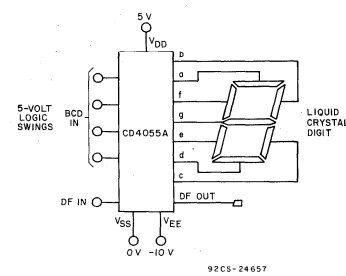


Fig. 26—Using the CD4055A to drive a liquid crystal.

COS/MOS TO GAS-DISCHARGE DISPLAY

The popular seven-segment gas-discharge display requires a cathode drive current that varies from segment to segment. Manufacturers supply drivers which are COS/MOS compatible at their inputs so that they can interface a COS/MOS system to the gas-discharge display without additional circuitry.

REFERENCE

1. "COS/MOS Digital Integrated Circuits", RCA DATABOOK Series SSD-203B, 1975.

Applications of the RCA-CD4093B COS/MOS Schmitt Trigger

by D. J. Blandford

This Note describes the characteristics and some typical applications of the CD4093B COS/MOS quad two-input NAND Schmitt Trigger. The CD4093B may be used in all applications in which the logical NAND function is required and, in addition, in a whole range of timing, waveshaping, and interfacing applications in which the Schmitt Trigger action on the inputs is utilized.

CHARACTERISTICS

The CD4093B consists of four Schmitt triggers in a fourteen-pin package. Each of the four devices is a two-input NAND gate with Schmitt action on each input, yielding a typical hysteresis voltage of 2.0 volts with a 10-volt supply without the need for any external components. In addition, the CD4093B is compatible, pin for pin, with the popular CD4011A quad NAND gate, has the balanced and standardized output drive of the 18-volt COS/MOS "B" series types, and has low propagation delay and very low power dissipation. Table I summarizes these characteristics.

If now the input voltage is reduced, the output stays low (V_{SS}) until Vn is reached. At this point the output goes high (V_{DD}) and remains high as the input voltage is reduced to zero (V_{SS}). The hysteresis voltage is the difference between V_p and Vn and is typically 0.6 volt for a 5-volt V_{DD} and 2.0 volts for a 10-volt V_{DD}.

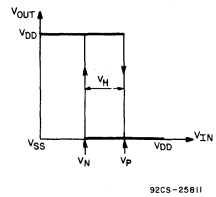


Fig.2 – Transfer characteristic of the CD4093B.

TABLE I

Static and Dynamic Electrical Characteristics at 25°C

CHARACTERISTIC	SYMBOL	V_O VOLTS	V_{DD} VOLTS	TYPICAL VALUES	UNITS
QUIESCENT DEVICE CURRENT	I_L		5	0.001	μA
			10	0.001	μA
OUTPUT VOLTAGE LOW LEVEL	V_{OL}		5	0	V
			10	0	V
HIGH LEVEL	V_{OH}		5	5	V
			10	10	V
NOISE IMMUNITY	V_{NL}	5	5	2.6	V
		10	10	5.2	V
	V_{NH}	0	5	3.0	V
		0	10	6.5	V
OUTPUT DRIVE CURRENT SINK	I_{DN}	0.4	5	0.8	mA
		0.5	10	1.8	mA
SOURCE	I_{DP}	4.6	5	−0.8	mA
		2.5	5	−1.8	mA
		9.5	10	−1.8	mA
POSITIVE THRESHOLD VOLTAGE	V_p		5	2.6	V
			10	5.2	V
NEGATIVE THRESHOLD VOLTAGE	V_n		5	2.0	V
			10	3.5	V
HYSTERESIS VOLTAGE	V_h		5	0.6	V
			10	1.7	V
PROPAGATION DELAY TIME	t_{PHL},		5	190	ns
C_L = 50 pF	t_{PLH}		10	100	ns
TRANSITION TIME	t_{TLH},		5	100	ns
C_L = 50 pF	t_{THL}		10	50	ns

Fig.1 shows the functional diagram of the Schmitt trigger; note that each input has the standard COS/MOS input protection network and that each output is double buffered.

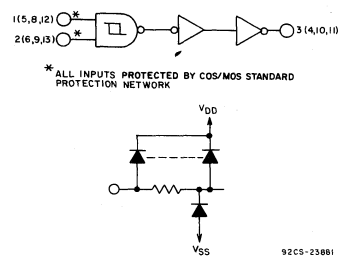


Fig.1 – Functional diagram of the CD4093B, COS/MOS Schmitt trigger. One of four Schmitt triggers is shown.

Fig.2 shows the transfer characteristic of the Schmitt trigger. The general shape of this characteristic is the same for all values of V_{DD}, but the relative values of V_p, Vn and V_H change with V_{DD} as shown in the data sheet. As the input voltage is increased from zero (V_{SS}), the output remains high (V_{DD}) until V_p is reached. At this point the output goes low. (V_{SS}) and remains low as the input voltage is raised to V_{DD}.

Fig.3 shows a graph of the typical hysteresis voltage V_H as a function of supply voltage V_{DD}.

Fig.4 shows the input/output characteristics of the CD-4093B; the output characteristic shown is the same for any COS/MOS output, including the Schmitt trigger. The input characteristic is unique to the Schmitt trigger and shows that, when driven by another COS/MOS device, the Schmitt trigger has more than 50-percent noise immunity in each state.

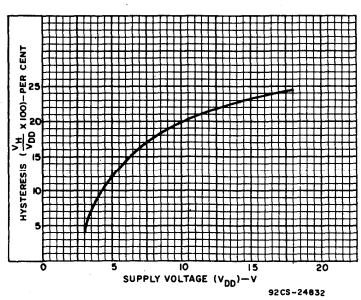


Fig.3 – Typical percent hysteresis vs supply voltage.

Figs.5 and 6 show measurements of voltage and energy noise immunity for the Schmitt trigger. Fig.5 shows, for example, that for a V_{DD} of 5 volts, the noise immunity in each

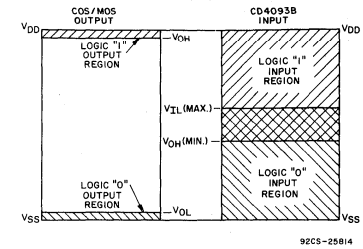


Fig.4 – Input and output characteristics.

state exceeds the supply voltage (5 volts) for pulses shorter than 200 nanoseconds. The energy noise immunity plotted in Fig.6 against pulse width is the product of noise-pulse voltage, noise-pulse time, and the appropriate value of the output drive current for the device under test. The units of energy are nanojoules (10^{-9} Joule). At each value of the supply voltage the curve has a minimum value. Inspection of Fig.6 shows that the value of the minimum energy noise immunity increases with increasing V_{DD}, and occurs at a lower value of noise-pulse width.

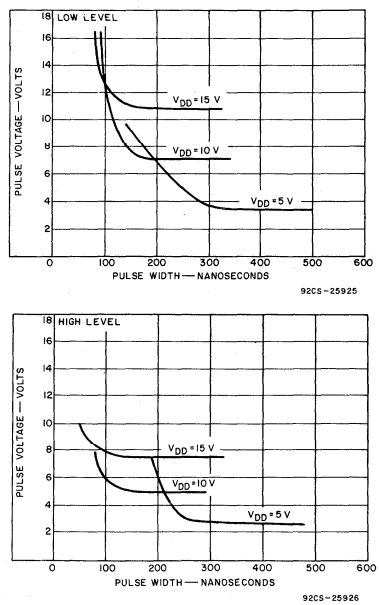
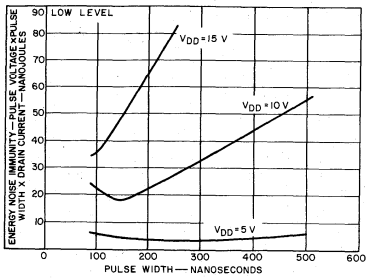


Fig.5 – Voltage noise immunity of the CD4093B.

Another important property of the Schmitt trigger is illustrated in Fig.7, which compares the supply current taken by the CD4093B with that of the CD4011A, with a long rise- and fall-time input. The power dissipated by the Schmitt trigger is clearly much less than that dissipated by the quad NAND gate, so that the Schmitt trigger should be used in applications in which slow input edges are anticipated.

APPLICATIONS

The application of the CD4093B COS/MOS Schmitt trigger in situations which require the logical NAND function and in timing, waveshaping, and interfacing applications in which the Schmitt trigger action on the inputs is utilized are discussed below.



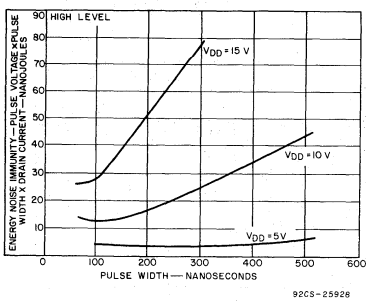
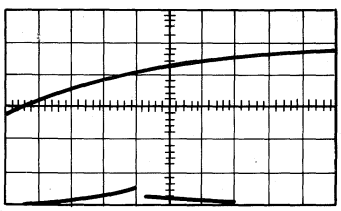
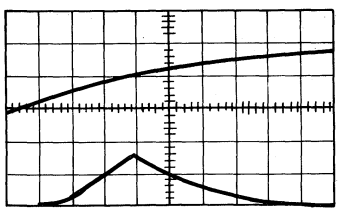


Fig.6 – Energy noise immunity of the CD4093B.



(a) CD4093BE:
Top vertical – 5V/Division
Lower vertical – 2mA/Division
Horizontal – 0.2/Division



(b) CD4011AE:
Top vertical – 5V/Division
Lower vertical – 2mA/Division
Horizontal – 200ms/Division

92CS-26636

Fig.7 – Power consumption with slow input edge; a comparison of the CD4093B with the CD4011A.

Waveshaping

Sine Wave to Square-Wave Converter – Fig.8 shows a typical application of the Schmitt trigger, the sine-wave to square-wave converter. The sine input is ac coupled by capacitor C; R_1 and R_2 bias the input midway between Vn and V_p, the input threshold voltages, to provide a square wave at the output.

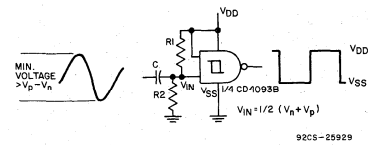
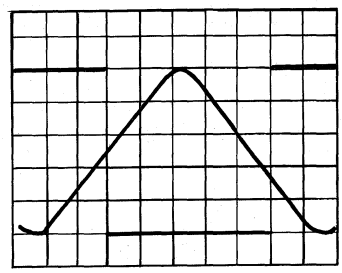


Fig.8 – Sine-wave to square-wave converter.

Slow Edges – Slow edges are a common phenomenon in digital systems; for example, at the output from a transducer, at the end of a long line, or an output with large capacitive load, or on the output of a filter. The Schmitt trigger is particularly useful in generating a waveform with fast edges in these applications, see Fig.9.



CD4093BE:
2V/Division
2ms/Division

92CS-26635

Fig.9 – Sharpening up a slow edge.

With an input edge time of 1 second and an output transition time of 100 nanoseconds, the improvement in edge time is a factor of 10^7. With longer input edge times the improvement is even greater.

Timing – In general, timing circuits use external resistors and capacitors to provide time constants. The advantage of the CD4093B COS/MOS Schmitt trigger in these applications is that the very high input impedance permits the designer to use high values of timing resistance. Therefore, long delay times may be produced with moderate values of capacitance, and small, low-cost capacitors may be used for short and medium time delays.

Edge Delays – In the circuit of Fig.10, the output falling edge is delayed with respect to the input leading edge by a time td_+ given by:

$$td_+ = RC \ln \frac{V_{DD}}{V_{DD} - V_p}$$

When the input goes high (V_{DD}) the capacitor charges up towards V_{DD} through R. When input B reaches V_p, the output goes low (V_{SS}). As soon as input A goes low, the output goes high.

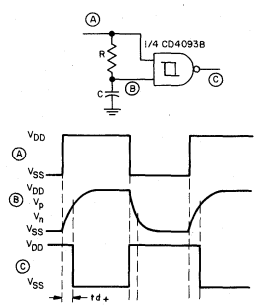


Fig.10 – Delay on leading edge.

By connecting one input to V_{DD}, as in Fig.11, both edges are delayed, because now, when input A goes low, output C remains low until capacitor C discharges to Vn. At this time, the output goes high. td_- is given by:

$$td_- = RC \ln \frac{V_{DD}}{Vn}$$

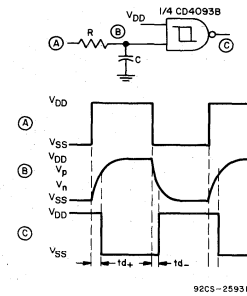


Fig.11 – Delayed pulse.

Both edges may be separately delayed by connecting different RC timing components to each input, as in Fig.12. Now td_+ and td_- are given by:

$$td_+ = R_2C_2 \ln \frac{V_{DD}}{V_{DD} - V_p}$$

$$td_- = R_1C_1 \ln \frac{V_{DD}}{Vn}$$

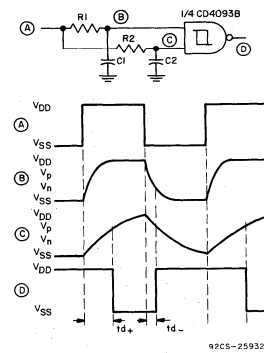


Fig.12 – Separate delay to each edge.

Edge Detector – Fig.13 shows a circuit that provides a short negative-going output pulse for every positive-going edge at the input. The input waveform is coupled to the input by capacitor C; the pulse length depends, as before, on R and C. If a negative going edge detector is required, the circuit of Fig.14 should be used.

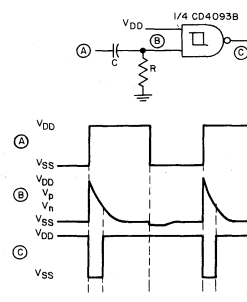


Fig.13 – Rising-edge detector.

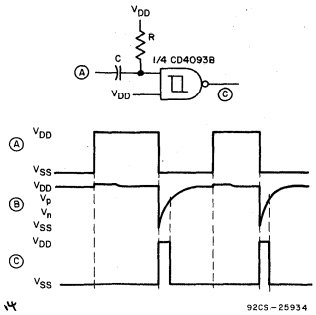


Fig.14 – Falling-edge detector.

Power-On Reset

A reset pulse is often required at power-on in a digital logic system. This type of reset pulse is ideally provided by the circuit of Fig.15(a). Because of the high input impedance of the Schmitt trigger, long reset pulse times may be achieved without the excess dissipation that results when both output devices are on simultaneously, as in an ordinary gate device, Fig.15(b).

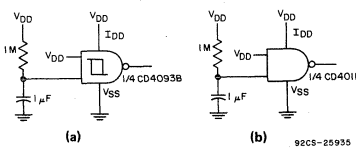


Fig.15 – Reset circuit; a comparison of the CD4093B with the CD4011A.

Astable Oscillators

A range of astable oscillators may be easily constructed by using the CD4093B. Fig.16 shows the basic circuit and its associated waveforms. Before power is applied, input and output are at ground potential and capacitor C is discharged. On power-on, the output goes high (V_{DD}) and C charges through R until Vp is reached; the output then goes low (V_{SS}). C is now discharged through R until Vn is reached. The output then goes high and charges C towards Vp through R. Thus input A alternately swings between Vp and Vn as the output goes high and low. One important advantage of this circuit is that the oscillator is self-starting at power-on.

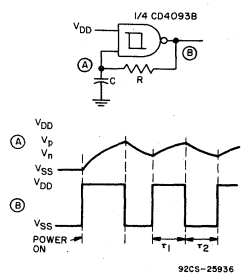


Fig.16 – Astable multivibrator.

The oscillator period is given by:

$$\tau = \tau_1 + \tau_2$$

where

$$\tau_1 = RC \ln \frac{V_{DD} - Vn}{V_{DD} - Vp}$$

and

$$\tau_2 = RC \ln \frac{Vp}{Vn}$$

In general $\tau_1 \neq \tau_2$, so that to get a 1:1 mark-to-space ratio the circuit of Fig.17(a) should be used. When the output is low in the circuit of Fig.17, C is discharged through R_1 in parallel with R_2, which shortens τ_2. If R_2 is much smaller than R_1, short, negative-going pulses are produced, as in Fig.17(b).

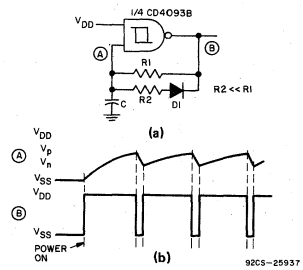


Fig.17 – Astable oscillator with controlled mark-to-space ratio.

In the circuit of Fig.18 the oscillator is gated by signal C on the second input of the CD4093B. The oscillator output is high while the gating signal is low; the oscillator then oscillates with the period τ, given above, while the gating signal is high.

Interfacing

The noise immunity of the COS/MOS NAND Schmitt trigger is very high, typically greater than 50 percent of V_{DD} in each state, as shown in Fig.4. Therefore, it is ideally suited to circuitry that requires a very high noise immunity. Because of the hysteresis built into the Schmitt trigger, it can tolerate noise on a slow input edge without false switching at the output, as shown in Fig.19. This noise performance permits the construction of an ideal interface from an industrial environment to a COS/MOS logic system, as shown in Fig.20. The CD4093B will function correctly under the most severe conditions of input overvoltage and in spite of noise spikes of up to hundreds of volts. The input is kept between V_{SS} and V_{DD} by D_1 and D_2 with R_1, typically 220 kilohms, as a current-limiting resistor. Resistor R_2 ties the logic input to V_{SS} should the interface input be open-circuited by the removal of a PC board from a system, for example. Capacitor C_1, with R_1, acts as a filter and enhances the noise-rejection properties of the interface.

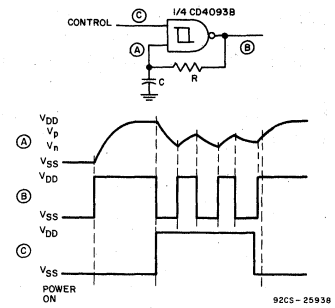


Fig.18 – Gated astable oscillator.

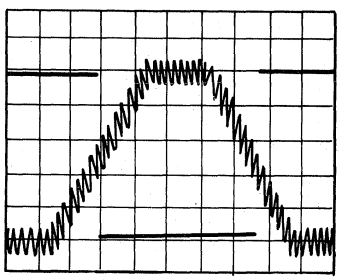


Fig.19 – Rejection of noise on slow input edge.

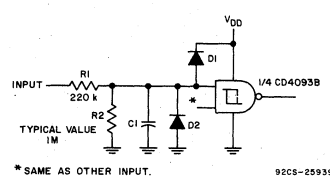


Fig.20 – Industrial-environment to COS/MOS interface.

Guide to Better Handling and Operation of CMOS Integrated Circuits

by J. Flood and H. L. Pujol

This Note recommends specific handling and operating practices that minimize the probability of damage to CMOS integrated circuits in the manufacturing operation and the field environment.

A description of various gate-oxide networks that protect against electrostatic discharge in both A-series and B-series RCA COS/MOS product is provided. A practical explanation of the SCR latch-up mechanism and its associated failure mode is given. In addition, operating procedures that help prevent device malfunction are described.

HANDLING CONSIDERATIONS

All CMOS devices are susceptible to damage by the discharge of electrostatic energy between any two pins. The gate input is equivalent to a small, low-leakage capacitor (5 picofarads typical) in parallel with a very high resistance (10^{12} ohms typical). This extremely high input impedance lends itself readily to the buildup of electrostatic charges. Therefore, because the gate-oxide breakdown of a CMOS device is typically 80 volts, damage by high levels of electrostatic discharge can occur.

To protect the gate oxide against high levels of electrostatic discharge, protective networks are implemented on all RCA CMOS (COS/MOS) devices, as described below.

Standard Protection Networks

Fig. 1 shows the standard protection network incorporated on all A-series devices

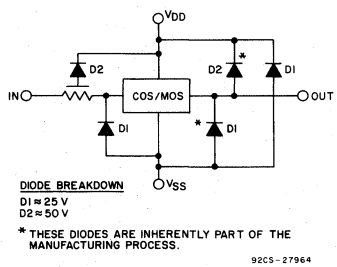


Fig.1 – Standard protection network.

and some B-series devices. Input-diode D_2 is a distributed resistor-diode network that appears as two diodes to V_{DD}.

Improved Protection Network

Fig. 2 shows the improved protection network incorporated on all new B-series devices as well as on all A-series, B-converted types.

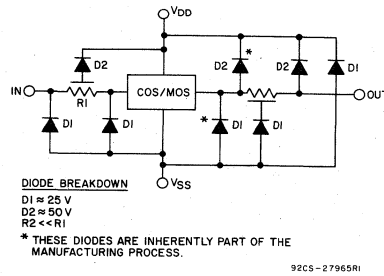


Fig.2 – Improved protection network.

Other Protective Networks

Fig. 3 shows the modified protective network for a CD4049/4050 buffer. The input diode to V_{DD} is not incorporated so that the level-shifting function can occur.

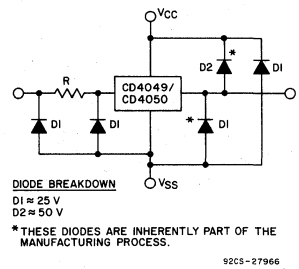


Fig.3 – Modified protection network.

Fig. 4 shows a transmission gate with the intrinsic diodes that protect against electrostatic discharge.

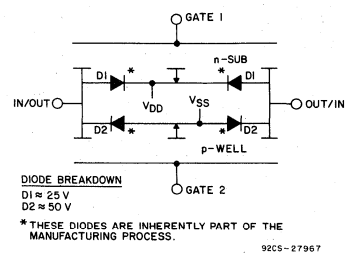


Fig.4 – Transmission gate with intrinsic diodes that protect against electrostatic discharge.

The protection networks described in this Note were characterized by using the equivalent body discharge network of Fig. 5. There are 12 possible combinations by which a device can be damaged. A discussion of the combinations is beyond the scope of this Note; however, Table I shows worst-case protection levels for the above networks.

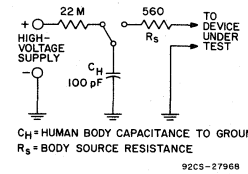


Fig.5 – Equivalent-body discharge network.

Additional protection can be obtained by adding external series resistors at device inputs. The value of this resistance should be 10 kilohms for gate inputs and 1 kilohm for transmission gate inputs, where applicable. In addition, zener diodes at the output pins can clamp the voltage at a safe level. The zener value should not exceed the absolute maximum rating of the part.

On-chip protection networks are not used on transmission gates to maintain low on resistance. The 800-volt worst case capability is provided by the intrinsic diodes shown in Fig. 4.

TABLE I – Worst-Case Capability of Protective Networks

Protective Network	Worst-Case Capability
Standard (inc. CD4049, CD4050)	1 kV to 2 kV
Improved	4 kV
Transmission Gate	< 800 V

General Handling Rules

Table I indicates the typical, worst-case voltage levels that the above networks can withstand. Because every manufacturing environment is different, levels above those shown in Table I should be anticipated and protected against by following the handling recommendations of Table II.

Basic protection starts with personnel and materials all at the same or ground potential.

Dry weather (relative humidity less than 30 percent) tends to multiply the accumulation of static charges on any surface. Conversely, higher humidity levels (40 to 50 percent) tend to reduce the magnitude of the static voltage generated. In a low-humidity environment, the handling precautions listed above take on added importance and should be adhered to without exception.

HANDLING OF UNMOUNTED CHIPS

In handling unmounted chips, differences in voltage potential should be avoided. A conductive carrier or a carrier having a conductive overlay should be used. Another important consideration is the sequence in which bonds are made; the V_{DD} (device supply) connection should always be made before the V_{SS} (ground) bond.

HANDLING OF SUBASSEMBLY BOARDS

After COS/MOS units have been mounted on circuit boards, proper handling precau-

TABLE II – General Handling Recommendations

	Should be conductive	Should be grounded to common point
Handling equipment	X	
Metal Parts of Fixtures and Tools		X
Handling Trays	X	
Soldering Irons		X
Table Tops	X	X
Transport Carts	X	
Manufacturing Operating Personnel		Utilize grounded, metal or conductive plastic wrist straps with 1-megohm series resistor
General Handling of Devices		Utilize grounded, metal or conductive plastic wrist straps with 1-megohm series resistor

tions should still be observed. Until these subassemblies are inserted into a complete system in which the proper voltages are applied, the board is no more than an extension of the leads of the device mounted on the board.

It is good practice to put conductive clips or conductive tape on the circuit-board terminals. This precaution prevents static charges from being transmitted through the board wiring to the devices mounted on it.

AUTOMATIC HANDLING EQUIPMENT

When automatic handling equipment is used, it may not always be possible to eliminate static electricity through grounding techniques alone. Automatic feed mechanisms must be insulated from the devices under test at the point where the devices are connected to the test set. The anvil transport portion of the automatic handling mechanism can generate very high levels of static electricity as a result of the continuous flow of devices over and then separating from the anvil. Total control of these static voltages is critical because of the high throughputs associated with automatic handling.

Fortunately, the resolution of this problem is simple, practical, and inexpensive. Ionized-air blowers, which supply large volumes of ionized air to objects that are to be charge neutralized, are commercially available from many supply sources. Field experience with ionized-air techniques reveals this method to be extremely effective in eliminating static electricity when grounding techniques cannot be used.

Failure Mechanisms

Electrical damage resulting from handling is usually caused by either of the two following failure mechanisms:

1. Low-level static electricity (voltage of 1 kV to 4 kV). Input diode protection may be overstressed and input leakage currents as high as 1 milliampere across diodes may cause a malfunction.
2. High-level static electricity (voltages greater than 4 kV). Gate oxides may become short-circuited. Inputs to V_{DD} or V_{SS} terminals will be low-impedance inputs.

The presence of these types of device malfunction can be detected by curve-tracer checks of the input protection diodes described above. Diode degradation resulting from static electricity is observable in the low-reverse-breakdown characteristics shown on the curve tracer. On the other hand, damage resulting from high levels of static electricity are observed as a resistive short to V_{DD} or V_{SS}.

Typical Manufacturing Area Procedure

The example below illustrates all of the above recommendations for handling CMOS devices in a typical manufacturing environment. Although existing protective networks offer a high level of protection against electrostatic discharge, this example emphasizes specific precautions that can help eliminate damage.

Receiving Area

Devices should not be removed from their conductive or antistatic carriers. If devices are not received in conductive or antistatic packing material, they should be returned to the supplier.

Incoming Inspection

Physical – Parts should be counted without removing them from their containers.

Storage – Devices should remain in carriers. Even a partial removal of IC's from a carrier should only be done by a grounded operator. Devices removed should be placed in a conductive tray.

Electrical – All testing should be performed by a grounded operator. Devices should be reinserted in conductive carriers after completion of a test.

PC Board Assembly

It is desirable that PC boards have shorting bars installed prior to assembly (soldering). Where possible, CMOS IC's should be the last component installed on the PC board.

Boards should be transported to the wave-solder area in conductive carriers. Flux removal should be done with an acceptable solvent. Examples of specific, acceptable alcohols are isopropanol, methanol and special denatured alcohols such as SDAI, SDA30, SDA34 and SDA44. The removal of flux from non-hermetic and molded-plastic devices by means of soap and water in a dishwasher is NOT recommended as this procedure will adversely affect the long-term life of the device.

OPERATING CONSIDERATIONS

Proper operating procedures are as important as proper handling techniques. A review of RCA COS/MOS A-series and B-series operating characteristics and ratings is given in Table III.

Operating Voltage

When devices are operated near the maximum supply-voltage range, power-supply turn-on or turn-off transients, power-supply ripple or regulation, and ground noise should be suppressed; any of the above conditions must not cause ($V_{DD} - V_{SS}$) to exceed the absolute maximum rating. A good practice is to use a zener protection diode in parallel with the power bus. The zener value should be above the expected maximum regulation excursion, but should not exceed the maximum supply voltage. Fig. 6 illustrates a practical zener shunt circuit. A current-limiting resistor is included if the supply-current compliance is higher than the zener power-dissipation rating for a given zener voltage. The shunt capacitor value is chosen to supply required peak-current switching transients.

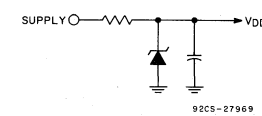


Fig.6 – Zener-diode short circuit.

Unused Inputs

All unused input leads must be connected to either V_{SS} or V_{DD}, whichever is appropriate for the logic circuit involved. A floating input on a high-current type (such as the CD4009A, CD4010A, CD4041A, CD4049A, CD4050A) can result not only in faulty logic operation, but can cause the maximum power dissipation of 500 milliwatts to be exceeded; the result may be damage to the device. Another consideration with high-current devices is the need for a pull-up resistor between the inputs and V_{SS} or V_{DD} should there be any possibility that the device terminals may become temporarily open or unconnected (e.g., if the printed circuit board driving the high-current types is removed from the chassis). A useful range of values for such resistors is from 0.2 to 1 megohm.

Input Signals

Signals should not be applied to the inputs while the device power supply is off unless the input current is limited to a steady-state value of typically less than 10 milliamperes. Input-signal interfaces that are the allowable 0.5 volt above V_{DD} or below V_{SS} should be current-limited to typically 10 milliamperes or less.

Whenever the possibility of exceeding 10 milliamperes of input current exists,

TABLE III – Maximum Ratings of RCA COS/MOS Devices (Voltages referenced to V_{SS})

DC Supply Voltage Range	3 to 15 V (A Series); 3 to 20 V (B Series)
Recommended Operating Voltage	3 to 12 V (A Series); 3 to 18 V (B Series)
DC Input Voltage Range	−0.5 to V_{DD} + 0.5 V
Dissipation per Package	500 mW
Device Dissipation per Output Transistor	100 mW
Storage Temperature Range	−65 to +150°C
Operating Temperature Range	
Ceramic Package Types	−55 to +125°C
Plastic Package Types	−40 to +85°C
Lead Temperature (during soldering) at a distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+ 265°C

a resistor in series with the input is recommended. The value of this resistor can be as high as 10 kilohms without affecting static electrical characteristics. However, speed will be reduced because of the added RC delay. Particular attention should be given to long input-signal lines where high inductance can increase the likelihood of large-signal pickup in noisy environments. In these cases, series resistance with shunt capacitance at the IC input terminals is recommended. The shunt capacitance should be made as large as possible consistent with the system speed requirements.

Fan-Out – COS/MOS to COS/MOS

All RCA COS/MOS devices have a dc fan-out capability of greater than 50. The reduction in COS/MOS switching speed caused by added capacitive loading should, however, be consistent with high-speed system design. The input capacitance is typically 5 picofarads for most types; the CD4009 and CD4049 buffers have a typical input capacitance of 15 picofarads.

Maximum Clock Rise and Fall Time

All COS/MOS clocked devices show maximum clock rise- and fall-time ratings (normally 5 to 15 microseconds). With longer rise or fall times, a device may not function properly.

Parallel Clocking

When two or more different CMOS devices use a common clock, the clock rise time must be kept at a value less than the sum of the propagation delay time, the output transition time, and the setup time. Most flip-flop and shift-register types are included in this rule and are so noted in the individual data sheets.

Output Short Circuits

Shorting of outputs to V_{SS} or V_{DD} can cause the device power dissipation to exceed the safe value of 500 milliwatts. In general, outputs of these types can all be safely shorted when the device is operated with $(V_{DD} - V_{SS}) \geq 5$ volts, but the 500 milliwatt dissipation ratings may be exceeded at higher power-supply voltages. For cases in which a short-circuited load, such as the base of a p-n-p or n-p-n bipolar transistor, is directly driven, the device output characteristics given in the published data should be consulted to determine the requirements for safe operation below 500 milliwatts. Note that a single output transistor short must be limited to 100 milliwatts.

SCR Latch-Up

Operation above maximum ratings can force CMOS devices into a p-n-p-n SCR "latch-up" mechanism, which can be destructive. Any transients should be avoided and any large loads occurring during operation near the maximum rating should be avoided.

"Latch-up" is considered to be the creation of a low-resistance path between the power supply and ground on a circuit during an electrical pulse; the path remains a low-resistance path after the pulse. In CMOS circuits, several parasitic bipolar transistors exist, as shown in Fig. 7. The p-n-p transistor is a wide-base lateral structure whose β, normally less than 0.2, is a function of device geometry. The conditions for SCR turn-on are as follows:

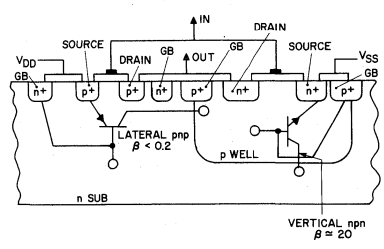


Fig.7 – Parasitic bipolar transistors in CMOS circuits.

1. β n-p-n x β p-n-p ≥ 1
   (vert.) (lat.)
2. The lateral p-n-p and vertical n-p-n base emitter junctions are forward biased.
3. The bias circuit that applies power to V_{DD} and to the input must be capable of supplying current equal to the holding current of potential SCR's.

Fig. 8 shows the equivalent circuit for the SCR structure present in CMOS circuits.

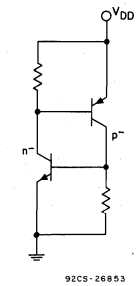


Fig.8 – Equivalent circuit for the SCR structure present in CMOS circuits.

Fig. 9 shows a curve of I_{DD} as a function of V_{DD}, which illustrates the effect of secondary breakdown and SCR latch-up.

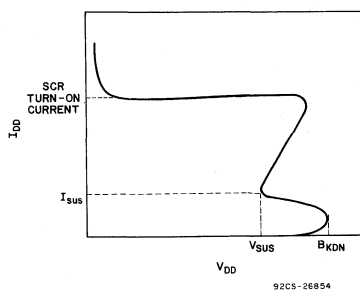


Fig.9 – Curve illustrating effect of secondary breakdown and SCR latch-up.

Table IV shows typical values of breakdown voltage and sustaining voltage and current for RCA COS/MOS A-series and and B-series devices. The table shows that B-series devices are much harder to latch than A-series types because of the higher breakdown voltage.

TABLE IV – Breakdown Voltage and Sustaining Voltage and Current Values

Characteristic	A-Series	B-Series
$V_{BKDN_{min}}$	17 V	25 V
V_{sus}	15 V	22 V
I_{sus}	Type-Dependent 2–40 mA	50–100 mA

Fundamentals of Testing COS/MOS Integrated Circuits

by J. Flood

This Note describes the techniques employed in testing RCA COS/MOS devices to assure their adherence to data-sheet specifications, and provides information useful in data-sheet interpretation and in the inspection of incoming devices. RCA COS/MOS devices are available in two basic families: A-series (3- to 15-volt product) and B-series (3- to 20-volt product).

RCA COS/MOS circuits are 100-percent tested by circuit probe in the wafer stage and are 100-percent tested again after they have been packaged. DC tests of RCA devices are performed at 5, 10, 15, and 20 volts; functionality is checked at 3, 17, and 22 volts depending on family (i.e., A or B series). Sample testing is used to assure adherence to quality requirements and ac specifications.

Static tests, high-speed functional and dc parametric tests, are performed at wafer and package stages by means of a Teradyne J283 test set. A Teradyne S157CM test set and a Macrodata MD154 test set are used in dynamic testing. Dynamic tests are performed with 15 and 50 picofarad loads. Testing at 15 picofarads is accomplished primarily by laboratory "bench-test" techniques; automatic testing at 15 picofarads is difficult because of the high input capacitance (approximately 20 to 35 picofarads) of most automatic ac test sets.

Users should follow the sequence below when testing COS/MOS devices:

1. Insert the device into the test socket.
2. Apply V_{DD}.
3. Apply the input signal.
4. Perform the test.
5. On completion of test, remove the input signal.
6. Turn off the power supply (V_{DD}).
7. Remove the device from the test socket and insert it into a conductive carrier. COS/MOS devices under test must not be exposed to electrostatic discharge or forward biasing of the intrinsic protective diodes shown in Fig. 1.

For detailed COS/MOS IC handling and operating considerations, refer to RCA Application Note, Guide to Better Handling and Operating of CMOS Integrated Circuits.[1]

STATIC TESTING

DC-Parameter Testing

DC parameters are those specified for steady-state conditions; dc testing of RCA devices is done at 5, 10, 15, and 20 volts depending on the family under test. Non-varying forcing conditions are applied to the inputs and/or outputs of a package while the device terminals are monitored for expected voltage or current levels.

DC-parameter tests include:

- Functional tests
- Contact tests (diode measurement)
- Leakage tests: quiescent and input
- Breakdown voltage tests
- Output voltage levels

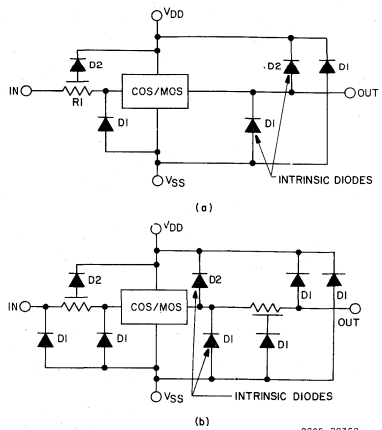


Fig. 1 – (a) Standard protection network used on all CD4000A- and some CD4000B-series devices; (b) improved protection network used on all new RCA COS/MOS devices. Diode breakdown: D1 = 25 V, D2 = 50 V, R2 << R1.

- Input voltage test (includes noise-immunity and noise-margin tests)
- Output drive-current measurements
- Diode tests
- Input-capacitance measurements
- Additional tests as required

A typical CMOS IC test sequence is shown in Fig. 2.

Functional Tests

Functional tests assure that the device under test will perform its logical operations in accordance with its truth table. The operating voltages for functional tests are shown in Table I. Operation is checked

Table I – Operating Voltage Limits For Functional Tests

	Recommended	Min.	Max.
4000A Series	3 - 12	3	15
4000B Series	3 - 18	3	20

against truth table values by monitoring output-voltage levels for valid logic-high and logic-low levels. Output logic levels for functional tests are:

Logic 0: $\leq V_{SS} + 0.5$ V

Logic 1: $\geq V_{DD} - 0.5$ V, V_{DD} is referenced to V_{SS}.

Fig. 3 shows an example of a CD4001 NOR gate functional test. V_{DD} is selected to cover the desired range of operation. This test is performed at a relatively low frequency ($<<f_{CL}$ max.) and with no load other than stray and probe capacitances.

When complex circuits such as the CD4094B, Fig. 4, are tested, input signals must

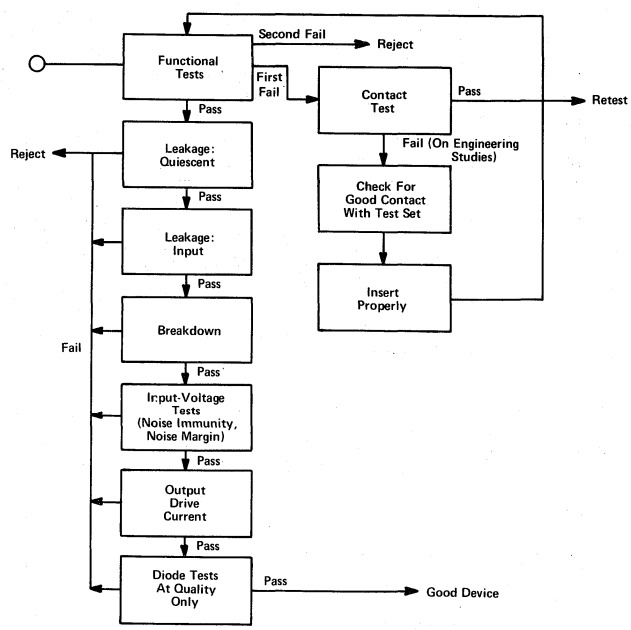


Fig. 2 – A typical COS/MOS IC test sequence.

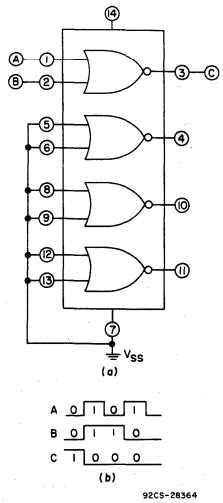


Fig. 3 – Example of CD4001 NOR-gate functional test.

be applied to control the functions being examined. The CD4094B is an 8-stage shift and store register whose eight stages are composed of D-type flip-flops connected in sequential logic form with a common clock. In addition to the flip-flop chain, the device has a latch option at each parallel output stage; the latch is controlled by the strobe input level. The parallel outputs are three-state and are controlled by the output enable level. Data stored in the register is available at the serial outputs on both the positive and negative clock transitions.

Prior to performance of the static or dc parameter tests, which reflect the data-sheet specifications, all register functions must perform 100 percent. Compliance of a device with functional test requirements is determined by monitoring all outputs for proper operation. Functional testing is performed by applying the waveforms shown in the timing diagram of Fig. 5 to the device under test, in this case the CD4094B of Fig. 4. The tests are performed at a frequency well below the maximum operating frequency of the device. Input logic 1 levels are equal to V_{DD}; input logic 0 levels are equal to V_{SS}. Again, output logic 1 and 0 levels are equal to $V_{DD} - 0.5$ V min. and V_{SS} + 0.5 V max., respectively. Functional tests for B-series devices are performed at a $V_{DD} - V_{SS}$ of 22 volts, 2.8 volts, and at intermediate levels depending on the device type.

The timing diagram, Fig. 5, shows 0-level data being clocked into the internal Q output of the shift register while the strobe input is maintained low. After eight positive clock transitions, all the internal Q outputs are at logic 0. Prior to the next positive clock transition, the strobe goes to a 1 state; this condition shifts the zeroes from the internal Q outputs to the external Q outputs and the serial outputs. At this time all outputs are at logic 0. The following clock pulses, those starting at time slot 1, begin shifting 1's and 0's to the parallel outputs. The alternate 1's and 0's are fed into the register up to the negative transition at time-slot 8. At this time the strobe input is sent low to check functionality of the latch. Note that a 0 data bit was transmitted to the Q1 output on the positive clock transition at time-slot 8; however, a positive transition at time-slot 9 does not shift the positive data input to the Q1 output. The Q1 output remains latched low because of the low level at the strobe input. When the strobe goes high, the 1 data bit is transmitted to the Q1 output. At this point the latch functionality plus the functions of the strobe, clock, data inputs, Q_S outputs, and Q outputs, Fig. 4, are fully tested, as shown by the timing diagram.

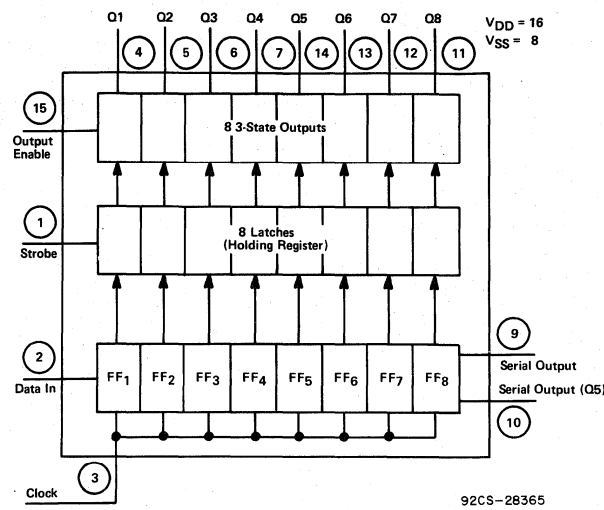


Fig. 4 – Functional diagram of the CD4094B.

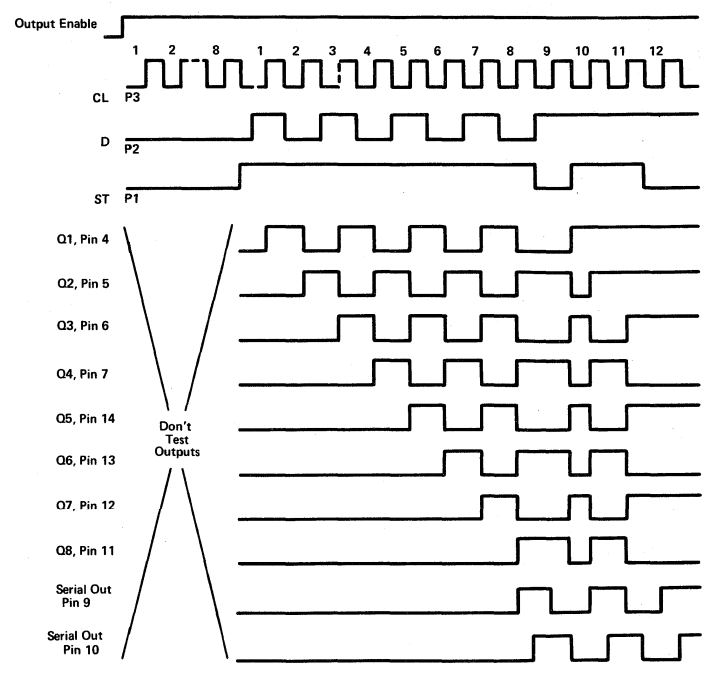


Fig. 5 – Waveforms used in functional testing.

Leakage Current Tests

Two types of static leakage currents are of concern in COS/MOS devices: Quiescent-leakage and input-leakage current.

Quiescent Leakage Current—In bipolar logic devices, such as TTL devices, the current paths that exist from the power source to ground in the quiescent state cause milliamperes of current to flow even when the device is not functioning. Quiescent leakage may be defined for a COS/MOS device as that current that flows from V_{DD} to V_{SS} when, theoretically, all paths for current flow have been opened because the MOS device is off, Fig. 6.

Typical input-leakage-current values for COS/MOS devices are in the picoampere range, hence the high input impedance. Automatic test sets cannot measure picoampere values because of test-set resolution. Input currents are measured using 100 nanoamperes as the maximum allowable leakage for a single input.

Examples of quiescent and input leakage test methods are shown in Figs. 8 and 9. In Fig. 8, the quiescent leakage current I_L (I_{DD} may be substituted for I_L) is measured by eliminating all current paths from V_{DD} to V_{SS}. This is done by turning off either the n or the p devices. The current may be measured in the V_{DD} or the V_{SS} line, whichever is more convenient. Unused inputs must be connected either high or low, depending on the channel leakage to be measured.

Input leakage current in Fig. 9 is measured by means of the gate input. Typical input impedance is 10^{12} ohms; therefore, typical input leakage currents are in the picoampere range. Figs. 8 through 14 show various test circuits for the CD4001A.

The testing of MSI and LSI parts for quiescent leakage current is more complex than that for SSI devices. However, the test is performed in a manner similar to that of the functional test described previously. The CD4090, for example, is connected as shown in Fig. 15. The device is then clocked into its various states, and the current monitored at applicable time slots.

Fig. 16 shows the intrinsic protection circuitry at each external-gate input. With S1 connected to either current source, the voltage drop from the gate input to ground will be one diode drop. A limit of 1.5 volts maximum is usually used to indicate a good diode. With S1 connected to the +100 microampere supply, the presence of the protective diode to the n substrate is tested. With S1 connected to the −100 microampere supply, the presence of the protective diode to the p well is tested. In the event of functional test failures, the above test can be used as a "contact test" to check for proper insertion of the device under test.

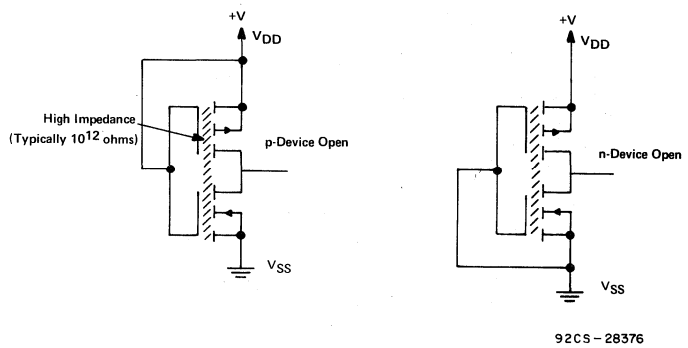


Fig. 6 — Schematic representations of p and n devices when turned off.

There is no perfect switch. However, the COS/MOS technology offers quiescent device currents that are orders of magnitude lower than in other forms of digital logic.

Quiescent-leakage tests are performed for all device states according to their respective truth tables. Voltages for quiescent leakage tests are 5, 10, and 15 volts for the CD4000A series and 5, 10, 15, and 20 volts for the CD4000B series. Power dissipation for COS/MOS devices is in the microwatt range regardless of complexity level, and is relatively stable with variations in temperature.

Input-Leakage Current—Input-leakage current is current that flows through reverse-biased diodes, whether intrinsic or diffused, and through the input-protection network connected to the gate. The diodes present in standard and improved protection networks are shown in Fig. 7.

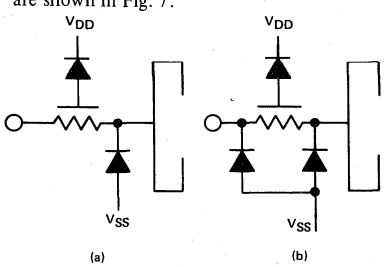


Fig. 7 — (a) Standard and (b) improved protection networks.

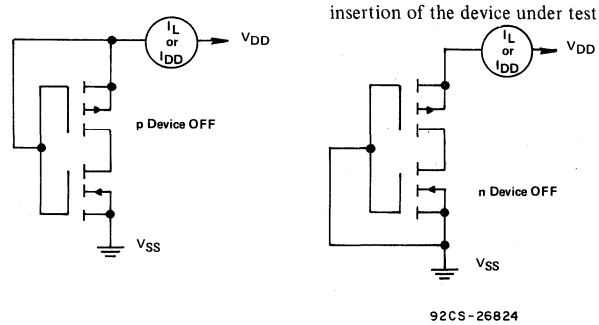


Fig. 8 — Measurement of quiescent leakage current.

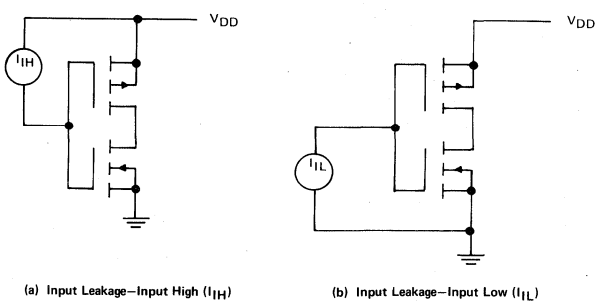


Fig. 9 — Measurement of input leakage.

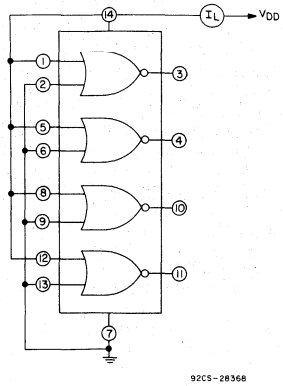


Fig. 10 – Quiescent-device-current test circuit for the CD4001A, leakage-inputs 1 (I_L).

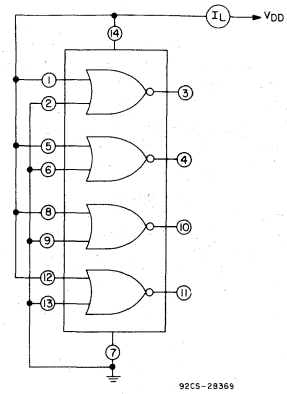


Fig. 11 – Quiescent-device-current test circuit for the CD4001A, leakage-inputs 2 (I_L).

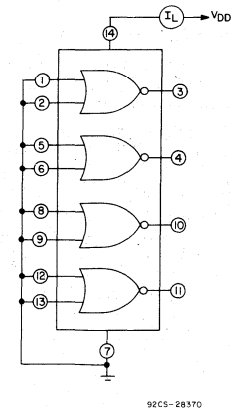


Fig. 12 – Quiescent-device-current test circuit for the CD4001A, leakage - n-devices off (I_L).

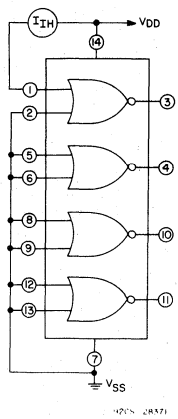


Fig. 13 – Input-current test circuit for the CD4001A, input high (I_{IH}).

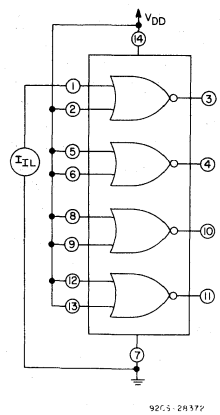


Fig. 14 – Input-current test circuit for the CD4001A, input low (I_{IL}).

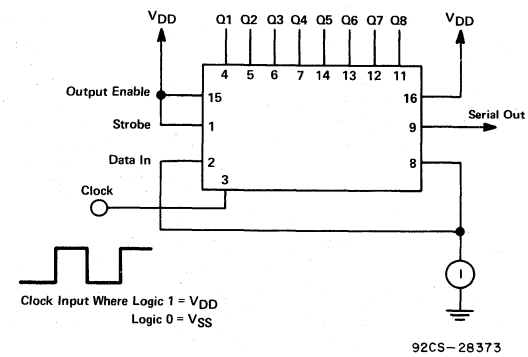


Fig. 15 – Functional-test arrangement for the CD4090.

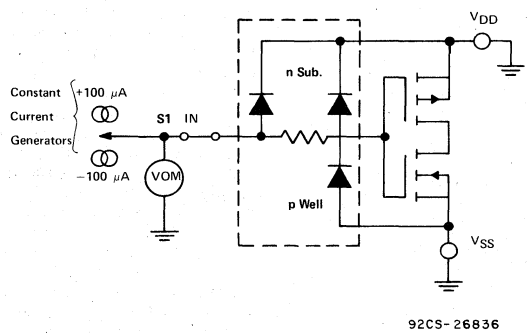


Fig. 16 – Intrinsic protection circuitry at each external input of a COS/MOS device.

Voltage Breakdown Tests

Breakdown tests are performed on the n and p channels of COS/MOS devices in a manner similar to that of quiescent-leakage-current tests. The purpose of the breakdown test is to assure that channel breakdowns can only occur at voltages above the maximum guaranteed supply voltage; Table II gives limits by series. Voltage breakdown test circuits are shown in Fig. 17. With switch S1 in position 1, the n devices are on and the p^+-to-n-substrate diodes are stressed. With switch S1 in position 2, the p devices are on and the n^+-to-p-well diodes are stressed.

Table II – Channel-Breakdown Limits

	Test Voltage	Max. Current Limit
CD4000A Series	15 V	100 μA
CD4000B Series	20 V	100 μA

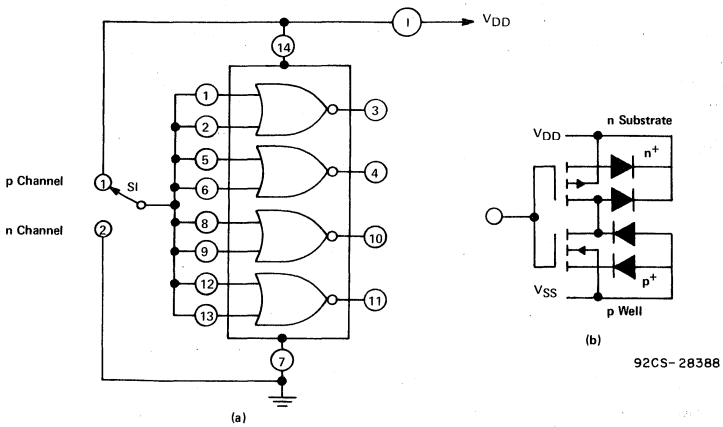


Fig. 17 – Voltage-breakdown test circuit.

Output-Voltage Levels

The output-voltage low (V_{OL}) and the output-voltage high levels (V_{OH}) of a COS/MOS device approach V_{DD} and V_{SS} within a few millivolts. Tests for V_{OL} and V_{OH} are primarily bench-type static tests performed as shown in Fig. 18. With switch S1 in position 1, one n device is turned on and the p devices are turned off. The voltage output will be at V_{SS} + 0.05 volt or V_{SS} – 0 volt. With switch S1 in position 2, all p devices will be turned on and the n devices will be turned off. The voltage output will be at V_{DD} + 0 volt or V_{DD} – 0.05 volt.

Few automatic test sets have the resolution to measure an offset of 50 millivolts from the V_{DD} and V_{SS} supply with satisfactory accuracy at reasonable test speeds.

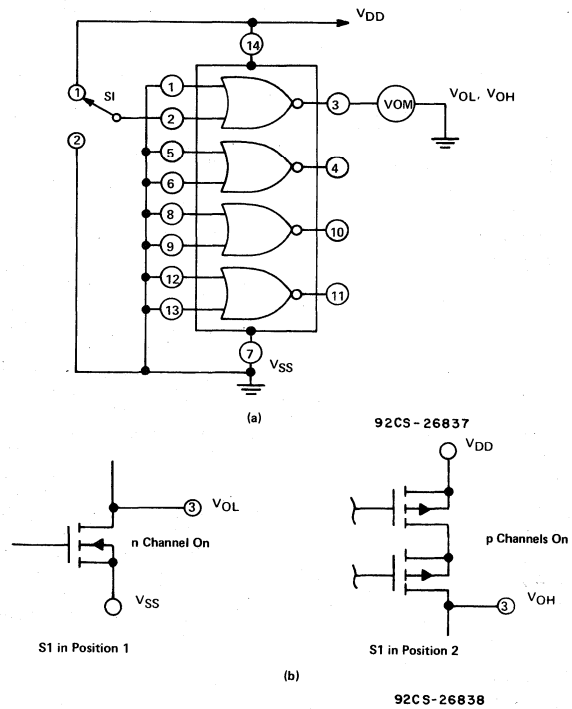


Fig. 18 – Test of output voltage levels (V_{OH} and V_{OL}) of a CD4001A.

Note that in functional testing, the pass/fail criteria for high and low output states of the device is a maximum of 500 millivolts deviation from V_{DD} and V_{SS}.

Noise Immunity

Noise immunity, V_{NL}, V_{NH}, is defined as the maximum low-level input (V_{IL}) for which an output logic level does not change state, and the minimum high-level input (V_{IH}) for which the output does not change state.

The typical noise immunity of a COS/MOS device is 45-percent of V_{DD}; i.e., the input voltage low and high levels will typically change 45-percent of their values before the output logic level changes. V_{IL} is guaranteed to be a maximum of 30 percent of V_{DD}; V_{IH} is guaranteed to be a minimum of 70 percent of V_{DD}.

Noise Margin

Noise margin is the difference between a device output voltage and V_{IL}; i.e., the magnitude of noise-margin voltage is that noise voltage that may be added to any COS/MOS input/output mode.

Noise margin and noise immunity are guaranteed to meet data-sheet specifications by the performance of input voltage tests, as shown in Fig. 19. The input voltage test is performed for each device as in functional testing. V_{IL} and V_{IH} are applied according to the device's truth table. The outputs are monitored for an expected V_{NMH} and V_{NML} state (voltage noise margin, voltage noise margin low).

$$V_{NML} = V_{OL} - V_{IL}$$
$$V_{NMH} = V_{OH} - V_{IH}$$
$$V_{IL} = V_{NL}$$
$$V_{IH} = V_{DD} - V_{NH}$$

Output Drive Current

Tests for output drive currents–I_{DN} (or I_{OL}), sink current, and I_{DP} (or I_{OH}), source current–are conducted by means of the circuits shown in Figs. 20 and 21.

The purpose of the sink-current test, Fig. 20, is to determine the amount of current that the output n device is capable of sinking (with the n channel on) at a given output-voltage level. Fig. 20(a) shows a CD4001AD device whose V_{DD} is equal to 10 volts and whose voltage output is specified at 0.5 volt. The amount of current that the output device can sink varies depending upon the voltage drop across the device (V_{DS}) for a fixed V_{GS}. n-channel drain characteristics are shown in Fig. 20(c).

The purpose of the source-current test, Fig. 21, is to determine the amount of current that the p device is capable of sourcing (with the p channel on) at a given output-voltage level. Fig. 21(a) shows a CD4001AD device whose V_{DD} is equal to 10 volts and whose voltage output is specified at 9.5 volts. Under these conditions, the

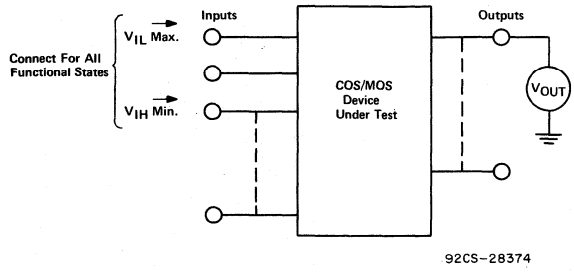
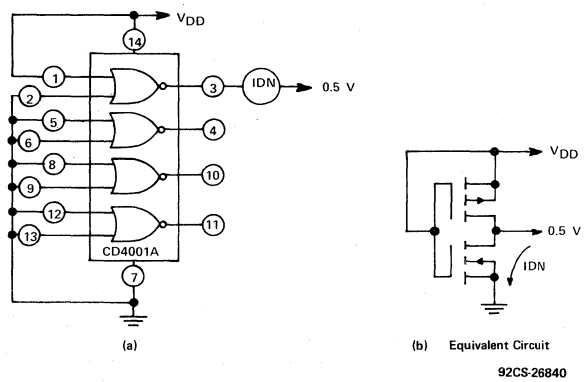


Fig. 19 – Input-voltage-level test arrangement.



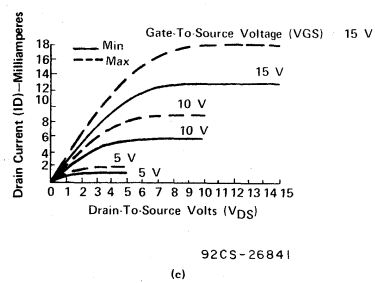


Fig. 20 – Output drive current (I_{DN}), sink-current, test arrangement.

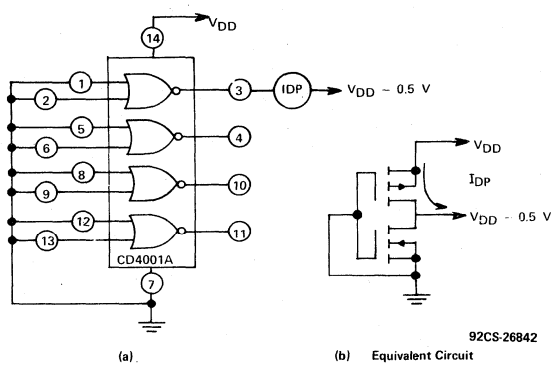


Fig. 21 – Output drive current (I_{DP}), source current, test arrangement.

output drive current will be a minimum of 0.25 milliampere. The amount of current that the device can source varies depending upon the voltage drop across the device (V_{DS}) for a fixed V_{GS}. p-channel drain characteristics are shown in Fig. 21 (c).

These current-voltage relationships can be verified, theoretically, by the use of the following equations.

In the triode region:

$$I_D = \frac{2K'W}{\ell}\left[V_{DS}(V_{GS}-V_{TH}) - \frac{V_{DS}^2}{2}\right] \quad 0 \leqslant V_{DS} \leqslant (V_{GS}-V_{TH})$$

In the saturated region:

$$I_D = \frac{K'W}{\ell}\left[V_{GS}-V_{TH}\right]^2 \quad 0 \leqslant (V_{GS}-V_{TH}) \leqslant V_{DS}$$

where V_{DS} = drain-to-source voltage

V_{GS} = gate-to-source voltage

V_{TH} = device threshold voltage

$K' = \frac{\mu\epsilon_O}{2t_{OX}}$ μ = effective surface mobility of the carrier in the channel

ϵ_O = permittivity of the oxide

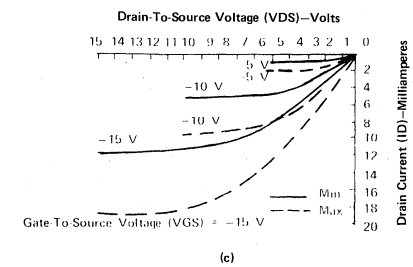
t_{OX} = oxide thickness

W = channel width

ℓ = channel length

Input Capacitance

The input capacitance of a device is measured as shown in Fig. 22. A capacitance bridge is connected between each input and V_{SS}. The capacitance is then measured after all stray capacitance has been nulled. The test is performed at a 1-MHz bridge setting. Device input capacitance is considered acceptable if the bridge reading is less than the maximum input capacitance specified on the data sheet.



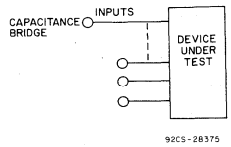


Fig. 22 – Input capacitance measurement.

DYNAMIC TESTING

Propagation Delay and Transition Times

Propagation Delay (t_{PLH}) is measured from the 50-percent point of the input pulse to the 50-percent point of the output pulse as the output goes from a low level to a high level.

Propagation Delay (t_{PHL}) is measured from the 50-percent point of the input pulse to the 50-percent point of the output pulse as the output goes from a high level to a low level.

Transition Time (t_{TLH}) is the time required for the output to make the transition from the low state to the high state (n device turns off, p device turns on). This time is measured from the 10-percent point to the 90-percent point of the output pulse.

Transition Time (t_{THL}) is the time required for the output to make the transition from the high state to the low state (p device turns off, n device turns on). This time is measured from the 10-percent point to the 90-percent point of the output pulse.

Dynamic parameters are measured at a specified load of 15 and/or 50 picofarads. The load specified is for total capacitance including stray and probe capacitance. Frequency is not a critical factor in determining switching speeds of COS/MOS devices. Testing should be done at a frequency compatible with the test set or laboratory equipment involved and must be less than the maximum operating frequency. Fig. 23 shows waveforms used in the measurement of propagation delay and transition times.

Note that certain dynamic tests, when performed on a go-no-go basis, are conducted with specified limits as test conditions and with the device outputs monitored. Parameters tested in this way include set-up times, minimum clock, reset and preset pulse widths, clock rise and fall times, maximum clock frequency, and preset and reset removal times. Parameters such as propagation delay and transition times are tested under a set of prescribed conditions so that the test yields actual characteristic data.

Maximum Operating Frequency

The maximum operating frequency, f_{CL}, is that clock input frequency above which the device will no longer perform its logical function. This frequency is determined by gradually increasing the input frequency while monitoring the output until the device no longer functions properly. The input frequency is then lowered until the device resumes correct operation. The frequency thus determined is the maximum operating frequency of the individual device.

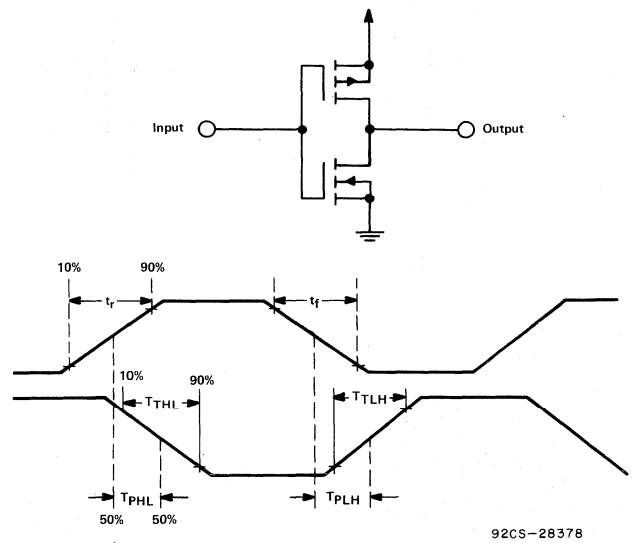
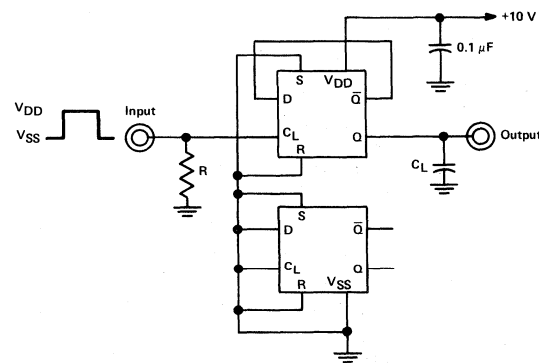


Fig. 23 – Waveforms used in the measurement of propagation delay and transition times.

When testing for compliance a device for which a maximum operating frequency has been specified, the maximum specified operating frequency is applied to the device while the outputs are monitored. This is a go-no-go test as opposed to a characterization test.

Fig. 24 shows a CD4013, dual D-type flip-flop, under test for maximum operating



Test Conditions (Per Data-Sheet Specifications*)

* Pulse-Generator Amplitude	10 V
Pulse-Generator Impedance-Matching Resistor (R)	50 ohms
*Pulse-Generator Rise and Fall Times ($t_r = t_f$)	20 ns
*Pulse-Generator Input Frequency (f_{CL})	7 MHz
*Load Capacity – C_L (Including Stray and Probe)	15 pF, 50 pF

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Fig. 24 – Test circuit for measuring the maximum operating frequency of a CD4013A/B.

frequency at an operating voltage of $V_{DD}-V_{SS}$ of 10 volts.

Set-Up Time

Set-up time (t_S) is the time interval during which a signal is applied and maintained at a specified input terminal before the device recognizes the presence of the specified input pulse. An example of set-up time measurement for a CD4013, Fig. 25, shows a data input which must be present for time t_S (value specified in data sheet) in order for the positive transition of the clock pulse to transmit the level at the data input to the Q output. If the data input is not present for a sufficient period of time prior to the positive transition of the clock, the previous state of the data input will be recognized and transmitted to the Q output.

When testing a device for compliance with a specified set-up time, a go-no-go test, the set-up time specified in the data sheet is used as a test condition and the output is monitored for expected operation. When characteristic data is required, the set-up time is varied until the expected output occurs.

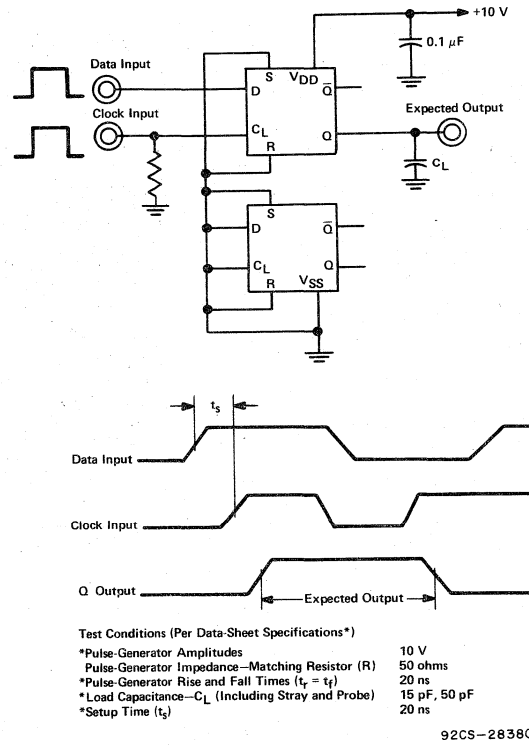


Fig. 25 – Set-up-time test circuit for a CD4013A.

Minimum Clock, Set, Reset, and Preset Pulse Widths

Pulse widths, t_W, are defined as the time from the point on the leading edge of the clock-pulse curve which is 50-percent of the maximum amplitude to a point on the trailing edge which is 50-percent of the maximum amplitude, Fig. 26. The minimum pulse width for the clock, set, reset, and preset inputs is that time that the pulse must be present in order for the device to recognize the presence of the pulse.

When testing a device for compliance with minimum pulse widths, a go-no-go test, the pulse width specified in the data sheet is used as a test condition and the output is monitored for expected operation. When characteristic data is required, the pulse width is varied until the expected output occurs.

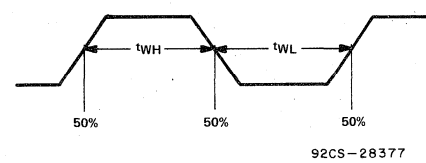


Fig. 26 – Waveform used to define pulse widths.

An example of minimum clock-pulse width measurement (t_{WH}) for a CD4013 at a $V_{DD}-V_{SS}$ of 10 volts, Fig. 27, shows the minimum clock-pulse width specified in the data sheet being applied to the clock input of the device under test at a frequency (f) that is less than the maximum operating frequency specified. The clock pulse is applied in one case when the data input is low and is then applied again when the data input is high. (The high and low states of the data input must be present for a time exceeding the specified set-up time.) A device that complies with the minimum clock-pulse width parameter specification will transmit the data input level to the Q output on the positive transition of the clock. Proper operation of the CD4013 can be checked by monitoring for an expected output at Q of f/2.

Maximum Clock Rise and Fall Times

The maximum clock rise and fall times (t_{rCL}, t_{fCL}) are the rise and fall times of the clock input signal (measured from 10 percent to 90 percent), above which the device is guaranteed to perform its logical function. This rise and fall time is determined by gradually increasing the clock rise/fall time while monitoring the output until the device no longer functions properly. The clock input rise and fall times are then lowered until the device resumes correct operation. The rise and fall times thus determined are the maximum clock rise and fall time of the individual device.

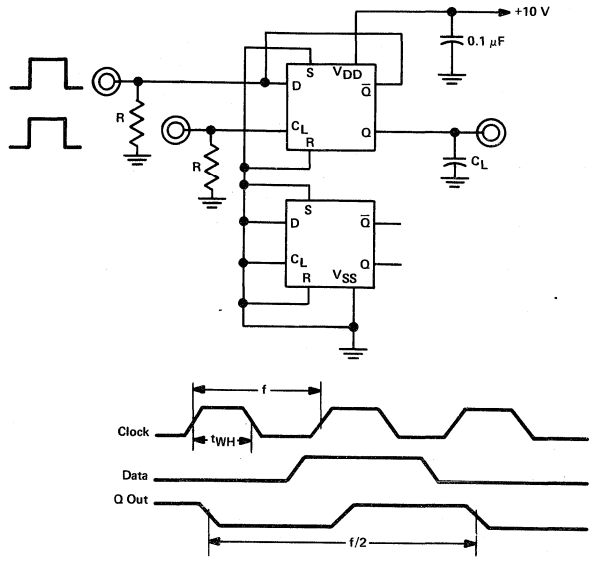
In testing a device for maximum clock rise and fall times to a specified limit, the maximum specified clock rise and fall times are applied to the clock input while the output is monitored. The input frequency used to perform this test must be less than the reciprocal of $2t_r$; for example, when applying the specified clock rise and fall times for a CD4013 at a $V_{DD}-V_{SS}$ of 10 volts, the maximum clock input frequency that may be used is 100 kHz.

Fig. 28 is an example of a test of maximum clock rise and fall times of a CD4013, dual flip-flop, at an operating voltage, $V_{DD}-V_{SS}$ of 10 volts.

Reset, Set and Preset Removal Time

The reset, set, and preset removal time, t_{REM}, when used in reference to flip-flops, counters, and shift registers, is that time for which the reset, set, or preset pulse must be in its clock enabling state before the device can resume synchronous operation.

When a device is in the preset mode, the JAM input levels are transmitted to the Q output asynchronously. The reset state causes the Q outputs to go to a low level; the set state causes the Q outputs to go to a high level. It is generally an invalid condition to



Test Conditions (Per Data-Sheet Specifications*)

* Pulse-Generator Amplitudes	10 V
* Pulse-Generator Rise and Fall Times	20 ns
Pulse-Generator Impedance-Matching Resistor	50 ohms
* Clock-Pulse-Generator Frequency	<< Max. Operating Frequency
* Load Capacity (C_L) (Total Including Stray)	15 pF, 50 pF

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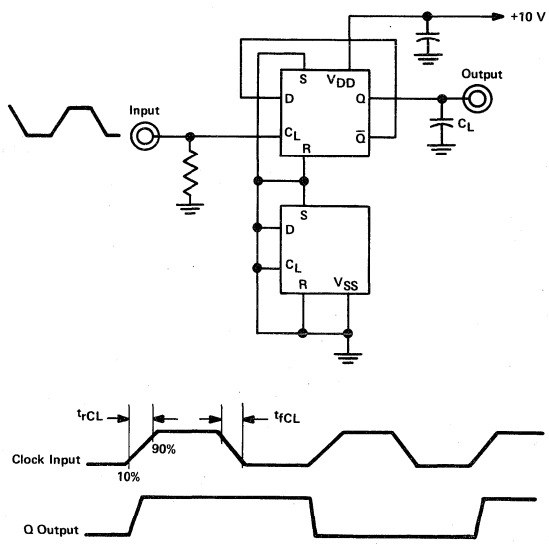
Fig. 27 – Test circuit for measuring minimum clock-pulse width in a CD4013A/B.



Test Conditions (Per Data-Sheet Specifications*)

* Pulse-Generator Amplitude	10 V
* Pulse-Generator Rise and Fall Times (t_{rCL}, t_{fCL})	5 μs
Pulse-Generator Impedance-Matching Resistor	50 ohms
* Pulse-Generator Frequency	100 kHz
* Load Capacity (C_L) (Total Including Stray and Probe)	15 pF, 50 pF

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Fig. 28 – Test circuit for measuring maximum clock-pulse width in a CD4013A/B.

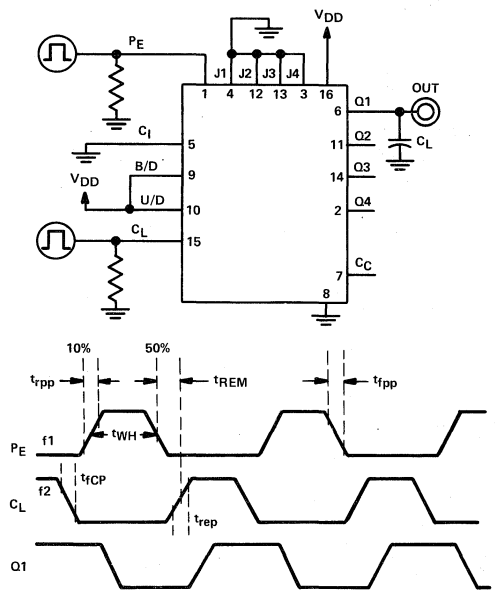
have a device in more than one asynchronous state at the same time.

In testing a device for compliance with data-sheet specifications, the removal time specified is applied at the appropriate input terminal of the device under test. When characterizing a device, the removal time is adjusted relative to the clock input such that expected operation occurs, decreased to the point where expected operation no longer occurs, and then increased until expected operation reoccurs. The time recorded at the reoccurrence of expected operations is the correct removal time (t_{REM}).

An example of a test for minimum preset-enable removal time as specified in the data sheet of a CD4029A, presettable up/down counter, is shown in Fig. 29. The JAM inputs J1, J2, J3, and J4 are hard-wired to ground (low). With the preset enable input high, the information on the JAM inputs is transmitted to the Q outputs (regardless of the state of the clock). The preset input is then set low. After a time equal to t_{REM}, the clock-pulse positive transition advances the counter and causes the Q1 output to go high. The transition of the Q1 output from the low to the high state confirms that the preset enable pulse has been removed for a sufficient time to allow the device under test to resume synchronous clocked operation.

Reference

1. Guide to Better Handling and Operation of CMOS Devices, ICAN-6525, J. Flood and H. Pujol, RCA Solid State, 1976.



Test Conditions (Per Data-Sheet Specifications)	
Pulse-Generator Amplitude	V_{DD}
Pulse-Generator Rise and Fall Times ($t_{rpp} = t_{fcp}$)	20 ns
Pulse Generator Impedance-Matching Resistor	50 ohms
Load Capacity (C_L) (Total Including Stray and Probe)	15 pF, 50 pF

92CS-28382

Fig. 29 – Test circuit for measuring preset-enable removal time in a CD4029A/B.

Understanding Buffered and Unbuffered CMOS Characteristics

by R. E. Funk

INTRODUCTION

Both buffered and unbuffered CMOS B-series gates, inverters, and high-current IC products are available from RCA; each product classification has application advantages in appropriate logic-system designs. Recently, many CMOS suppliers have been concentrating on promoting buffered B-series products with applications literature focusing on the attributes and use of the buffered types. This practice has left an imbalance in the understanding and application of **both** buffered **and** unbuffered gates and, in many instances, customers are not using unbuffered products when they are the best for the intended application. This Note narrows the misunderstandings involved in this issue by presenting and discussing the relative merits of the buffered and unbuffered CMOS devices.

Background

Historically, most CMOS gates, inverters, and high-current IC products were unbuffered, and exhibited good logic-system performance, speed, noise immunity, and quasi-linear characteristics in a wide variety of applications. As the scope of CMOS products broadened and more manufacturers entered the scene, buffered gate and inverter products were brought out by RCA and others. While RCA confined initial buffered products to new OR and AND functions, other manufacturers introduced buffered NOR and NAND gates having the **same** generic 4000A-series designations as the original widely-used unbuffered gates. Many users were surprised by the non-interchangeability of the devices in applications where speed, noise immunity, output impedance, and linear gain-bandwidth characteristics were critical. It is of immense benefit to CMOS users to have available the definitions and designations of **both** buffered and unbuffered B-series CMOS devices as determined by the JEDEC CMOS Standardizing Committee under the cognizance of the JC40.2 JEDEC Committee of EIA. The official JEDEC definitions are repeated below along with detailed explanations and examples. Comparison of user-oriented characteristics and the use of buffered and unbuffered gates are also reviewed.

Definitions

Buffered CMOS–A CMOS device for which the output on impedance is independent of any and all valid input logic conditions, both preceding and present, is said to have a buffered output or to be a buffered CMOS device. All such products are designated by the suffix B.

Unbuffered CMOS–Products that meet B-series specifications except that the logical outputs are not buffered and the V_{IL} and V_{IH} specifications are 20 percent and 80 percent of V_{DD}, respectively, are marked with the UB designation, such as (including, but not limited to):

4000UB	4025UB
4001UB	4007UB
4002UB	4009UB
4011UB	4041UB
4012UB	4049UB
4023UB	4069UB

The official JEDEC definitions are primarily applicable to gates, inverters, and high-current (inverting) drivers such as the specific UB types shown above. Non-inverting gates and drivers as well as all MSI and LSI B-types are by definition B types. There are special analog I/O types that are also included as B types since they conform to all B standards except that they have special analog I/O circuitry. Examples of parts that have no buffered or unbuffered significance are:

4016B	4053B
4046B	4067B
4051B	4097B
4052B	4066B
	4511B
	4528B

RCA will make available both types of CMOS gates. Logic examples of the buffered and unbuffered 2-input NOR gate are shown in Fig. 1. Note that the buffered logic can be implemented by either a 2-input NOR function followed by two inverters or by two input inverters followed by the 2-input NAND gate and an output buffer. RCA uses the latter logic configuration, which has the advantage of optimizing device noise immunity by negating the effect of stacked devices at the input. This characteristic is

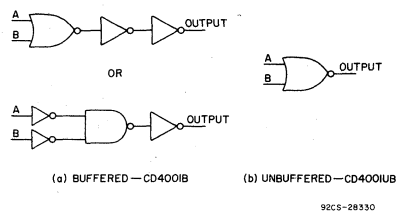


Fig. 1 – Examples of the buffered (CD4001B) and unbuffered (CD4001UB) 2-input NOR gate.

especially significant for 3- or 4-input gates where three or four PMOS or NMOS transistors are stacked in series at the input. In this case, the inputs have an effective offset in threshold and reduced input noise immunity.

Fig. 2 is a schematic representation of the RCA buffered and unbuffered 2-input NOR gates. The improved 4-diode-input gate-oxide protection circuit is shown at the inputs.

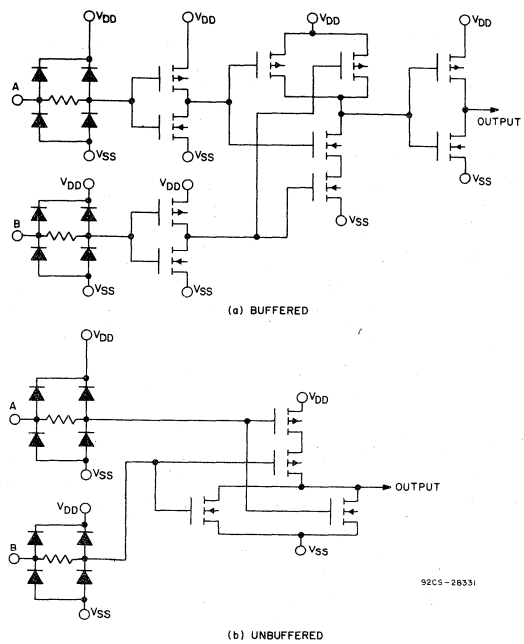


Fig. 2 – Schematic diagrams of the buffered and the unbuffered 2-input NOR gate.

Examples

Examination of the dc performance characteristics of both the buffered and unbuffered 2-input NOR gate reveals the two electrical characteristics, output impedance and noise immunity, by which the types are differentiated by the JEDEC standard specifications:

Output Impedance

–Buffered–Fig. 3 depicts the buffered output stage and shows the MOS transistor as switched on with a channel resistance R; R is the **same** value for the n-switch closed or the p-switch closed.

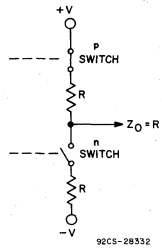


Fig. 3 – Constant output impedance of a buffered gate.

–Unbuffered–Fig. 4 depicts the unbuffered 2-input-gate p- and n-channel MOS switches and appropriate on-channel resistances. Note that the two stacked p-channel switches are designed for an on resistance of R/2. so that the output impedance is R when both the logic inputs are low, Fig. 4(b). In Fig. 4(a) the output impedance is R to the negative supply terminal (usually ground) for an input logic state of 1, input high. Fig. 4(c) shows the condition when the unbuffered gate has an output impedance of R/2 for both logic inputs high. Hence the variable output impedance of the unbuffered gate. For a 4-input gate, this variable is R to R/4! The maximum output resistance of RCA buffered or unbuffered gates is R. Thus, minimum I_{OL} and I_{OH} specifications for buffered and unbuffered gates are identical.

Noise Immunity

The second JEDEC-defined difference between the buffered and unbuffered CMOS gates (or inverters) is the difference in input noise-immunity characteristics.

–Buffered–The buffered 2-input NOR gate voltage-transfer characteristics, Fig. 5, are squared because of the gain of three CMOS stages from input to output. Fig. 5 shows that noise voltage inputs of ±1.5 V at V_{DD} = 5 V and ±4 V at V_{DD} = 15 V will have little discernible effect on the output voltage; i.e., noise immunity for **all** logic states is optimally high as is noise margin: 1 volt at V_{DD} = 5 V and 2.5 V at V_{DD} = 15 V.

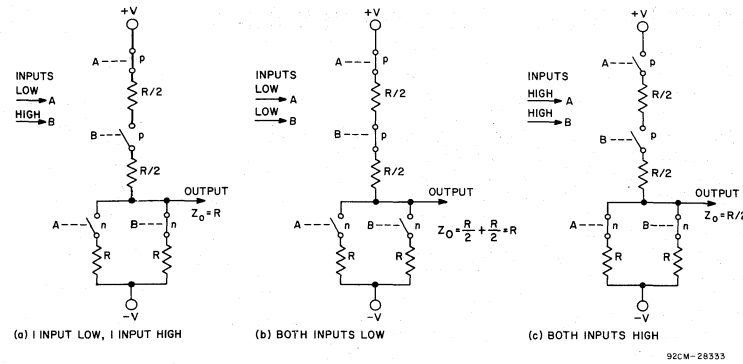


Fig. 4 – Variable output impedance of an unbuffered 2-input NOR gate. The resistors represent the on impedance of a p- or n-channel MOS transistor.

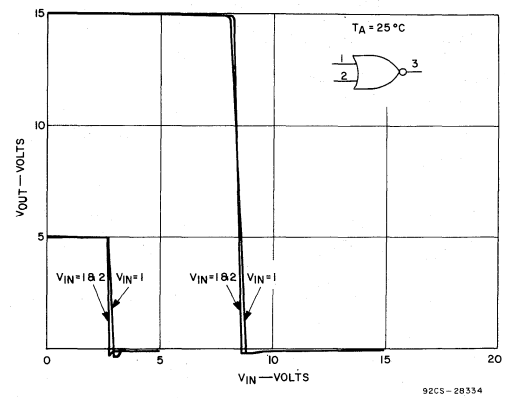


Fig. 5 – Voltage transfer characteristics of a buffered 2-input NOR gate (CD4001B).

–Unbuffered–Fig. 6 shows the rounded voltage-transfer characteristics of the 2-input unbuffered NOR gate. Also evident is the shift in the transfer curve for the different logic input states. Compare these curves to those of Fig. 5 and the effects of the non-buffered inputs as well as the gain differences are evident. The rounded characteristics require a noise-immunity specification of ±20% of V_{DD} at 5, 10 and 15 V as well as a reduced noise margin: 0.5 V at V_{DD} = 5 V and 1.0 V at V_{DD} = 15 V.

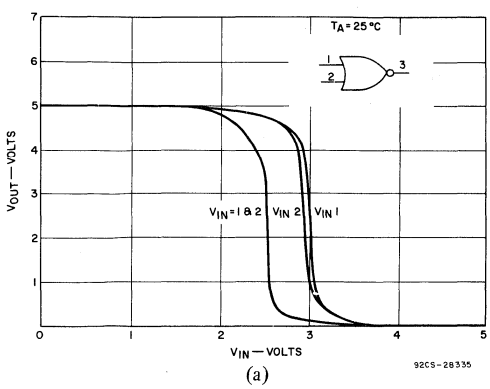
The above definitions use gate characteristics as illustrative of the JEDEC definitions for buffered and unbuffered characteristics relative to variable output impedance and noise-immunity performance. Inverters and high-current drivers may also be defined as buffered (B) types or unbuffered (UB) types by virtue of the squared or rounded transfer characteristics of Figs. 3 and 4, respectively. Even though both types have a single NMOS and single PMOS output transistor, the rounded transfer characteristic of the unbuffered inverters makes them UB types by virtue of:

1. Reduced noise-immunity performance where the 20% rating is applicable.
2. Varying output impedance as a function of input voltage change along the rounded portion of the transfer curve.

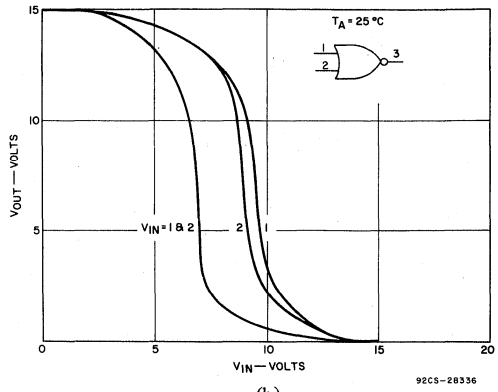
COMPARISONS

Table I shows the qualitative comparisons of user-oriented performance characteristics of buffered and unbuffered CMOS gates, inverters, or drivers. Table II is a quantitative comparison of the key performance characteristics with explanations as follows:

Propagation Delay–Delays shown are applicable to RCA 2-, 3-, and 4-input NOR and NAND gates.



(a)



(b)

Fig. 6 — Voltage transfer characteristics of an unbuffered 2-input NOR gate (CD4001UB) with output voltages of 5 and 15 volts.

Table I—Comparison of Buffered and Unbuffered Gate Characteristics

Characteristic	Buffered	Unbuffered
Propagation Delay	Slow	Fast
Noise Immunity/Margin	Excellent	Good
Output Impedance and Output Transition Time	Constant	Variable
AC Gain	High	Low
Output Oscillation for Slow Inputs	Yes	No
Input Capacitance	Low	High

Table II—Characteristics of Buffered and Unbuffered Gates

		Buffered Gates	Unbuffered Gates
Typical Propagation Delay			
V_{DD} = 5 V, C_L = 50 pF		150 ns	60 ns
V_{DD} = 10 V		65 ns	30 ns
V_{DD} = 15 V		50 ns	25 ns
Noise Immunity		30% of V_{DD} at 5 and 10 V 27% at 15 V	20% of V_{DD} at 5, 10, and 15 V
Noise Margin	V_{DD}= 5 V	1 V	0.5 V
	10 V	2 V	1.0 V
	15 V	2.5 V	1.0 V
Typical Output Impedance			
V_{DD} = 5 V, V_O = ±0.4 V			
2-Input Gate		400 ohms	200-400 ohms
3-Input Gate		400 ohms	133-400 ohms
4-Input Gate		400 ohms	100-400 ohms
Typical Output Transition Time			
V_{DD} = 5 V, C_L = 50 pF (2-, 3-, 4-Input Gates)		100 ns	50-100 ns
AC Gain	V_{DD}=10 V	≈68 dB	≈23 dB
AC Bandwidth	V_{DD}=10 V	280 kHz	885 kHz
Output Oscillation For Slow Inputs		Susceptible For t_r,t_f to 1 ms	Not Susceptible For t_r,t_f to 100 ms
Typical Input Capacitance			
Average		1-2 pF	2-3 pF
Peak		2-4 pF	5-10 pF

Noise Immunity—Table III shows the detailed input-voltage data-sheet specifications for buffered and unbuffered gates. From these test conditions the user-oriented noise-immunity and noise-margin data of Table II are derived. Also refer to Figs. 5 and 6 for the voltage-transfer characteristics that illustrate the reason for the different input-voltage-specification requirements for buffered and unbuffered devices.

Output Impedance—Refer to Figs. 3 and 4 and accompanying descriptions of the constant output impedance of buffered gates and the variable output impedance of unbuffered gates. Note that **both** buffered and unbuffered RCA 2-, 3- and 4-input gates are designed to meet the same maximum output impedance; output current ratings (I_{OL} and I_{OH}) have the same minimum limit on RCA data sheets.

Output Transition Time—The time required for a CMOS output to transfer high or transfer low is constant for buffered gates but varies according to input logic states for unbuffered gates. Output transition time varies as a function of the driving source resistance of the output, which is state dependent as indicated in Fig. 4, as well as the device output capacitance, which is dependent on both device size and input logic state. Because of variable output capacitance, output-transition-time variations are not a linear function of output resistance. As Table II shows, RCA 2-, 3- and 4-input unbuffered gates exhibit a net 2-to-1 difference in output transition time even though the output resistance has a net 4-to-1 variation for the 4-input gate.

Table III—Input-Voltage Specifications

Characteristic	V_O	V_{DD}	Limit Min.	Limit Max.	Units
Input Voltage Low (V_{IL})	4.5	5	–	1.5	Volts
	9	10		3	
B	13.5	15	–	4	
UB	4.5	5	–	1	
	9	10	–	2	
	13	15	–	3	
Input Voltage High (V_{IH})	0.5	5	3.5	–	
	1	10	7	–	
B	1.5	15	11	–	
UB	0.5	5	4	–	
	1	10	8	–	
	2	15	12	–	

Notes:

1. Noise-immunity voltage is the V_{IL} or V_{IH} Specification Limit.
2. Noise-margin voltage is computed as follows:
   Noise-Margin Voltage = $V_{IL} - (V_{DD} - V_O)$
   = $(V_{DD} - V_{IH}) - V_O$.

AC Gain and Bandwidth—CMOS linear-mode gain was measured for both the buffered and unbuffered RCA 2-input NOR gate by means of the test circuit of Fig. 7. Fig. 8 shows typical linear-mode gain difference between buffered and unbuffered RCA 2-input NOR gates. While absolute performance depends on device type (inverters; 2-, 3-, 4-input gates) and test configurations, Fig. 8 defines the approximately 3-to-1 difference in linear-mode performance between buffered and unbuffered gates.

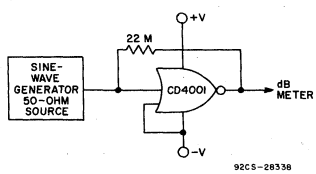


Fig. 7 – Linear-gain test circuit.

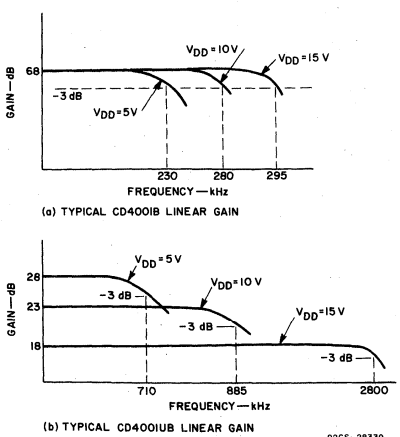


Fig. 8 – Typical linear-mode gain of buffered and unbuffered 2-input NOR gate.

Output Oscillation for Slow Inputs—The high linear-mode gain of buffered CMOS devices can lead to undesirable oscillation at outputs when input ramps are in excess of approximately 1 millisecond duration. Fig. 9 illustrates this effect when approximately 1 to 2 millivolts of ac noise within the device bandwidth on the input signal are amplified through the device and tend to develop a few cycles of oscillation between the positive and negative rails under 5-volt operation. In contrast, unbuffered gates do not tend to oscillate unless a noise voltage of 200 to 300 millivolts were present within the bandwidth of the device. An input ramp of up to 100 milliseconds duration did not create oscillation in laboratory tests of RCA unbuffered gates.

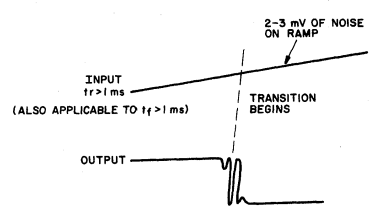


Fig. 9 – Buffered output oscillation for a slow input.

Input Capacitance—Figs. 10 and 11 show the dynamic input capacitance of the RCA buffered and unbuffered 2-input NOR gates, respectively. The large MOS transistor geometry of the unbuffered NOR gate is responsible for the higher peak input capacitance (Miller effect) in the linear switching range. The longer dwell in this linear region also tends to broaden the Miller capacitance, and therefore increases the effective average input capacitance. Buffered gates and inverters are rated at a maximum input capacitance of 1 unit load (7.5 picofarads—JEDEC standard); unbuffered gates and inverters are rated at 2 unit loads (15 picofarads maximum). High-current unbuffered drivers, such as the CD-4049UB, are rated at 3 unit loads (22.5 picofarads maximum).

Applications Guidance

Table IV summarizes preferred application areas for both buffered and unbuffered RCA B-series IC products. This information is based on the buffered and unbuffered CMOS device characteristics listed in Table II combined with the author's experience and familiarity with the application areas indicated. The information given is general guidance to allow the designer to key in on the specific performance characteristics of either device type. The data provided in this Note are derived from RCA standardized B and UB products whose circuit designs were implemented to match performance between UB and B gate types as closely as possible. For example, device sizes were selected to assure matched output drive. In addition, the process and layout rules followed in B and UB designs of RCA product are identical, as is the use of improved gate-oxide protection circuitry for B and UB product.

RCA Gate, Inverter, and Driver Products

Table V is a current list of SSI (small scale integrated) B and UB products presently in production by RCA. Refer to RCA product guides and the Databooks for detailed product information.[1]

References

1. COS/MOS Digital Integrated Circuits, Product Guide, COS-278E, 1976.
   RCA Integrated Circuits, Databook, SSD-210, 1976.

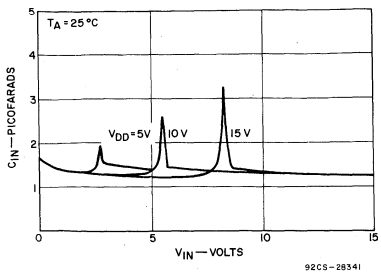


Fig. 10 — Input capacitance of a buffered 2-input NOR gate (CD4001B).

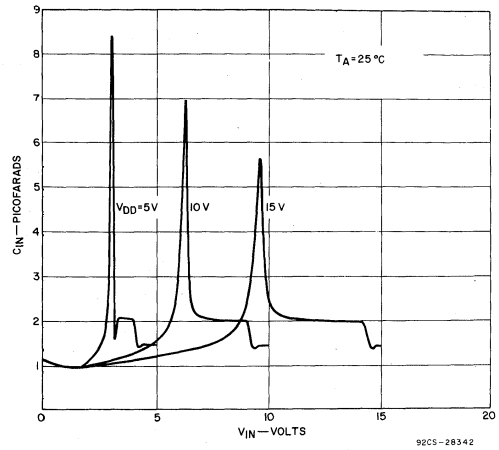


Fig. 11 — Input capacitance of an unbuffered 2-input NOR gate (CD4001UB).

Table IV—Applications of Buffered and Unbuffered CMOS Gates and Inverters

Application	Buffered	Unbuffered
High-Speed Systems	—	Preferred
High-Noise Environments, Low-Speed Systems	Preferred	—
Ultra-Low-Frequency Systems Inputs <1 kHz sine wave or ramps with t_r,t_f >1 ms* excluding Schmitt Triggers	—	Preferred
Gate Applications Requiring Constant Output Impedance Such as D/A R-2R Conversion	Preferred	—
High-Freq., Moderate Gain, Linear Amplification	—	Preferred
Low-Freq., High Gain, Linear Amplification	Preferred	—

*Applies to gates of inverter designs of Astable or Monostable multivibrators with T > 1 millisecond.

Table V—RCA COS/MOS Buffered and Unbuffered Gate, Inverter, and Driver Types

Buffered	Unbuffered
CD4000B	CD4000UB
CD4001B	CD4001UB
CD4002B	CD4002UB
CD4010B	CD4007UB
CD4011B	CD4009UB
CD4012B	CD4011UB
CD4023B	CD4012UB
CD4025B	CD4023UB
CD4050B	CD4025UB
CD4068B	CD4041UB
CD4071B	CD4049UB
CD4072B	CD4069UB
CD4073B	
CD4075B	
CD4078B	
CD4081B	
CD4082B	

COS/MOS Electrostatic-Discharge Protection Networks

by H. L. Pujol

RCA's two families of CMOS devices, the standard A series (3 to 15 volts) and the high-voltage B series (3 to 20 volts), are equipped with networks to protect the gate oxide of the devices against damage resulting from discharge of electrostatic energy between any two pins.

The gate input of a CMOS device is equivalent to a small, low-leakage capacitor (typically 5 picofarads) in parallel with a very high resistance (typically 10^{12} ohms). Because of this extremely high impedance which lends itself to the buildup of electrostatic charge, even a very low energy source (such as a static charge) is capable of developing voltages in the order of 80 volts, the typical breakdown voltage of an MOS gate oxide. In contrast with other semiconductor devices in which the breakdown can be tested any number of times without damage, the MOS gate oxide can be shorted, and the device destroyed, as the result of only one voltage excursion to the breakdown limit.

Protection Networks

Figs. 1 through 4 show the various protection networks incorporated in all COS/MOS product.

Standard Protection Networks

Fig. 1 shows the standard protection network incorporated in all A-series and some B-series devices. Input-diode D_2 is a distributed resistor-diode network that appears as two diodes to V_{DD}.

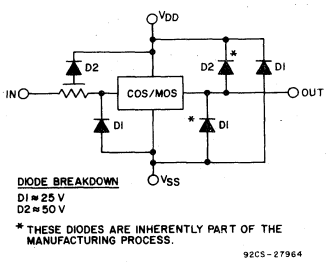


Fig.1 – Standard protection network.

Improved Protection Network

Fig. 2 shows the improved protection network incorporated on all new B-series devices as well as on all A-series B-converted types.

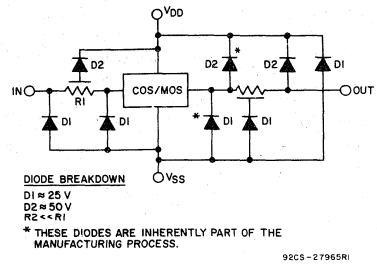


Fig.2 – Improved protection network.

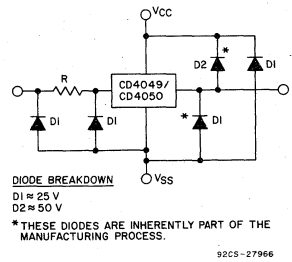


Fig.3 – Modified protection network.

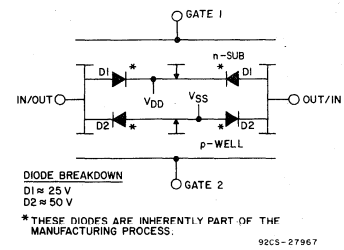


Fig.4 – Transmission gate with intrinsic diodes that protect against electrostatic discharge.

Other Protective Networks

Fig. 3 shows the modified protective network for a CD4049/4050 buffer. The input diode to V_{DD} is not incorporated so that the level-shifting function can occur.

Equivalent-Body Discharge Network

The protection networks described in this Note are evaluated and characterized by using the equivalent-body discharge network of Fig. 5. As C is increased, the amount of static energy dumped into the CMOS device increases. As R is decreased, the energy dissipated outside the device is reduced, thereby increasing the energy dissipated in the unit. A mercury relay is used to switch the RC source because such relays are fast and free from arcing or bouncing effects. Characterization of the various protection networks is done in 12 different combinations of inputs, outputs, and

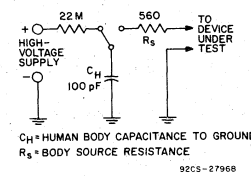


Fig.5 – Equivalent-body discharge network.

polarities. The combinations include all combinations of any two of the following pins: input, V_{DD}, V_{SS}, and output.

Evaluation of a protective network begins with the charging of a 100-picofarad capacitor through a 22-megohm resistor and a mercury relay to the desired voltage. The capacitor C_H of Fig. 5 is then discharged through the same mercury relay and a 560-ohm resistor into the pins under test. Results of repetitive tests are used to determine the worst-case capability of the protective networks, Table I.

TABLE I – Worst-Case Capability of Protective Networks

Protective Network	Worst-Case Capability
Standard (incl. CD4049, CD4050)	1 kV to 2 kV
Improved	4 kV
Transmission Gate	<800 V

Additional protection can be obtained by adding external series resistors at device inputs. The value of this resistance should be approximately 10 kilohms for gate inputs and 1 kilohm for transmission gate inputs. In addition, zener diodes at the output pins can clamp the voltage to a safe level. The zener-voltage should not exceed the absolute maximum rating of the part. On-chip protection networks are not used on transmission gates so that their low "on" resistance can be maintained. The 800-volt worst-case capability shown in Table I is provided by the intrinsic diodes shown in Fig. 4.

The value of the input resistor on all protection networks, except that used in

transmission gates, can vary between 100 ohms and 2.5 kilohms because of circuit-design differences. This resistance, in conjunction with the capacitance of the gate and the associated protective diodes, integrates and clamps the device voltages to a safe level. The diagrams of Figs. 6, 7, and 8 demonstrate that the standard protection networks prevent higher than normal voltages from reaching the gate of the MOS device. In addition, the low RC time constant assures that circuit speed remains unchanged in spite of the additional components.

Because of the presence of the integral protection network, the V_{DD} power supply must not be turned off while a signal from a low-impedance pulse generator is being applied at an input of a COS/MOS circuit. Should the V_{DD} supply be turned off under such conditions, the V_{DD} line would be essentially grounded, and a positive voltage from the pulse generator would be impressed across the input diode to V_{DD}. This voltage could cause permanent damage to the diode or burn out the V_{DD} metallization. If it is expected that any input excursion will exceed $+ V_{DD}$ or fall below V_{SS}, the current through the input diodes should be limited to 10 milliamperes or less to assure safe operation.[1]

Reference

1. For additional operating considerations see "Guide to Better Handling and Operation of CMOS Integrated Circuits," J. Flood, H. L. Pujol, RCA Solid State Application Note ICAN-6525.

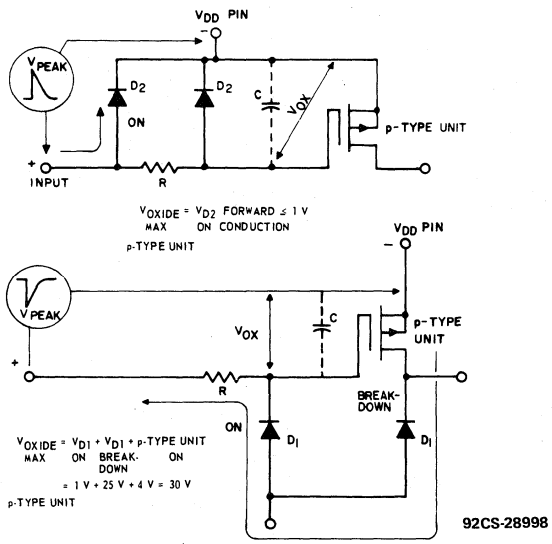


Fig.6 — Circuits used to provide protection between input pin and V_{DD} pin.

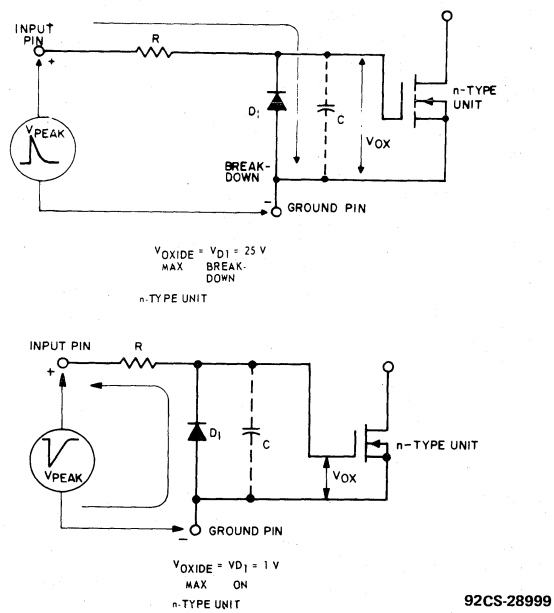


Fig.7 — Circuits used to provide protection between input pin and ground pin.

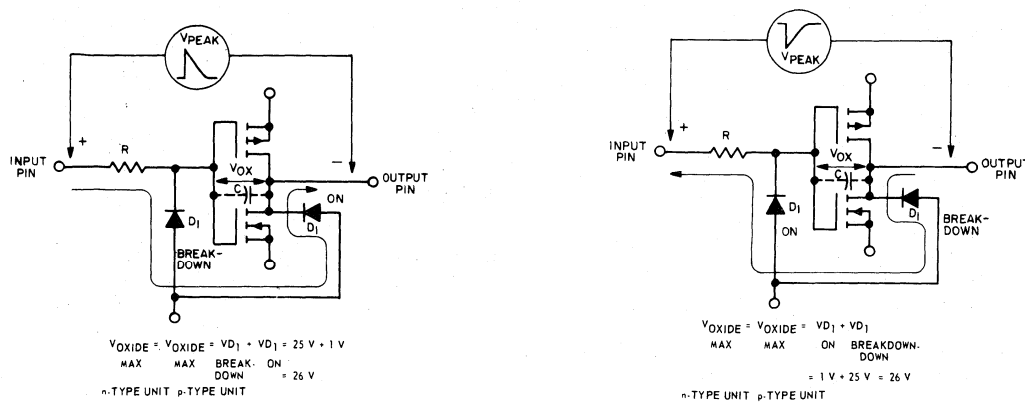


Fig.8 — Circuits used to provide protection between input pin and output pin.

Noise Immunity of COS/MOS B-Series Integrated Circuits

by T. Chesney
R. Funk

The excellent noise-immunity characteristics of COS/MOS (complementary-symmetry/metal-oxide-semiconductor) digital IC's is a paramount reason for their preferred and successful use in high-noise automotive, process-control, production-monitoring, and similar harsh-noise-prone applications. The introduction of the RCA B-series COS/MOS devices furthers the well-known noise immunity advantages of the COS/MOS technology in two important ways:

1. Improved noise-energy immunity as a result of balanced low-impedance output circuitry in all RCA B-series COS/MOS devices.

2. Standardized (EIA-JEDEC standards) dc noise-immunity and noise-margin ratings covering buffered and unbuffered CMOS-logic types.

Included in this Note are brief discussions of logic-system noise and rejection concepts, COS/MOS dc/ac noise-immunity specifications and definitions, and dc/ac noise-immunity performance data for several B-series COS/MOS gates, inverters, and high-current drivers.

Logic-System Noise Concepts

Successful application of any digital-logic IC family requires consideration of the following:

1. Externally or internally generated noise — both radiated and conducted.

2. The inherent noise-immunity capability of the logic family selected.

3. System noise-rejection measures.

Without coordination of these three points, a system design may perform unfavorably.

Consider first the various system or environmental noise generating sources. External system noise may include the noise imposed upon a logic system by electric motors, welders, rf transmitters, x-ray machines, high-current solenoids or relays, pulsed lasers, and circuit breakers. All of the preceding emit EMI (electromagnetic interference), and many produce power-line or ground-path noise disturbance. External noise is characterized by randomly occurring high-energy transients that are not easily anticipated. Usually, this noise is coupled electromagnetically or capacitively to signal, supply, and ground lines. Internal logic-system noise is usually generated on logic-signal lines by capacitively coupled crosstalk or by logic-switching current surges on supply lines or ground lines. In ultra-high-speed logic families such as ECL, reflection noise resulting from an impedance mismatch is also an internal noise problem; but because of relatively long output transition times of CMOS devices (more than 10 nanoseconds), reflection noise can be excluded from further consideration.

Since both external and internal noise must be considered, logic systems must be designed to survive in a medium to severe noise environment, a fact that leads to the second consideration, selection of an IC logic family having noise-rejection characteristics appropriate to the application. As is demonstrated below by considerable data, B-series COS/MOS devices have good dc and ac and noise-energy immunity characteristics. No matter how good the noise-rejection capability of a logic IC family, such as COS/MOS, system design measures to reduce noise entry into logic signal lines, power supply lines, and the ground are usually necessary to some extent. The methods most commonly used to minimize noise effects in COS/MOS logic systems are:

1. **Power-source line decoupling** - Good practice suggests use of a small-value series resistor and zener diode and a capacitor to ground on each logic card or each 50 to 100 IC's. High-voltage supply transients can usually be rejected by this simple measure. Separate lines should be used for logic circuits and power switching circuits.

2. **Ground-Line Noise** - In a system in which many high-current switching components, such as motors, relays, and SCR's are involved, logic grounds should be separated from high energy component grounds. The logic grounds should be returned to a common point.

3. **AC noise on system signal inputs** - 60 Hz is a commonly used frequency reference. Raw ac power lines should be isolated using a transformer or optical coupler. Zener-diode limiters are also effective. 60-Hz signals can be shaped by using COS/MOS Schmitt-trigger circuits.

NOISE SPECIFICATIONS

COS/MOS noise immunity is characterized by dc specifications, ac noise-immunity performance, and noise-energy immunity performance. Each of these characteristics is defined below and supported by performance data.

DC Specifications

Table I shows the industry standardized (JEDEC) noise immunity and noise margin ratings, V_{IL} and V_{IH}, for B-series devices. Note that separate specifications have been established for B (buffered) types and UB (unbuffered) types.[1]

Two important noise characteristics can be defined by using the V_{IL} and V_{IH} ratings:

1. **Noise Immunity** - The V_{IL} and

V_{IH} limits are the device input-signal noise-immunity ratings which, as defined in Table II, are 30, 30, and 27 percent, respectively, of the 5, 10, and 15-volt supply voltages for the B-series types. Percentages are lower for unbuffered gates, as shown in Table II. The V_{IL} and V_{IH} ratings define the maximum permissible additive noise voltages at an input terminal when input signals are 50 millivolts off the supply rails.

2. **Noise Margin** - The difference between V_{IL} and V_O or V_{IH} and V_O is the device noise-margin voltage for the noninverting case. Table II designates the B and UB noise-margin voltages. Noise margin voltage is defined as that noise voltage that can be impressed upon V_{IN} at any (or all) logic I/O terminals without upsetting the logic or causing any output to exceed the V_O ratings of Table I.

Of the two COS/MOS dc noise definitions, immunity and margin, RCA prefers the noise-immunity specification as the more practical COS/MOS system definition because CMOS outputs are normally 50 millivolts off the rails.

However, designers familiar with TTL may prefer to use the noise-margin voltage for system analysis.

AC Noise Immunity

COS/MOS ac noise immunity takes into account both the device switching threshold (dc noise immunity) and the noise-pulse width. The latter is affected primarily by the COS/MOS IC bandwidth, especially output transition times. Fig. 1 shows the usual COS/MOS noise-voltage amplitude, V_t, as a function of noise-pulse-width characteristic, t_p.

Because noise pulses are narrow compared with device output transition time, noise-voltage rejection is high. As the pulse widths approach the IC bandwidth, the curve flattens out at the device switching-threshold voltage. AC noise-voltage

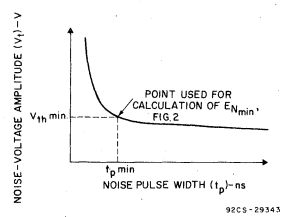


Fig. 1 Generic ac noise-immunity curve.

immunity curves, such as those in Fig. 1, are applicable to:

- Positive noise pulses on signal lines in the 0 state.
- Negative noise pulses on signal lines in the 1 state.
- Positive noise pulses on the ground terminal.
- Negative noise pulses on the positive supply terminal.

Curves of this type indicate the frequency (as defined by noise-pulse characteristics) at which the user has satisfactory dc noise performance. The curves are especially useful in calculating typical noise-energy performance, a parameter that takes into account the circuit impedance.

Noise-Energy Immunity

Noise-energy immunity takes into account the pulse width and the circuit impedance at the point where the noise is introduced. Noise-energy immunity, E_N, in nanojoules, is calculated as follows:

$$E_N = \frac{V_{th}^2}{R_O} t_p$$

where E_N is noise-energy immunity in nanojoules, V_{th} is the device switching-voltage threshold for a given noise-pulse width, t_p is the noise-voltage pulse width in nanoseconds, and R_O is the impedance to ground in ohms at the point of noise entry. R_O is usually the output resistance of the COS/MOS device.

By using values of V and t_p obtained from the curve of Fig. 1, the noise-energy immunity curve of Fig. 2 is generated for a

Table I – B-Series DC Noise Immunity and Noise Margin (T_A = 25°C)

Characteristics	Test Conditions		Input
	V_O (V)	V_{DD} (V)	Voltage (V)
Input Low Voltage V_{IL} max.			
B types	0.5/4.5	5	1.5
	1/9	10	3
	1.5/13.5	15	4
UB types	0.5/4.5	5	1
	1/9	10	2
	1.5/13.5	15	2.5
Input High Voltage V_{IH} min.			
B types	0.5/4.5	5	3.5
	1/9	10	7
	1.5/13.5	15	11
UB types	0.5/4.5	5	4
	1/9	10	8
	1.5/13.5	15	12.5

Table II – B-Series Noise Immunity and Noise Margin

	Noise Immunity (%)		Noise-Margin Voltage (V)	
V_{DD}	B-Series	UB-Series	B-Series	UB-Series
5	30	20	1	0.5
10	30	20	2	1
15	27	17	2.5	1

given value of R_Q. A comparison of Figs. 1 and 2 shows that the minimum values of

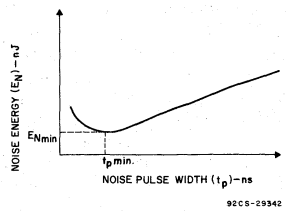


Fig. 2 Generic noise-energy-immunity curve.

noise-energy immunity occur at an input-noise pulse width for which the noise-voltage amplitude of Fig. 1 begins to approach the dc noise-immunity or threshold voltage of a device. The minimum noise-energy immunity is the basis for the calculations and comparisons involving most IC families.

NOISE-IMMUNITY TEST DATA

DC Noise-Immunity Test Data

CMOS dc noise-immunity performance is obtained by plotting the voltage-transfer characteristic of a CMOS gate, inverter, or buffer. Figs. 3 and 4 show the voltage-transfer characteristics of the CD4001B, a

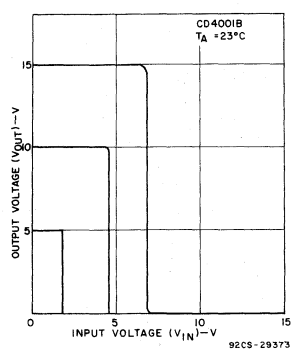


Fig. 3 CD4001B voltage transfer characteristic.

buffered, quad 2-input NOR gate, and the CD4001UB, an unbuffered version of the same gate. Comparison of Figs. 3 and 4 and Table I indicates that the values of V_{IL} and V_{IH} for these devices are well

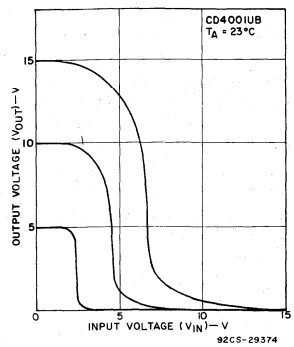


Fig. 4 CD4001UB voltage transfer characteristic.

within the standard JEDEC specifications. The V_{IL} and V_{IH} values for any typical COS/MOS device indicate a typical dc noise immunity close to 50 percent of the supply voltage, a paramount advantage of CMOS logic devices over TTL, ECL, PMOS, and NMOS logic devices.

AC Noise-Immunity Test Data

Fig. 5 shows the test circuit used in the evaluation of the ac noise immunity of B-series COS/MOS devices. The criterion used is the triggering of a typical CD4013B flip-flop at the clock input. The

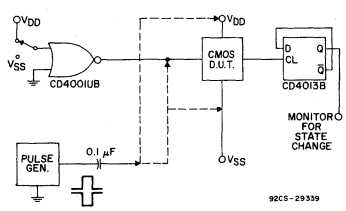


Fig. 5 Test circuit used in the evaluation of B-series COS/MOS devices.

circuit of Fig. 5 accounts for typical CMOS loading factors and generally reflects the ac noise performance of typical B-series devices. The device types used in the evaluation include the following:

CD4001UB unbuffered quad 2-input NOR gate,
CD4001B buffered quad 2-input 2-input NOR gate,
CD4011UB unbuffered quad 2-input NAND gate,
CD4069UB hex inverter,
CD4049UB hex inverting buffer.

The above list includes the most commonly used COS/MOS gates, inverters, and buffered devices. The ac noise-immunity characteristics of the buffered NOR gate (CD4001B) reflect the noise-immunity performance of buffered CMOS products of all descriptions.

SIGNAL-LINE OR EXTERNAL NOISE IMMUNITY

The following analysis was used to determine the immunity of a COS/MOS gate to noise on the input line at both the 0 (low-level) and 1 (high-level) logic states.

0-State Analysis

The signal-line noise immunity of COS/MOS gates and inverters was evaluated by means of the test circuit shown in Fig. 6. The COS/MOS units

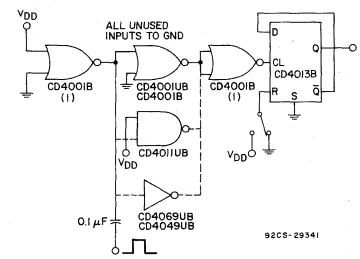
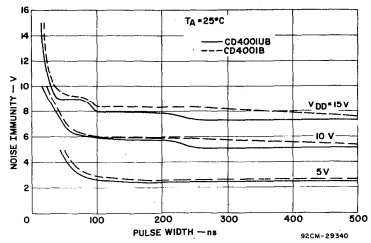


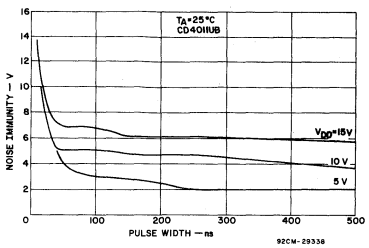
Fig. 6 Test circuit used to evaluate signal-line noise immunity of COS/MOS gates and inverters.

tested were the CD4001UB, CD4001B, CD4011UB, CD4049UB, and CD4069UB. Fig. 7 shows the results obtained. The test circuit is designed to measure the voltage required at the input of the unit under test to trigger a CD4013 flip-flop.

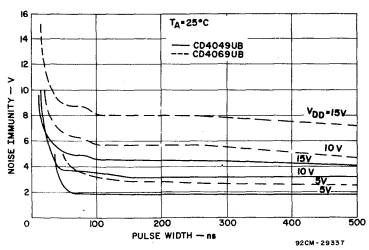
During test, a positive-going noise pulse is introduced into the signal line of the unit under test. At some voltage level, depending on the width of the pulse and the gate thresholds, this pulse causes the flip-flop to be clocked via the CD4001B gate. This voltage level defines the permissible input range for a logical 0.



(a) CD4001B, CD4001UB



(b) CD4011UB

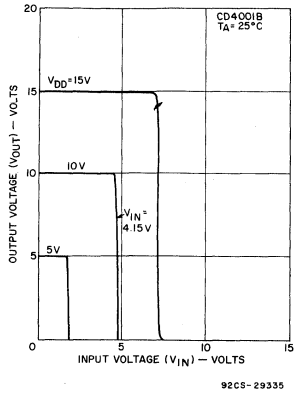


(c) CD4049UB, CD4069UB

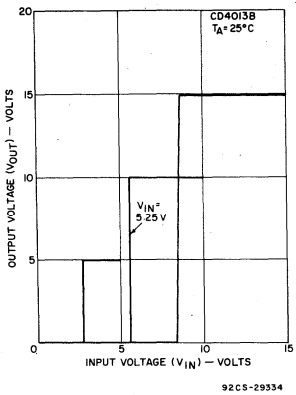
$T_A = 25°$

Fig. 7 Results of 0-state signal-line noise-immunity tests.

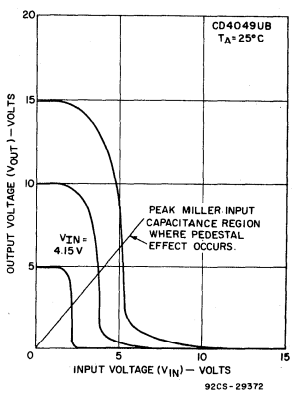
A dc analysis of the transfer characteristics of the components included in the test setup can also be used to determine the noise level required to clock the flip flop. Fig. 8(a) shows that a signal of 4.15 volts is required at the input to the CD4001B gate to produce an output of 4.5 volts at a supply voltage, V_{DD}, of 10 volts. Fig. 8(b) shows that an input of 5.25 volts is required to trigger the CD4013 flip-flop at a supply voltage, V_{DD}, of 10 volts. All measured values shown in Fig. 8 were obtained from measurements on gates that have typical threshold-switching characteristics.



(a) CD4001B



(b) CD4013B



(c) CD4049UB $T_A = 25°C$.

Fig. 8 Transfer characteristics of components used in the circuit of Fig. 6.

Careful analysis of the ac noise curves of Fig. 7(c) (for the CD4049UB) for 0-state signal-line noise shows a voltage-pedestal effect occurring at noise pulse widths associated with the noise-threshold region of the units under test. A comparison of the voltage-transfer curves of Fig. 8(c) with the dynamic input capacitance curves for the CD4049UB, Fig. 9, reveals that this pedestal effect occurs in the same region as the peak Miller input capacitance, where the inverter is in its maximum linear-gain region. Most 0- and 1-state noise-voltage characteristics curves in this Note exhibit this pedestal effect to some degree.

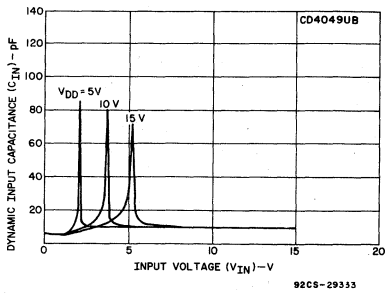


Fig. 9 Dynamic input capacitance curves for the CD4049UB. $T_A = 25°C$.

1-STATE ANALYSIS

Fig. 10 shows the test arrangement used and Fig. 11 the results obtained from noise-immunity measurements on the COS/MOS logic gates and inverters identified above when the input is high and a negative-going pulse is superimposed on the signal line.

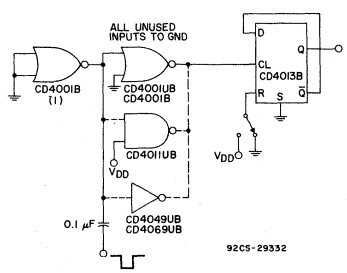
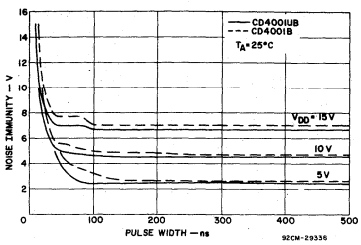
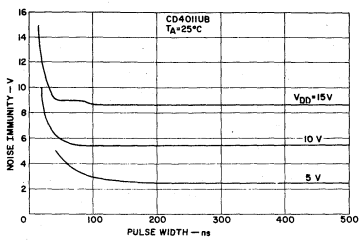


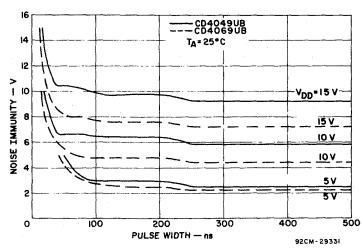
Fig. 10 Test circuit used to measure noise immunity of COS/MOS logic gates and inverters when the input is high and a negative-going pulse is superimposed on the signal line.



(a) CD4001B, CD4001UB



(b) CD4011UB



(c) CD4049UB, CD4069UB

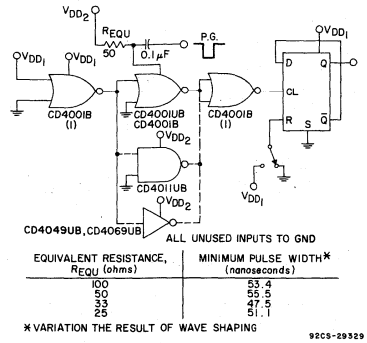
$T_A = 25°C$.

Fig. 11 Results of 1-state signal-line noise-immunity test.

POWER-SUPPLY NOISE IMMUNITY

The test configuration shown in Fig. 12 measures the ability of test units to withstand a negative-going noise pulse superimposed on the supply line without a change in state; Fig. 13 shows results of tests. A pulse of sufficient amplitude causes the output of the gate to decrease so that, at some point, the CD4013B flip-flop is triggered from the rising voltage at the output of the driving inverter stage.

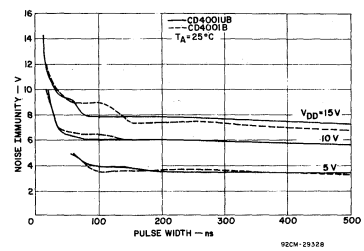
It should be noted that two power supplies are used in the arrangement of Fig. 12. An equivalent resistor or inductor



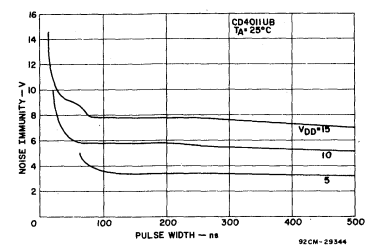
EQUIVALENT RESISTANCE, R_{EQU} (ohms)	MINIMUM PULSE WIDTH* (nanoseconds)
100	53.4
50	55.5
33	47.5
25	51.1

*VARIATION THE RESULT OF WAVE SHAPING

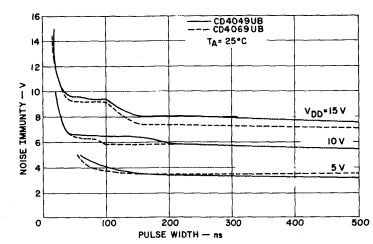
Fig. 12 Test circuit used to measure the ability of test units to withstand a negative-going noise pulse on the supply line without a change in state.



(a) CD4001B, CD4001UB



(b) CD4011UB



(c) CD4049UB, CD4069UB

$T_A = 25°C$.

Fig. 13 Power-line noise immunity.

for simulating contact resistance and lead length is used in the V_{DD} line of the unit under test. Without this resistance the test unit will not react to the noise pulse.

GROUND-NOISE IMMUNITY

Noise on the power line may be effectively reduced or eliminated by the use of decoupling capacitors; however, ground-line noise cannot be reduced so easily and, therefore, is more objectionable. Fig. 14 shows the test circuit used to measure the ground-line noise immunity of COS/MOS gates and inverters; Fig. 15 shows curves of the results obtained. Again, the units under test would not react to the noise unless a 25-ohm resistor or small inductor simulating lead length or contact resistance were placed to ground.

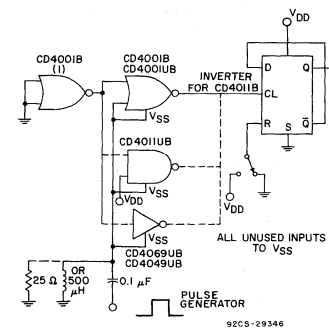
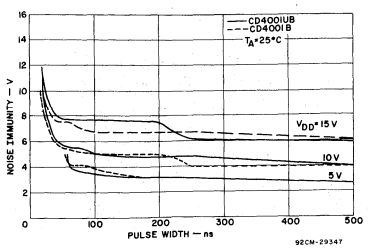


Fig. 14 Circuit used to measure ground-line noise immunity.

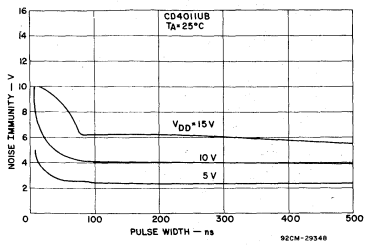
CROSSTALK NOISE IMMUNITY

A test circuit used to evaluate crosstalk is shown in Fig. 16. A noise pulse from a pulse generator is coupled to the signal line of the gate or inverter through a capacitor. The noise voltage necessary to trigger the flip-flop is then measured for different values of capacitance under high and low input conditions. Fig. 17 shows the effect of capacitance on the inputs of the units under test.

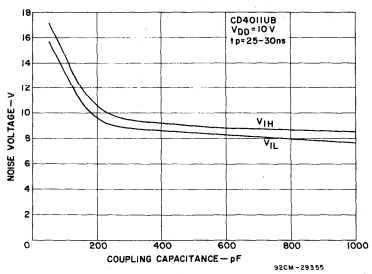
The circuit shown in Fig. 18 more closely approximates crosstalk caused by adjacent signal lines. The response of the test circuit to a noise pulse may be explained by analysis of the response of a high-pass RC circuit to a ramp input of $V_i = \alpha t$, where α is the coefficient of



(a) CD4001B, CD4001UB



(b) CD4011UB



(c) CD4049UB, CD4069UB

Fig. 15 Ground-line noise-immunity measurements.

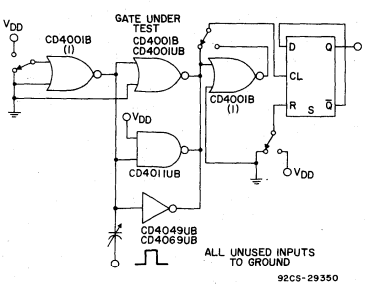
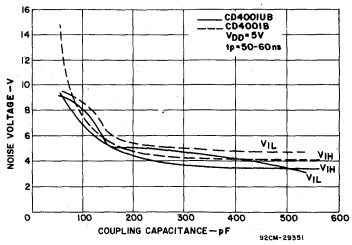
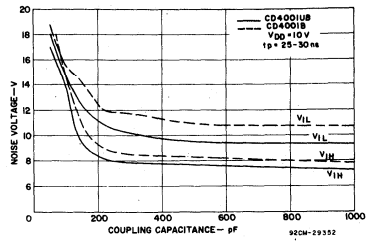
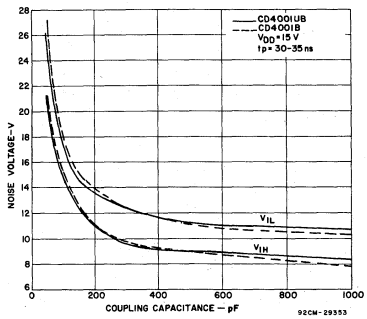
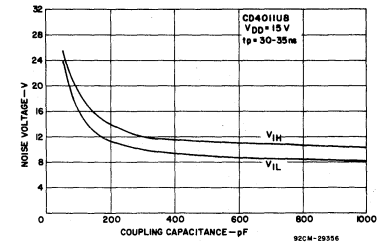


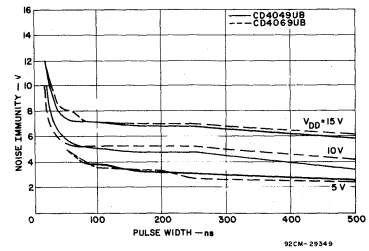
Fig. 16 Circuit for measuring noise voltage as a function of coupling capacitance.

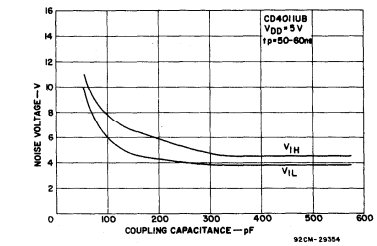


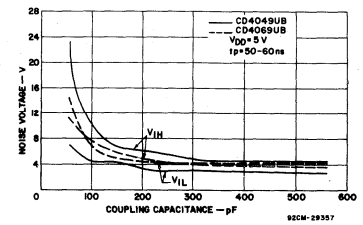


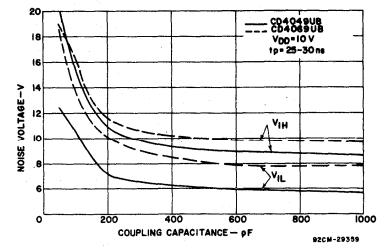












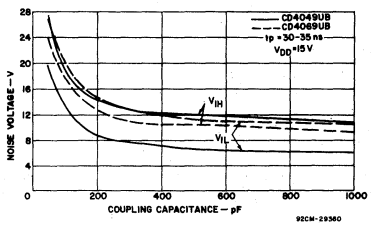


Fig. 17 Effect of coupling capacitance on the inputs of the units under test (T_A = 25°C).

coupling and t is rise time, 10 to 90 percent. The output voltage V_O may be expressed by the following equation:

$$V_O = \alpha RC\,(1\text{-}e^{-t/RC}) \qquad (1)$$

The equivalent circuit for the part of the test configuration used in this analysis is shown in Fig. 19. On the basis of this equivalent circuit, Eq. (1) may be rewritten as follows:

$$V_O \text{ max} \cong \propto (Z_O \parallel Z_{IN}\, C\,[(1-e^{t/2Z_O \parallel Z_{in}})\, C] \qquad (2)$$

If V_i is assumed to be $\propto t$ during the period in which the output voltage switches from 10 to 90 percent of its total value, this change in output voltage can be expressed as follows:

$$\Delta V_O \text{ max} \approx \frac{V_i\,(Z_o \parallel Z_{in})\,C}{t} \cdot [i\text{-}e^{-t/2}\, Z_o \parallel Z_{in})\, C] \qquad (3)$$

The results of this analysis may be applied to the various crosstalk waveforms obtained.

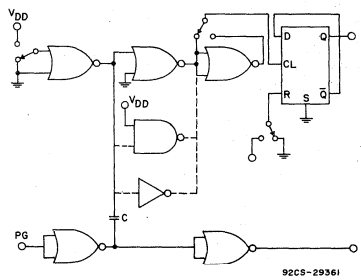


Fig. 18 Circuit closely approximating conditions for crosstalk on adjacent signal lines.

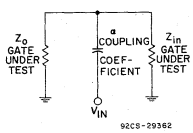


Fig. 19 Equivalent circuit used in crosstalk analysis of test configuration shown in Fig. 18.

Crosstalk measurements that simulate actual operation are made by use of the test circuits shown in Figs. 20 and 21. The circuit of Fig. 20 simulates a round-cable system and Fig. 21 a ribbon-cable system.

In Fig. 20, a sense line is placed tightly within five surrounding wires (No. 22 gauge) to form a 6-foot-long cable with a capacitance of 18 picofarads per foot (determined by measurement).

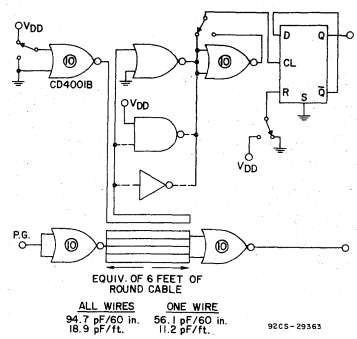


Fig. 20 Circuit simulating a round-cable system.

In Fig. 21, a sense line is placed between two adjacent driving lines (No. 22 gauge) of a 6-foot-long ribbon cable with a capacitance of 16 picofarads per foot (determined by measurement).

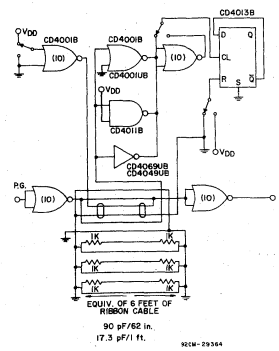


Fig. 21 Circuit simulating a ribbon-cable system.

The results of crosstalk are shown in the photographs of Figs. 22 and 23 for round cable and ribbon cable, respectively. The crosstalk was insufficient to trigger the CD4013B under all conditions of the circuits of Figs. 20 and 21.

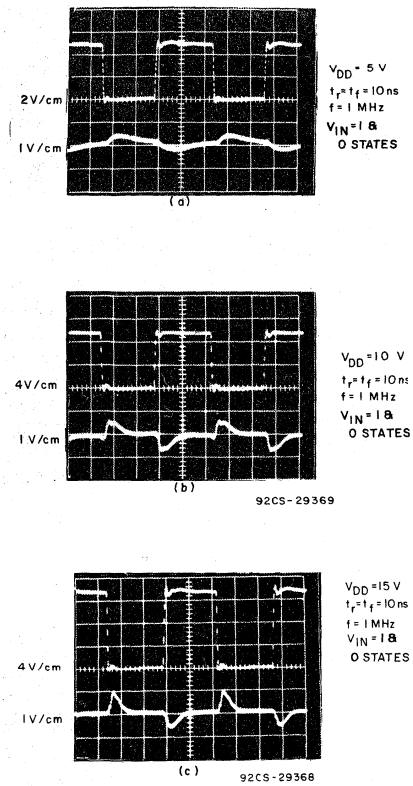


Fig. 22 Crosstalk in the round-cable system.

NOISE-ENERGY-IMMUNITY PERFORMANCE DATA

Table III shows computed values of noise-energy immunity for the gate, inverter, and buffer types identified above. Noise pulse width, t_p, and noise threshold voltage, V_T, data were obtained directly from the 1 and 0 signal-input ac noise-immunity test curves presented earlier in this Note, Figs. 7 and 11. Values of R_o are typical output impedances for the CD4001B driving gate used in obtaining the curves. Fig. 24 is a plot of high- and low-input state noise-energy immunity for the CD4001B gate as a function of input pulse width. These curves show that noise-energy immunity is high for noise bandwidths that exceed the speed capability of the device, and a minimum of approximately 1.3 nanojoules where the noise-pulse width (50 to 100 nanoseconds) approximates the device output transition time. Noise-threshold energy increases steadily with greater pulse widths.

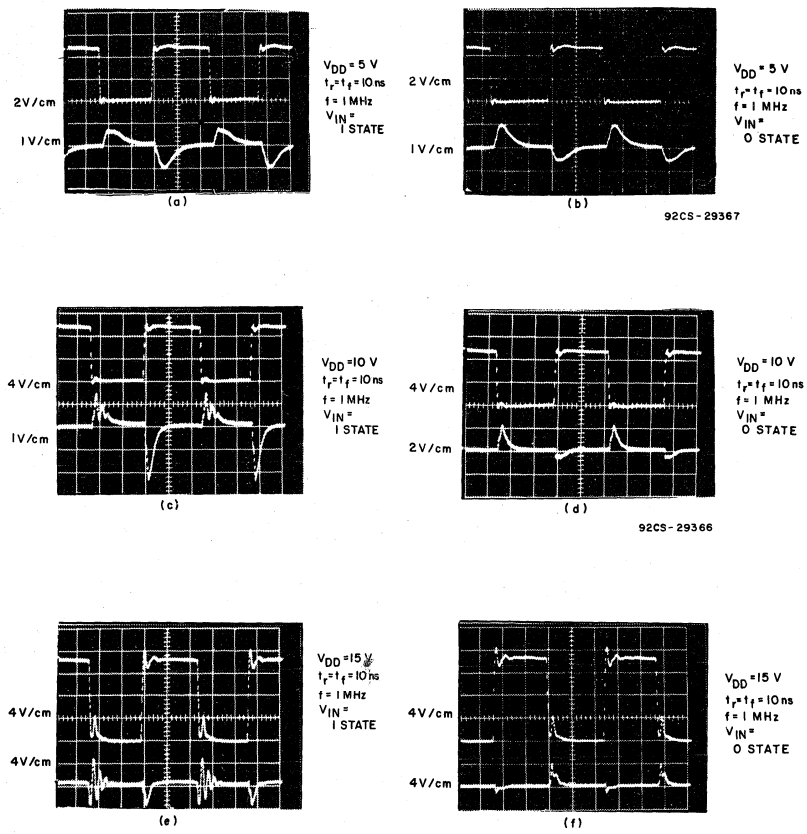


Fig. 23 Crosstalk in the ribbon-cable system.

Table III – Typical Values of Noise-Energy Immunity.

TYPE	SUPPLY VOLTAGE V_{DD} (V)	NOISE PULSE WIDTH t_p (ns)		NOISE THRESHOLD VOLTAGE V_t (V)		TYPICAL SIGNAL LINE IMPEDANCE R_O (ohms)		TYPICAL NOISE-ENERGY IMMUNITY* LOGIC STATE	
								LOW	HIGH
		LOW	HIGH	LOW	HIGH	R_{OL}	R_{OH}	E_{NL}(nJ)	E_{NH}(nJ)
CD4001UB	5	100	100	2.75	2.65	700	700	1.08	1.00
	10	60	40	6.3	5.1	270	270	8.82	3.85
	15	40	40	9.0	7.0	190	190	17.05	10.32
CD4001B	5	160	150	2.58	2.85	700	700	1.52	1.74
	10	80	40	6.2	5.6	270	270	11.40	4.65
	15	40	40	9.6	7.8	190	190	19.40	12.81
CD4011UB	5	100	140	3.0	2.67	700	700	1.29	1.43
	10	40	80	5.0	5.45	270	270	3.70	8.80
	15	60	40	6.9	9.1	190	190	15.03	17.43
CD4049UB	5	60	120	2.0	2.9	700	700	0.343	1.44
	10	40	40	3.7	6.7	270	270	2.03	6.65
	15	60	40	4.9	10.4	190	190	7.58	22.77
CD4049UB	5	150	150	2.75	2.60	700	700	1.62	1.45
	10	60	60	6.4	5.2	270	270	9.10	6.01
	15	40	60	8.7	8.0	190	190	15.94	20.21

$$*E_N = \frac{V_t^2}{R_O}(t_p)$$

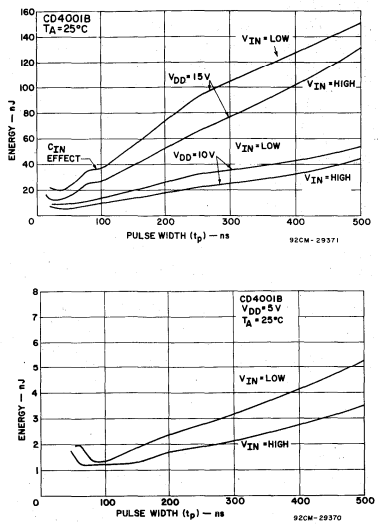


Fig. 24 High- and low-input state noise-energy immunity for the CD4001B gate as a function of input pulse width. T_A = 25°C.

CONCLUSIONS

The noise-immunity test data demonstrates the high noise immunity of COS/MOS digital integrated circuits. Typical ac noise-voltage immunity for an unbuffered gate is 2 volts for a 5-volt supply, 5 volts for a 10-volt supply, and 7 volts for a 15-volt supply. As expected, the low-level ac noise-immunity for the CD4049UB buffer is slightly lower because of the lower effective input threshold of the large NMOS transistor used.

Of paramount interest is the good noise-energy performance of approximately 1.3 nanojoules for B-series gates, which is comparable to the performance of bipolar TTL gates at 5 volts despite their much higher output drive current. At operation above 5 volts, the noise-energy immunity of COS/MOS devices ranges up to 20 nanojoules at 15 volts, far exceeding the noise-energy immunity of TTL. This improved noise immunity makes CMOS logic devices far more economical to use in high-noise automotive and industrial control environments than TTL devices. This noise-rejection capability exceeds even that of bipolar high-threshold logic, which has only approximately 5 nanojoules of noise-energy rejection in the high logic-input state.

The good inherent noise immunity provided by COS/MOS devices leads to design economy, and complements the accompanying benefits of COS/MOS: low-cost, medium- to high-speed operation, wide operating voltage range, good temperature stability, wide selection of SSI, MSI, and LSI device types, etc.

References

1. "Understanding Buffered and Unbuffered CMOS Characteristics," R.E. Funk, RCA Solid State Application Note ICAN-6558.

2. "Noise Immunity of COS/MOS Integrated Circuits," S.S. Eaton, RCA Solid State Application Note ICAN-6176. Discusses noise immunity of A-series devices.

3. "Designing Logic Circuits for High Noise Immunity," Verell Boaen, IEEE Spectrum, Jan. 1973.

4. JEDEC Standard for B-series COS/MOS devices.

Application Note Abstracts

COS/MOS DIGITAL INTEGRATED CIRCUITS

ICAN-6080 . . . . . 6 pages
Digital-to-Analog Conversion Using the RCA CD-4007A COS/MOS IC

The use of the RCA-CD4007A COS/MOS dual complementary pair plus inverter as a digital-to-analog (D/A) switch is demonstrated. The op-amp output stage for the digital-to-analog converter (DAC) uses COS/MOS and bipolar transistor-array IC's. Resistance networks for DAC's, the design of a voltage-follower amplifier for single supply operation, and a 9-bit COS/MOS DAC are described.

ICAN-6086 . . . . . 12 pages
Timekeeping Advances Through COS/MOS Technology

Most COS/MOS timing circuits consist of an oscillator, some digital processing logic, and logic-circuit drivers. This Note discusses oscillator design (including crystal characteristics and feedback circuit and oscillator-amplifier configurations), practical COS/MOS oscillator circuits, frequency dividers, and COS/MOS timing-circuit applications in wristwatches, wall clocks, and automobile clocks.

ICAN-6101 . . . . . 8 pages
The RCA COS/MOS Phase-Locked-Loop – A Versatile Building Block for Micro-Power Digital and Analog Applications

The phase-locked-loop described in this Note is the COS/MOS CD4046A, which consumes only 600 microwatts of power at 10 kHz, a power consumption 160 times *less* than the 100 milliwatts required by similar monolithic bipolar PLL's. The Note discusses the fundamentals of phase-locked-loops and presents a detailed technical description of the COS/MOS PLL as well as its application in FM demodulators, frequency synthesizers, split-phase data synchronization and decoding, and phase-locked-loop lock detection.

ICAN-6166 . . . . . 16 pages
COS/MOS MSI Counter and Register Design and Applications

Logic and schematic diagrams for counter and register types CD4006A, CD4014A, CD4015A, CD4018A, CD4020A, CD4021A, CD4022A, and CD4024A are presented; circuit designs are outlined and device-design trade-off's are discussed. Performance criteria are summarized and applications by type are outlined by means of logic or subsystems diagrams and waveforms photographs.

ICAN-6176 . . . . . 8 pages
Noise Immunity of COS/MOS Integrated-Circuit Logic Gates

The types of noise usually encountered in a logic system are discussed and the noise immunity of a COS/MOS integrated-circuit logic-gate test circuit in relation to system variables is evaluated. The evaluation is performed on a circuit that includes a CD4000A dual 3-input gate plus inverter and a CD4001A quad 2-input gate connected in cascade to drive a CD4013A flip-flop. Measurement of the voltage required at various gate leads to switch the flip-flop defines the noise immunity threshold of the gate circuits.

ICAN-6210 . . . . . 11 pages
A Typical Data-Gathering and Processing System Using CD4000A-Series COS/MOS Parts

This Note is developed in terms of a typical system for process controls. The flexibility of system design and common data-bus architecture made possible by the three-state outputs and bidirectional input/outputs incorporated in many COS/MOS circuits are stressed, as is the ease of system design for data handling in increments of 4 bits made possible by the CD4000A family. The implementation of the system is shown in terms of the COS/MOS standard parts that can be used to perform the desired system functions. Attention is focused on the multiplicity of applications and the scope of information processing that can be covered by standard parts.

ICAN-6218 . . . . . 2 pages
Gate Oxide Protection Circuit in RCA COS/MOS Digital Integrated Circuits

A protection circuit developed by RCA to reduce the problem of gate-oxide failure in COS/MOS integrated circuits is presented. The circuit has been shown to be effective in minimizing occurrences of gate-oxide failure and, when used in conjunction with the handling guidance contained in ICAN-6000, "Handling Considerations for MOS Integrated Circuits," in eliminating the problem entirely.

ICAN-6224 . . . . . 2 pages
Radiation Resistance of the COS/MOS CD4000A Series

Two types of radiation resistance, permanent and temporary, are discussed, and the radiation resistance of CD4000 and CD4000A series devices are compared. The use of shielding to increase resistance is examined.

ICAN-6230 . . . . . 13 pages
Using the CD4047A in COS/MOS Timing Applications

This Note compares the theoretical and actual performance of oscillator circuits with that of the CD4047A. The device functions as either an oscillator or one-shot and meets the power dissipation, stability, and speed requirements of most COS/MOS systems. Applications discussed include a noise discriminator, a frequency discriminator, a low-pass filter, a band-pass filter, an envelope detector and a pulse generator. Four appendixes amplify test material.

ICAN-6267 . . . . . 8 pages
Astable and Monostable Oscillators Using RCA COS/MOS Digital Integrated Circuits

This Note describes several techniques that may be used to compensate for the normal threshold variation of MOS devices in the design of stable multivibrator circuits for operation at frequencies up to 1 MHz. The circuits shown can be formed by use of COS/MOS inverters and NAND or NOR gates connected in an inverter configuration. The Note also describes various applications for COS/MOS multivibrator circuits (e.g.: voltage-controlled oscillators, voltage-controlled pulse-width circuits, phase-locked voltage-controlled oscillators, frequency multipliers, and modulator/demodulators (envelope detectors). Specific data relate to use of "A" series gates.

ICAN-6289 . . . . . 12 pages
A COS/MOS PCM Telemetry and Remote Data Acquisition Design

Descriptive background material on telemetry systems is given along with systems for both immediate and remote data conversion and transmission. Parts from the CD4000 family are used to show how various sections of the system may be realized in the general case. The exact configuration of any specific system will, of course, depend on the unique requirements of the application.

ICAN-6304 . . . . . 5 pages
Power Supplies for COS/MOS

Examples of various COS/MOS power-supply circuits and their relative costs are given along with factors important in their design. Design examples include low-frequency systems, mixed systems of 2-MHz and 50-kHz circuits, a COS/MOS system powered by a 5-volt TTL supply, and battery-powered systems. Design considerations discussed include operating frequency, noise immunity, power dissipation, and regulation.

ICAN-6362 . . . . . 10 pages
Using the CD4520B to Design Dividers with Symmetrical Outputs

The general-purpose COS/MOS dual up-counter, the CD4520B, a counter that may be used in various counting and dividing applications is discussed. Dividers of the form $N=2^i \pm 1$ and $N=2^i + 1$ and described. Applications of symmetrical dividers are also discussed.

ICAN-6374 . . . . . 8 pages
The COS/MOS CD4059A Programmable Divide-by-N Counter in FM and Citizens-Band-Transceiver Tuners

The frequency synthesis capability of the CD4059A programmable divide-by-N counter is demonstrated in applications in an FM digital tuner and in the digital tuner for a citizens-band tranceiver. The digital approach described in the paper allows desired frequencies to be selected by depressing numbered buttons on a keyboard. By using the appropriate basic circuitry along with a phase-locked-loop circuit, the local oscillator of the receiver is adjusted and locked to the proper frequency, thus assuring proper station selection. Alternate methods of station selection that enhance the flexibility of the system are described.

ICAN-6445 . . . . . 8 pages
Memory-System Characteristics and Applications of the CD4061A

The CD4061A 256-word by 1-bit RAM is a versatile building block in medium-scale memory systems. This Note describes circuit and system applications concepts of the device and includes design, timing, performance and testing details for a practical memory-system.

ICAN-6498 . . . . . 6 pages
Design of Fixed and Programmable Counters Using the RCA CD4018A COS/MOS Presettable Divide-by-N Counter

The use of the CD4018A single-decade and multidecade fixed and programmable divide-by-N counters are described. System considerations such as switch simplifications, components minimization, and speed are also discussed.

ICAN-6563 . . . . . 4 pages
Radiation Resistance of the COS/MOS CD4000A and CD4000B Series

COS/MOS integrated circuits possess many advantages that recommend their use in radiation-susceptible space and military environments. Several of the most significant of these advantages are: ultra-low standby-power consumption, high noise immunity, extremely high packaging density, and inherently high reliability. Latest radiation-process improvements and resultant production studies indicate that some 1976 product exhibits radiation-resistance levels up to and beyond 1×10^6 rads (si). RCA expects to have production CD4000A and B series product available to 1×10^6 rads (Si) in 1977.

ICAN-6564 . . . . . 4 pages
Applications of CD40107BE COS/MOS Dual NAND Buffer

This Note describes the characteristics of the COS/MOS dual NAND buffer, the CD-40107BE, and the wide variety of practical applications in which this important addition to the CD4000-series of COS/MOS devices can be used.

ICAN-6576 . . . . . 6 pages
Power-Supply Considerations for COS/MOS Devices

This Note describes those features of COS/MOS devices that permit them to operate from a wide range of power sources. The Note also provides the system designer with the information he needs to design an economical power supply for his COS/MOS system. Features discussed are quiescent device dissipation, switching characteristics, and ac dissipation and performance characteristics. The calculation of system power, regulation and filtering requirements, and high-dc sources are also discussed along with a battery standby system.

ICAN-6600 . . . . . 6 pages
Arithmetic Arrays Using Standard COS/MOS Building Blocks

The design of a COS/MOS arithmetic unit capable of adding, subtracting, multiplying, and dividing is described. The device is also able to perform the logical functions of OR, AND and the Exclusive OR of two 4-bit words. Three 4-bit registers are provided that permit either of two words to perform a desired operation with a third word. The system is configured with standard, commercially available COS/MOS devices, which include registers, AND-OR select gates, a full adder, and NOR and NAND gates.

ICAN-6601 . . . . . 12 pages
Transmission and Multiplexing of Analog or Digital Signals Utilizing the CD4016A Quad Bilateral Switch

The CD4016A quad bilateral switch is the ideal semiconductor switch for use in switching applications; it can be used for the transmission of analog or digital signals with low distortion. The Note discusses features of the device; operation of the COS/MOS switch; switch and logic applications, including switch and logic functions; multiplexing/demultiplexing; digital control of signal gain, frequency, and impedance, including resistor networks, and variable frequency control; digital-to-analog conversion, including weighted resistor networks for the D/A converter, and an R-2R resistor ladder D/A converter; sample-and-hold applications; and squelch control (level detection).

ICAN-6602 . . . . . 12 pages
Interfacing COS/MOS with Other Logic Families

The RCA CD4000A COS/MOS series circuits operate from power-supplies of 3 to 15 volts. Thus, they can drive and be driven by a number of logic families, including all DTL and TTL families, within certain conditions and limitations. This Note describes the conditions of interface.

ICAN-6716 . . . . . 15 pages
Low-Power Digital Frequency Synthesizers Utilizing COS/MOS IC's

A digital frequency synthesizer that employs a digital phase-locked loop and other COS/MOS circuits is described. Following a reveiw of phase-locked-loop fundamentals, the use of COS/MOS devices in FM receiver systhesizers is discussed.

ICAN-6733 . . . . . 16 pages
Battery-Powered Digital-Display Clock/Timer and Metering Applications Utilizing the RCA CD4026A and CD4033A Decode Counters – 7 Segment Output Types

This Note describes the CD4033A and CD4026A and their use with various 7-segment display units presently available. Interface packages and methods are discussed to help the the designer select the best system to meet his demands. Also included are battery-operated systems for digital clocks and watches.

ICAN-6739 . . . . . 12 pages
COS/MOS Rate Multipliers – Versatile Circuits for Synthesizing Digital Functions

COS/MOS rate multipliers, the CD4527B and CD4089B, can be used as building blocks to generate a range of digital functions in low-power systems where minimum package count is desirable. The circuits may be employed in numerical control, instrumentation, digital filtering, and frequency synthesis. When used with an up/down counter and control logic, they can be used to perform such operations as multiplication, addition, subtraction, generation of algebraic equations and differential equations, integration, and to raise numbers to various powers. Symmetric rate multiplication, the problem of eliminating round-off error in a direct frequency-synthesis application in a common-carrier multiplex system is also covered.

MICROPROCESSOR INTEGRATED CIRCUITS

ICAN-6562 . . . . . 2 pages
Register-Based Output Function for RCA COSMAC Microprocessors

This Note describes a circuit for use with RCA COSMAC Microprocessors; the circuit provides the capability to output information from any of the 16 general-purpose scratch-pad registers contained within the CPU. This circuit is of particular interest to users constrained to operating with memory systems containing only ROM, or to users wishing to transfer 16 bits of data with a single Output instruction. The information given and the terminology used are presented with the assumption that the reader is familiar with the COSMAC architecture and manuals.

ICAN-6565 . . . . . 4 pages
Design of Clock Generators for Use with RCA COSMAC Microprocessor CDP1802

The CDP1802 features of static operation, single-phase clock input, and the on-chip oscillator amplifier make practical the use of a low-cost, highly stable, crystal-controlled oscillator as its clock generator. In addition to the oscillator amplifier, the CDP1802 incorporates all necessary start/stop logic on-chip. This application note describes clock generator designs suitable for various applications.

ICAN-6581 . . . . . 2 pages
Power-On Reset/Run Circuits for the RCA CDP1802 COSMAC Microprocessor

This Note describes several circuits which enable a power-on reset/run capability for COSMAC microprocessor systems. It is assumed that the user is familiar with the hardware considerations for the CDP1802 as explained in the **User Manual for the CDP1802 COSMAC Microprocessor, MPM-201A.**

ICAN-611 . . . . . 4 pages
Keyboard SCAN Routine for Use with COSMAC Microterminal CDP18S021

The COSMAC Microterminal CDP18021 provides general purpose subroutines in UT5 so that the Microterminal can be used as an output display device by the user program being run. In particular, the REGDIS subroutine sends the contents of registers RA and RB to the display while the LEDD subroutine provides independent control of all eight display digits and decimal points. However, UT5 does not contain a general purpose keyboard read routine that a user program can call. This Note contains the code for a keyboard reading routine that can be added as a subroutine in the user program to make the Microterminal useful as a general purpose input as well as output device.

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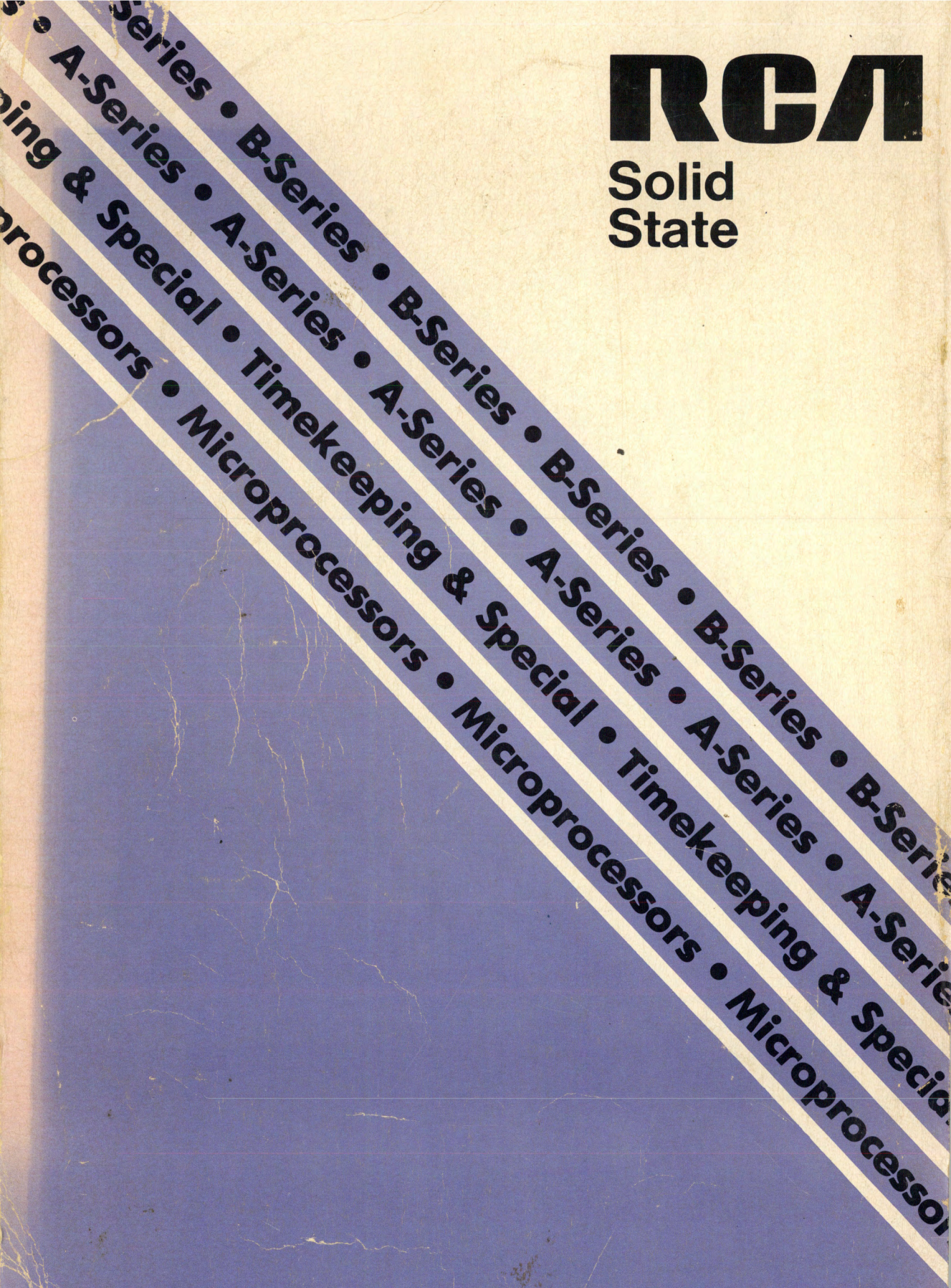
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